



GenRad

IC Test System Instruction Manual



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GR 1732 Digital IC Test System

Operation and Program Preparation

For 1732-9740 through 9744
and 1732-9720 through 9724

Form 1732-0104-05

Symbol  IEC 417 on equipment signifies that the manual contains information to prevent injury or equipment damage. Refer to Page iii and to other manuals in set.

Warnings and Cautions

WARNING—SHOCK HAZARD

The following instructions must be observed to prevent possible injury to personnel. Chassis must be earth grounded by direct wire, in addition to ground connection through power cord. Operators must not expose hazards by removing covers. Qualified service personnel must follow suitably safe procedures, appropriate to the particular hazards in the area of their maintenance or other work on the system.

On the rear panel, observe the warning "Dangerous voltages are present inside this system. Refer all servicing to qualified personnel."

On the rear of the control unit, observe the warning "Protective earth grounding provides protection from electric shock. This equipment must be earth grounded." Use the stud provided (near the power connector) to connect a directly grounded wire.

CAUTION

Observe the following precaution to prevent damage to the equipment. On the rear panel, observe the caution "For continued protection against fire, replace only with same type and rating of fuse."

CAUTION

This system tests sensitive electronic components that can be easily damaged by static discharges created by improper handling. Please refer to Section 2 of this manual for instructions to prevent such damage.

NOTE

The material in this manual is for information only and is subject to change without notice. GenRad assumes no responsibility for any errors or for damages that may result from the use or misuse of any of the procedures in this publication.

Specifications

DUT Power Supply

DEVICE POWER-SUPPLY VOLTAGES AND MAX AVAILABLE CURRENT

DPS†	Range	Resolution	Accuracy (±)*	Current Max
1	0 to +8 V	2 mV	(4 mV + 0.3% Set)	400 mA
2	0 to +19 V	5 mV	(10 mV + 0.3% Set)	160 mA
	+19 to +20 V	5 mV	(10 mV + 0.3% Set)	100 mA
3	0 to -7 V	2 mV	(4 mV + 0.3% Set)	160 mA
	-7 to -8 V	2 mV	(4 mV + 0.3% Set)	100 mA

†DUT power supply 1, 2, 3 corresponds to V1, V2, V3 in the parameters screen.

* "Set" means of setting; "Rdg" means of reading.

ACCURACY OF P-S CURRENT MEASUREMENT VS LIMIT IN TEST PROGRAM

Power Supply Current Range*	Meter Range	DPS†	Programmed Limit (Setting)	Resolution	Accuracy (±)**
Hi		1	+ (50 to 400) mA	100 μ A	(1.5 mA + 1.0% Set)
Med		1	+ (6.25 to 50) mA	12.5 μ A	(200 μ A + 0.6% Set)
Low		1	+ (0 to 6.25) mA	1.6 μ A	(25 μ A + 0.6% Set)
Hi		2	+ (20 to 160) mA	40 μ A	(1.5 mA + 0.7% Set)
Med		2	+ (2.5 to 20) mA	5 μ A	(200 μ A + 0.6% Set)
Low		2	+ (0 to 2.5) mA	0.625 μ A	(25 μ A + 0.6% Set)
Hi		3	-(20 to 160) mA	40 μ A	(1.5 mA + 0.7% Set)
Med		3	-(2.5 to 20) mA	5 μ A	(200 μ A + 0.6% Set)
Low		3	-(0 to 2.5) mA	0.625 μ A	(25 μ A + 0.6% Set)
Hi	X1	1	(200 to 400) mA	200 μ A	(400 μ A + 1.0% Rdg)
Hi	X2	1	(98 to 200) mA	100 μ A	(200 μ A + 0.8% Rdg)
Hi	X2	2,3	(98 to 160) mA	100 μ A	(200 μ A + 0.7% Rdg)
Hi	X4	1, 2, 3	(48 to 98) mA	50 μ A	(100 μ A + 0.6% Rdg)
Hi	X8	1, 2, 3	(23 to 48) mA	25 μ A	(50 μ A + 0.5% Rdg)
Hi	X16	1, 2, 3	(10 to 23) mA	12.5 μ A	(30 μ A + 0.5% Rdg)
Hi	X32	1, 2, 3	(4 to 10) mA	6.25 μ A	(20 μ A + 0.6% Rdg)
Hi	X64	1, 2, 3	(0 to 4) mA	3.125 μ A	(10 μ A + 0.7% Rdg)
Med	X1	1	(24 to 50) mA	25 μ A	(50 μ A + 0.5% Rdg)
Med	X2	1	(12 to 24) mA	12.5 μ A	(25 μ A + 0.5% Rdg)
Med	X2	2, 3	(12 to 20) mA	12.5 μ A	(25 μ A + 0.5% Rdg)
Med	X4	1, 2, 3	(6 to 12) mA	6.25 μ A	(13 μ A + 0.5% Rdg)
Med	X8	1, 2, 3	(2.8 to 6) mA	3.125 μ A	(6.5 μ A + 0.5% Rdg)
Med	X16	1, 2, 3	(1.3 to 2.8) mA	1.56 μ A	(3.5 μ A + 0.5% Rdg)
Med	X32	1, 2, 3	(0.5 to 1.3) mA	780 nA	(2.4 μ A + 0.6% Rdg)
Med	X64	1, 2, 3	(0 to 500) μ A	390 nA	(1.2 μ A + 0.7% Rdg)
Low	X1	1	(3.0 to 6.25) mA	3.125 μ A	(6.5 μ A + 0.5% Rdg)
Low	X2	1	(1.5 to 3.0) mA	1.56 μ A	(3.5 μ A + 0.5% Rdg)
Low	X2	2, 3	(1.5 to 2.5) mA	1.56 μ A	(3.5 μ A + 0.5% Rdg)
Low	X4	1, 2, 3	(0.75 to 1.5) mA	780 nA	(1.8 μ A + 0.5% Rdg)
Low	X8	1, 2, 3	(360 to 750) μ A	390 nA	(1000 nA + 0.5% Rdg)
Low	X16	1, 2, 3	(165 to 360) μ A	195 nA	(600 nA + 0.5% Rdg)
Low	X32	1, 2, 3	(65 to 165) μ A	98 nA	(400 nA + 0.6% Rdg)
Low	X64	1, 2, 3	(0 to 65) μ A	49 nA	(300 nA + 0.7% Rdg)

* Range resistors for "hi, med, low" are 10, 80, and 640 ohms, respectively, in each power supply and are determined by parameters-screen data rather than measured value.

** "Set" means of setting; "Rdg" means of reading.

† DUT power supply 1, 2, 3 corresponds to I1, I2, I3 in parameters screen.

Parametric Measurement Unit (PMU)

PMU FORCE-VOLTAGE/MEASURE-CURRENT SPECS

Voltage Range (force)	Resolution	Accuracy*	Available Current
-1 to +1 V	0.5 mV	(1 mV + 0.3% Set)	-150 mA to +330 mA
±(1 to 4) V	2 mV	(4 mV + 0.3% Set)	-100 mA to +280 mA
4 to 16 V	5 mV	(10 mV + 0.3% Set)	-100 mA to +100 mA

Current Range (measure)

-22 to +22 μ A	12 nA	(100 nA + 0.8% Rdg + B) or 1 count
±(22 to 47) μ A	24 nA	(125 nA + 0.7% Rdg + B) or 1 count
±(47 to 94) μ A	49 nA	(200 nA + 0.6% Rdg + B) or 1 count
±(94 to 188) μ A	98 nA	(300 nA + 0.6 Rdg + B) or 1 count
±(188 to 375) μ A	195 nA	(600 nA + 0.6% Rdg + B) or 1 count
±(375 to 750) μ A	390 nA	(1.2 μ A + 0.7% Rdg) or 1 count
±(0.75 to 1.5) mA	780 nA	(1.6 μ A + 0.6% Rdg) or 1 count
±(1.5 to 3) mA	1.56 μ A	(3.2 μ A + 0.6% Rdg) or 1 count
±(3 to 6) mA	3.125 μ A	±(6.4 μ A + 0.6% Rdg) or ± 1 count
±(6 to 12) mA	6.25 μ A	±(20 μ A + 0.7% Rdg) or ± 1 count
±(12 to 25) mA	12.5 μ A	±(26 μ A + 0.6% Rdg) or ± 1 count
±(25 to 50) mA	25 μ A	±(50 μ A + 0.6% Rdg) or ± 1 count
±(50 to 100) mA	50 μ A	±(100 μ A + 0.7% Rdg) or ± 1 count
-100 to -170 mA	100 μ A	±(200 μ A + 0.9% Rdg) or ± 1 count
+100 to +200 mA	Same	Same
+200 to +350 mA	200 μ A	±(400 μ A + 1% Rdg) or ± 1 count

* "Set" means of setting; Rdg means of reading. For current ranges up to 375 μ A, for relative humidity of 80% or less, in temperature range $25^{\circ}\text{C} \leq T < 40^{\circ}\text{C}$, $B = 10(T-25)$ nA, where T is the ambient temperature. For $0 < T < 25^{\circ}\text{C}$, $B = 0$.

PMU FORCE-CURRENT/MEASURE-VOLTAGE SPECS

Current Range (force)	Resolution	Accuracy*	Available Voltage (Volts)	
			For I < 0	For I > 0
-75 μ A to +75 μ A	39 nA	±(500 nA + 0.6% Set)	-(10 - 12800 lll) to +20	-10 to +(21 - 12800 lll)
±(75 to 300) μ A	156 nA	±(800 nA + 0.6% Set)	-(10 - 12800 lll) to +20	-10 to +(21 - 12800 lll)
±(0.300 to 1.25) mA	625 nA	±(1.7 μ A + 0.6% Set)	-(10 - 810 lll) to +20	-10 to +(21 - 810 lll)
±(1.25 to 5) mA	2.5 μ A	±(5 μ A + 0.6% Set)	-(10 - 810 lll) to +20	-10 to +(21 - 810 lll)
±(5 to 20) mA	10 μ A	±(20 μ A + 0.6% Set)	-(10 - 60 lll) to +20	-10 to +(21 - 60 lll)
±(20 to 80) mA	40 μ A	±(80 μ A + 0.7% Set)	-(10 - 60 lll) to +20	-10 to +(21 - 60 lll)
80 to 320 mA	100 μ A	±(200 μ A + 1% Set)	-(10 - 60 lll) to +20	-10 to +(21 - 60 lll)

Voltage Range (measure)

-300 to +300 mV	156 μ V	±(470 μ V + 0.5% Rdg) or ± 1 count
±(300 to 600) mV	312 μ V	±(630 μ V + 0.4% Rdg) or ± 1 count
±(0.600 to 1.25) V	625 μ V	±(1.25 mV + 0.3% Rdg) or ± 1 count
±(1.25 to 2.5) V	1.25 mV	±(2.5 mV + 0.3% Rdg) or ± 1 count
±(2.5 to 5) V	2.5 mV	±(5 mV + 0.3% Rdg) or ± 1 count
±(5 to 10) V	5 mV	±(10 mV + 0.3% Rdg) or ± 1 count
±(10 to 20) V	10 mV	±(20 mV + 0.3% Rdg) or ± 1 count

* "Set" means of setting; "Rdg" means of reading

Driver/Sensor Characteristics. Four driver voltages (high A, B; low A, B; for up to 48 pins) and four sense voltages (similarly), where A and B correspond to pin-set assignments 1 and 2. Driver output resistance: 4 ohms typical, 10 ohms max. Driver slew rate: 50 V/ μ sec. Driver skew: $\pm(20 \text{ ns} + 5 \text{ ns/V} \times \text{del V})$, where "del V" means change of output voltage: $V_{IH} - V_{IL}$. Configurations: 16, 24, 32, 40, 48 pins.

ACCURACY OF DRIVER/SENSOR LEVELS

Parameter	Range	Resolution	Accuracy*
Drive Voltages	-2.5 to 16 V	5 mV	$\pm(50 \text{ mV} + 0.4\% \text{ Set})$
Sensed Voltages	-2.5 to 16 V	5 mV	$\pm(60 \text{ mV} + 0.3\% \text{ Set})$
Sensor Current, High	-(0 to 8) mA	2 μ A	$(-14 \text{ to } +30) \mu\text{A} \pm 0.5\% \text{ Set}$
Sensor Current, Low	+(0 to 24) mA	6 μ A	$(-39 \text{ to } +30) \mu\text{A} \pm 0.5\% \text{ Set}$

* "Set" means of setting.

Functional Testing Specifications. There are six driver/sensor functions: Drive high, drive low, sense high, sense low, sense tristate, and disconnect. Drive/sense levels: Two independent voltage sets, i.e., 2 drive sets and 2 sense sets, A and B, which are independently selectable on a pin-by-pin basis. Drive/sense timing: Resolution 62.5 ns, in two independent timing sets, independently selectable on pin-by-pin basis. Drive/sense pin can change direction (if defined as bidirectional) from one truth-table step to another.

TRUTH-TABLE MACRO COMMANDS

Name	Format	Definition and Comments
Jump (looping)	JNNN-CCC	Jump to step NNN the number of times specified by CCC.
Subroutine	SNNN	Jump to subroutine starting at step NNN.
Return from subroutine	R	Return to the step following the step from which the last subroutine call (SNNN) was made.
Wait or pause comment	WCCC	Program pause or stall at the current instruction for CCC number of cycles.
Program end statement	E	Last statement in the truth table, to signal "program end."
Truth table looping (jump to zero with error reporting disabled)	Z	Return to step zero and repeat program, continuously.*

* Used in debugging the truth table. The loop repeats at functional speed, allowing waveforms to be shown on the scope.

Truth-table macro-command protocol and nesting:

1. No nesting of waits within loops.
2. No nesting of jumps within loops.
3. No multiple waits within one step of each other.
4. One or more truth-table steps between end of one loop and beginning of next loop.
5. Subroutines can be nested up to 4 deep, i.e., no more than 4 subroutine calls before a return.

6. No wait command at step 0 of truth table.
7. Step 0 of the truth table cannot be the destination of a loop command.
8. Loops or waits can be placed inside a subroutine as long as rules 1, 2, 3, and 4 are not violated.
9. The first statement of a subroutine cannot be a loop or wait.
10. A loop or wait cannot be the destination of a subroutine return.
11. A loop or wait can be 4095 steps long, max, i.e., 4095 loops for the jump command and 4095 clock cycles for a wait command.

Cycle Timing.

The 1732 cycle time (i.e., the time per functional test step, also the length of a "sync clock" cycle) is set by two methods, which interact. Independent of the method used, the maximum frequency of operation cannot exceed 2 MHz. The first method is via a programmable clock generator and the second by a jumper on the DUT board. The programmable clock can be set (using the describe screen) to one of the following frequencies:

8 MHz	(125 ns)	1.6 MHz	(625 ns)
5.33 MHz	(187.5 ns)	1.454 MHz	(687.5 ns)
4.0 MHz	(250 ns)	1.33 MHz	(750 ns)
3.2 MHz	(312.5 ns)	1.23 MHz	(812.5 ns)
2.666 MHz	(375 ns)	1.14 MHz	(875 ns)
2.2 MHz	(437.5 ns)	1.06 MHz	(937.5 ns)
2.0 MHz	(500 ns)	1.00 MHz	(1000 ns)
1.7 MHz	(562.5 ns)		

Each of the above programmed frequencies is divided by a factor of 1, 2, 4, 8 or 16, depending on the jumper present on the DUT socket-adaptor board. In any event, the resultant frequency must not exceed 2 MHz. (Refer to "Conditions for 2-MHz Testing," below.)

Gate/Strobe Timing.

The 1732 hardware has the capability to shift the time at which data to/from the DUT is changed or strobed. Gate/strobe timing refers to the setting (gate) of data to DUT and the strobing (strobe) time of data from the DUT. There are two (2) sets of gate/strobes, A and B. Each set of gate/strobes can be independently programmed. Each driver/sensor pin can be individually assigned to either set, on the gate/strobe screen. The reason for the two gate/strobe sets is to allow edge triggered devices to be clocked at a precise time within a truth-table step. The setup and hold requirements of edge-triggered devices can be provided without the need for an added step before and after the clock transition. For clocked devices, this eliminates the need for many redundant truth-table steps. Some devices require a two-phase clock for proper operation. By assigning different gate/strobe sets to the two appropriate driver/sensor pins, a 2-phase clock can be provided. In general, the strobe time

must occur after the gate time. This requirement results from characteristics of internal latches in the driver/sensor chip. Certain timing requirements must be considered when setting the cycle and gate/strobe times. For example, if large voltage swings are required, gate/strobe timing must be chosen to allow for the driver's finite slew rate (dV/dt), which is about $50\text{ V}/\mu\text{s}$.

The gate marker position can be set to assign the desired timing of data driven to the DUT. The gate can be set in increments of 62.5 ns (one "tick"). The gate should be set at least 315 ns after the beginning of the DUT sync cycle and at least 2 ticks before the end of the cycle. (Thus there is an interval after the gate for the strobe to be set before the end of the cycle.)

The strobe setting is used to determine when the data from the DUT is latched into the driver/sensor circuit (a custom chip). In general, the strobe is placed as late in the cycle as possible. The position of the strobe can be changed in 62.5-ns increments (ticks), using the gate/strobe screen. The strobe cannot be placed any earlier than one tick (i.e., 62.5 ns) after the gate position. Also, the strobe cannot be placed any later than 1 tick (62.5 ns) before the end of the sync clock cycle.

The gate/strobe screen displays graphically the timing of gates and strobes, in relation to one cycle of the sync clock, and lists the pins in each gate/strobe set (A, B).

DUT Signal Timing.

The interval between gate and strobe must be long enough to include the following events in sequence.

- T1. (50 ns) for driver to respond.
- T2. (50 ns , if applicable) for conversion from sensor to driver (if the pin being driven was previously sensed or was tristate and now being driven).
- T3. ($20 \times E\text{ ns}$) for driven pin to slew from one logic level to the other. E is the full nominal voltage swing for logic state change.
- T4. (device dependent) for DUT to respond, including propagation time in DUT and time for output pin to slew to final logic level.
- T5. ($50 + 3 \times E\text{ ns}$) for sensor to be set up. E is defined as before.

For example, if the driven pin was previously sensed, then $T2 = 50$. If $E = 15\text{ V}$, and $T4 = 75\text{ ns}$, then the gate-to-strobe interval must be at least:

$$50 + 50 + 20 \times 15 + 75 + 50 + 3 \times 15 = 570\text{ ns}.$$

This is over 9 ticks, so 10 or more ticks are required between gate and strobe in this example.

IEEE-488 Bus, Serial, and Handler Interfaces

IEEE-488 Bus (middle connector on rear panel). All front panel functions are programmable from the bus. The following functions, per IEEE-488, have been implemented:

- AH1 Acceptor handshake (listener)
- SH1 Source handshake (talker)
- TS Talker with normal and talk-only modes (for systems without a controller), switch selectable on rear panel.

L4 Listener

- SR1 Service request (to request service when measurement is complete and the instrument is not addressed to talk).
- RL2 Remote/local (no local lockout, no return-to-local switch).
- PP0 No parallel poll
- DC1 Device clear implemented
- DT1 Device trigger (to start a measurement)
- C0 No controller functions
- E1 Open collector driver

Serial Interface: internally switch selectable between "RS232 PORT I" and "20-mA PORT I" connectors on rear panel. For the 20-milliampere current loop, the following inputs and outputs: +in, -in, +out, -out. Open-circuit output voltage of any external current source must be limited to 12 V .

Handler Connection (connector on rear panel with option)

- 1. Outputs, Active Low, $-0.2\text{ V} < VL < +0.7\text{ V}$, $+2.4\text{ V} < VH < +5.5\text{ V}$. Sorting data (7 lines): Bin 1 through bin 5, PASS, FAIL, TEST DONE (1 line): indicates end of test and bin no. is valid.
- 2. Input, Active Low, $-0.2\text{ V} < VL < +0.7\text{ V}$, $+2.4\text{ V} < VH < +5.5\text{ V}$. Start (1 line): initiates new measurement.

Input Power Requirements. Frequency: $48\text{ to }63\text{ Hz}$. Voltage: (RMS) $87\text{ to }127$, $174\text{ to }250$. Current: (RMS) 10 amp max .

Environment. Operating: $0\text{ to }40\text{ degrees C}$. Storage: $-40\text{ to }55\text{ degrees C}$. Humidity: 80% maximum @ 35 degrees C .

Physical Configuration

Program Display Unit: Height $12.8''$ (32.6 cm), width $19''$ (48.25 cm), depth $25''$ (63.5 cm), weight 67 lbs (30.4 kg).

Pin Electronics Module: Height $9.0''$ (22.9 cm), width $19.9''$ (50.6 cm), depth $11.5''$ (29.2 cm), weight 29 lbs (13.2 kg).

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Service Manual, Volume 2, Diagrams	1732-1806
Service Diagnostics Manual (with service kit)	1732-0120
Program-Library Manuals	1732-01XX or 1732-05XX or 1732-18XX
Index to Device Programs	1732-0124
Handler Interface Manual	1732-1819

Introduction—Section 1

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1.1 PURPOSE

(Figure 1-1)

The 1732 Digital IC Test System is a microprocessor controlled bench-top tester suited to special-purpose measurements as well as routine inspections, with provisions for convenient changeover from one purpose to another. For routine uses, the test programs, which include details of testing and handling of results, are entered automatically from a magnetic tape cartridge. Such operational convenience for sophisticated measurements means that a prime use of this system is for incoming inspection by the integrated-circuit user. Other outstanding applications are for wafer-probe and package-test inspections by the semiconductor device manufacturer.

For non-routine uses, the operator participates in a dialog with the system, via keyboard and display screen, to make the desired changes in program, conditions, limits, and operating modes.

Test programs are available on tape from GenRad or can be generated manually. One particularly convenient method of writing new programs makes use of the system's capability to "learn" the functional (digital logic) test details from a known good device.

Adaptability to particular package style and pin configuration of the device under test (DUT) is provided by a selection of plug-in socket adaptors, each designed, for example, to receive a 14-, 16-, 20- ... or 48-pin DIL package. Because the adaptation to IC function is in software and the test programs, a few socket adaptors can handle hundreds of DUT types.

A significant level of adaptability is also provided by the modular construction of this system. (Inquire from GenRad about availability of new features.)

Convenience and efficiency of program changes are enhanced in several ways. The magnetic tape storage enables recall of routine test programs automatically and provides a convenient vehicle for bringing you prepared programs from GenRad. The language and format of the operator/system dialog for program changes are clear, concise, and easy to understand. Parameters are identified with the standard symbols that are found in engineering data sheets of representative DUTs. Prompting messages and data tables on the display screen show the operator's alternatives and verify inputs. The dialog is automatically tailored to certain particulars, such as the pin count of the DUT that is to be measured.

Simple and complex test systems can be set up using this digital IC tester. Perhaps the simplest system is the combination with a parts handler, providing automatic con-

nection to DUTs and sorting into five GO bins and one NO-GO bin. For suitable interface kits or complete installation, refer to paragraph 5.2. Another system is the combination with a printer to provide test results on paper. More complex systems are easy to build, with interconnections via the IEEE-488 bus, providing such additional capabilities as mass storage of test results, statistical analyses of results, automatic (fast) access to more test programs, coordination of environmental control with functional testing, and special-purpose measurement with process control or calculations for manufacturing or laboratory needs.

1.2 GENERAL DESCRIPTION

1.2.1 Physical Description

The test system consists of two benchtop units. The control and display module has a cathode-ray-tube display screen and a magnetic-tape-transport slot on the front (illustration in paragraph 1.3). A keyboard, with 4 indicator lights, a start button, and 36 keys, is located on a ledge below the display screen. Interface to the device under test is provided at a cable-connected pin-electronics module that can be on the bench or mounted on a parts handler.

The sturdy metal cabinets are durably finished, in keeping with the reliable controls and other long-life circuitry. Glass-epoxy circuit boards interconnect and support high-quality components to assure years of dependable performance.

Adaptability to any common ac power line is assured by the removable power cord and the convenient line-voltage switch. Safety is enhanced by the fused, isolating power transformer and the 3-wire connection. The power switch breaks both connections to the power line.

1.2.2 Adaptation of DUT

This test system is adaptable to measure hundreds of types of digital ICs, and most of the adaptation is provided by means of the software. A relatively simple socket adaptor is needed to match the pin configuration of the DUT and provide a few universal circuit connections and passive parts (such as decoupling capacitors). For certain special applications, such as testing LSI devices, the socket adaptor may include active devices.

For routine measurements, the user needs a socket adaptor, generally one for each socket type. In most cases, each socket adaptor can be used for many DUT types having the same number of pins.

To obtain any particular socket adaptor, order a socket adaptor kit (which contains parts, except sockets, for four

adaptors), make the few appropriate jumper connections, and mount a socket that fits the particular DUT. A selection of recommended sockets is tabulated with other accessories in para 1.4. Each basic socket adaptor matches any of several types of ICs and can be tailored to match a specific configuration. The assembly procedure is a simple task for an electronic technician or assembler accustomed to working with circuit boards. (Any customer who does not have the technical resources to do this tailoring should consult with GenRad about buying ready-to-use socket adaptors.)

Section 4 of this manual contains helpful information and examples for you in writing test programs for this system. An index to prerecorded test program tapes is also available from GenRad.

1.2.3 Classification of Tests

The testing capabilities of the system are classified in descending stages arranged from broadest to narrowest category as follows.

1. The "system" capability, including the software and hardware necessary to execute a test program.

2. A "class" of tests is identified with a class of DUT, such as a TTL, CMOS, ECL, processors, etc.

3. A "test program" (which contains one or up to six test "groups"—see below) includes all the instructions to run a test; the "name" assigned to the test program; pin assignments; number of test groups; voltage and current

parameters; digital-logic stimulus/response "truth table"; and system run, display, and output mode details.

4. A parameter "group" of voltage and current parameters and relay-control specifications, applicable to one complete performance evaluation (a test "group") from which two "pass/fail" results can be obtained (parametric and functional). Bin assignments are made on the basis of group pass/fail results.

5. A "type" of tests. There are four: continuity (that checks for any open-circuited pin), Kelvin (verification that drive and sense lines are joined at each pin), parametric (analog checks of the voltage or current at specified pins, under specified conditions), and functional. A "truth table" tabulates the details of a functional test, step by step, in terms of digital logic, the stimulus patterns to apply at input pins, and response patterns that should result at the output pins.

6. A "step" (defined in the truth table, identified by a step number) tabulates the conditions for all input and output pins: inputs high, low, or tri-state; outputs high, low, or "don't care", etc. If any one of the outputs is not confirmed when the step is executed, the functional test fails.

1.3 CONTROLS AND OTHER OPERATIONAL FEATURES

Figure 1-1 shows the controls, indicators, and other points of operational importance at the front of the test system. Table 1-1 identifies them with descriptions and functions. Similarly, Figure 1-2 shows the controls and connectors at the rear; Table 1-2 identifies them.

Table 1-1
FRONT CONTROLS, INDICATORS, AND OPERATIONAL FEATURES
(Refer to Figure 1-1.)

Ref	Name	Description	Function
1	Control module	Main unit of system. Also called "control and display module" or "program/display unit."	Contains central processor, memories, input and output circuits, main power supply, keyboard with indicators, tape handler, and display screen.
2	Pin electronics module	Socket adaptor station. Sometimes called the "test box."	Interconnects the system with the socket adaptor and DUT. Provides stimulus and response electronic circuitry, physically near to the DUT. Cable connection from control module allows easy attachment to a handler.
3	DUT socket position	Pair of zero-insertion-force connectors with locking handle.	Interface between the pin electronics module and the socket adaptor which receives the DUT.
4	Display screen	Alphanumeric display, 22 lines of 32 (or 64) characters on a 130 mm (5 in.) cathode-ray-tube face.	Multipurpose display of operating guidelines, CPU-operator dialog, test modes, conditions, limits, logical truth tables, results, etc.
5	Tape cartridge receptacle	Slot, approx 80 × 13 mm (3.2 × 0.5 in.)	Receives tape cartridge for input of operating system software and for storage and retrieval of test programs, results, etc.
6	Eject button	Mechanical pushbutton	To eject the tape cartridge.
7	Line power switch	Rocker pushbutton switch, labeled POWER, ON OFF.	To switch the system's primary power on and off.
8	START	Pushbutton switch, labeled START and ABORT.	Initiates testing of the DUT (regardless of the screen being displayed), but if a test is under way, aborts the test.
9	PASS/FAIL	Green and red lights labeled PASS and FAIL.	Indicates the basic summary test result, for the test group. However, if SYSTEM RUN MODE (item 13) is set to TEST CONTINUOUSLY, the indication is only a brief flash, easily overlooked.
10	OPEN	Red Light with label.	Indicates a continuity failure in the DUT, faulty connection to it, or DUT-power-supply shutdown due to excessive current.

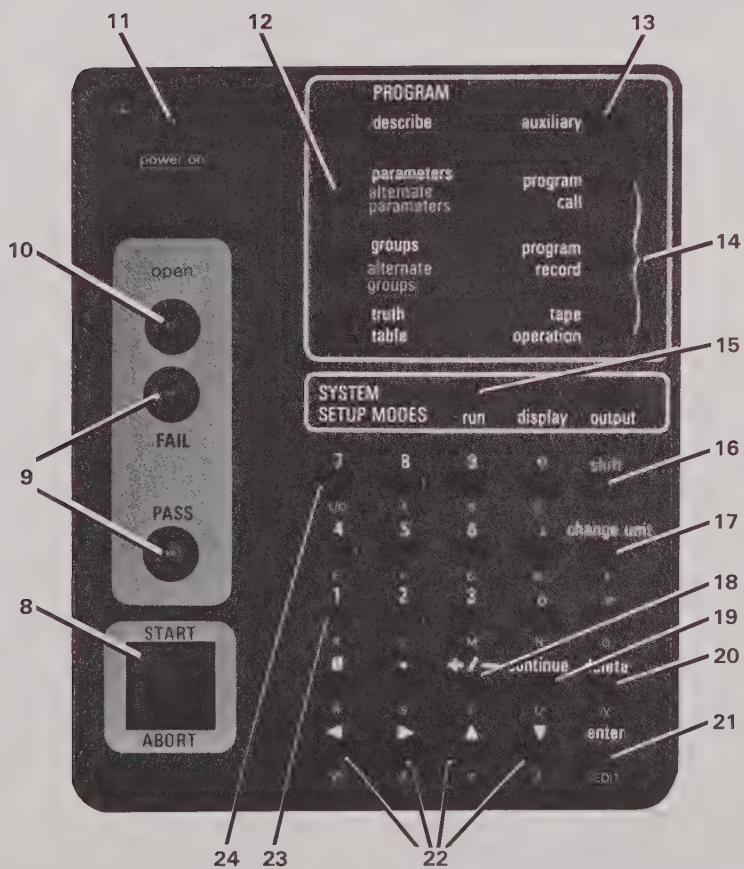
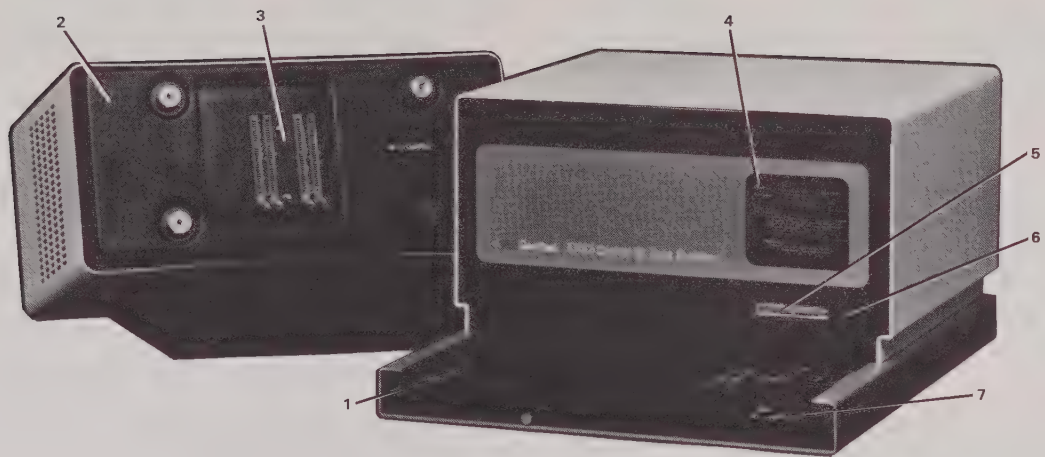


Figure 1-1. Front view of the 1732 Digital IC Test System, showing controls, displays, and other operational features. Upper, overall view; lower, keyboard details.

Table 1-1 Continued
FRONT CONTROLS, INDICATORS, AND OPERATIONAL FEATURES
(Refer to Figure 1-1.)

Ref	Name	Description	Function
11	POWER ON	Red light with label.	Indicates that power is applied to the system.
12	PROGRAM	Set of 4 keys, as follows:	Each key brings up a different screen for program creation or modification. Display shows corresponding information read from program recalled from tape, previous selections, default choices, or blanks; and indicates where the operator can make selections by inserting or changing key words and numbers. (Use cursor control, [DELETE], character, [CHANGE UNIT], [EDIT], [I/O], [+/-], and [ENTER] keys.)
	[DESCRIBE]	Key	DESCRIBE screen appears, with 3 parts as follows. 1. Heading includes program name, a line for user's comment, number of pins in the socket, and number of test groups in this test program. 2. Left margin includes main clock frequency and selection of sync. 3. Table of pin assignments: pin number, ID (i.e., function, such as input or output), and pin set (1 or 2, not applicable to some pins, such as ground, don't care, dc voltage, or clock). ID code is explained in left margin.
	[PARAMETERS]	Key labeled PARAMETERS and ALTERNATE PARAMETERS	PARAMETERS (test) GROUP 1 screen appears (could be called by pressing [GROUPS] [1] keys), with 5 parts as follows. 1. Heading, with name of program automatically displayed. 2. STEP number, specifies step in truth table at which these current limits are to be verified. 3. Power-supply parameters table for two positive voltages V1 & V2, one negative voltage V3, and the current limit (for "pass") as well as a maximum (above which testing will be aborted) corresponding to each of the 3 power supplies. 4. Pin-set-1 table of voltage and current specifications for logic low and high states. For parametric tests, the format is: "Limit @ test condition;" for functional tests, "condition" only. 5. Pin-set-2 table, same, but applicable to the 2nd set of pins. [SHIFT] [PARAMETERS] sequence brings up the ALTER-NATE PARAMETERS screen, similar to the above but with step-number range (for parametric tests only) and a relay specification table (up to 4 circuits, selectable for parametric and for functional tests). Certain of the limits specified in the PARAMETERS screen can be respecified on this screen, thus creating limit pairs (upper and lower limits).
	[GROUPS]	Key labeled GROUPS and ALTER-NATE GROUPS.	If you press [GROUPS] and [2], PARAMETERS (test) GROUP 2 screen appears (similarly for other test groups, up to 6). Parameters appear automatically as previously defined for this group or, if this group not defined, like the present version of group 1. [SHIFT] [GROUPS] [2] sequence brings up the group-2 ALTERNATE PARAMETERS screen. (See above.)
	[TRUTH TABLE]	Key	TRUTH TABLE Screen appears with program name on first line and pin IDs automatically indicated (as specified on describe screen). Each column is headed by pin number, each row by a functional test step number. Truth table can be far longer than the portion displayed and can be generated by use of special editing features, including the possibility of deriving functional data from a known good device.

Table 1-1 Continued
FRONT CONTROLS, INDICATORS, AND OPERATIONAL FEATURES
(Refer to Figure 1-1.)

Ref	Name	Description	Function
13	[AUXILIARY]	Key	Calls up auxiliary screen which displays a "menu" of special-purpose screens, explained below. Use cursor control keys to select your choice and press [ENTER] to call that screen. • GATE/STROBE screen, permits specification of 2 drive and 2 sense timing marks within the DUT measurement clock cycle. • SERIAL INTERFACE screen, permits selection of interface control characters as required for a printer or other peripheral device. • TEST STATISTICS screen, displays totals of tests completed, passed, failed, as well as bin totals, real-time calendar and clock, etc. • RESULTS screen, displays results of latest test (format determined in test program via display-mode screen). • DEBUG screen (primarily for GenRad use).
14	Tape Control	Set of 3 keys as follows:	
	[PROGRAM CALL]	Key	Calls up the PROGRAM CALL Screen. Verify or type in the desired test program name. Press [ENTER] to load the program into memory. Subsequently, the program tape cartridge can be replaced by another (results) tape cartridge before the test is started.
	[PROGRAM RECORD]	Key	Calls up PROGRAM RECORD screen to help you store on tape the test program now in system memory. Verify or enter the desired tape program name (which must be different from any already on the tape), depress [ENTER], write a comment, if desired, then press [ENTER] again to trigger the storage action.
	[TAPE OPERATION]	Key	Calls up the TAPE OPERATION screen. Here you can request a directory listing of a tape or format or compress it, can delete or restore a file (i.e., test program or results), and can retrieve a recorded result, record one that is in system memory, or transfer the information that is on tape, via the IEEE bus.
15	SYSTEM SETUP MODES	Set of 3 keys, as follows:	
	[RUN]	Key	Calls up the SYSTEM RUN MODE screen. Operator can further define a test program by positioning the cursor in the 4-part display: 1. Test sequence. Three subgroups (continuity, functional, parametric) can be ordered in any sequence. 2. Bin assignments, expressed as a table of pass/fail results from both functional and parametric tests in all groups used. 3. Several choices related to stopping on failure, continuation of testing, single-group testing etc. 4. Whether to lock the keyboard.
	[DISPLAY]	Key	Calls up the SYSTEM DISPLAY MODE screen. Enables selection of test-result display mode (CRT display only) to be written into the test program: either pass/fail/bin, result summary, or parametric-subgroup results in detail for certain specified pins.
	[OUTPUT]	Key	Calls up the SYSTEM OUTPUT MODE screen. Enables selection among these test-result dependent modes: 1. Whether to enable sending replicas of certain test-program screens and/or results out on the IEEE-488 bus and/or the TTY/CRT connector (20-mA current loop, typically to a printer). 2. Specifications of results format: pass/fail/bin, summary, and/or complete parametric subgroup; whether to suppress results that "pass"; and which test groups to include. 3. Instructions for automatic restart of tests in conjunction with a handler (disable, continue endlessly, or continue until a specified number [up to 99] or consecutive DUTs have failed).

Table 1-1 Continued
FRONT CONTROLS, INDICATORS, AND OPERATIONAL FEATURES
(Refer to Figure 1-1.)

Ref	Name	Description	Function
16	[SHIFT]	Key	Alters the input from each alphanumeric key and certain others with yellow legends in the same block of 25 keys, and certain PROGRAM keys. Press and release the [SHIFT] key before typing each character (or calling each function) shown in color on the keyboard <i>below</i> each key. These characters include most of the alphabet. Press [SHIFT] again before each such entry; do not hold [SHIFT] key down. Make deliberate keystrokes (not too fast).
17	[CHANGE UNIT]	Key	Changes from one to the next of a set of predetermined choices, associated with cursor, as follows. Changes the automatically displayed unit of measure by a factor normally associated with the measurement. In an "option" field, toggles the cursor triangle to appear (select) or disappear (reject). In a "scroll" field, increments to next item in a multiple-choice set; for example, increments the clock frequency or "sync" to next available value or changes "IS locked" to "NOT locked" and vice versa. (To cycle thru multiple choices in inverse order, type [SHIFT] [CHANGE UNIT].)
18	[+/-]	Sign key.	Changes the sign of the number indicated by cursor. Inserts a minus sign into a blank field.
19	[CONTINUE]	Key	Keyboard command to continue testing from a pause.
20	[DELETE]	Key	To delete data in the cursor field (indicated by bright background and reverse-video characters).
21	[ENTER] or [EDIT]	Key labeled ENTER and EDIT	[ENTER] To store in memory information specified by the cursor. Also used to reposition the cursor from the present field to the next. The cursor-field action is identical to that of the [right-arrow] key. Also used to initiate actions, such as tape transport for program call or record or the sending of program data out via the IEEE-488 bus. [SHIFT] [EDIT] sequence enables a special mode (available when the TRUTH TABLE screen is displayed) in which certain characters or strings typed at the keyboard are interpreted as commands. Useful in modifying or generating complex functional-test tables.
22	Cursor control keys	Set of 4 keys labeled: 	To position the cursor on the screen (left, right, up, down, respectively). [Up-arrow] and [down-arrow] keys move the cursor within a field; [left-arrow] and [right-arrow] keys move the cursor field (if there is more than one on the screen). For details, refer to para 3.3.
23	Character keys	Keys with alphanumeric labels or punctuation.	Used in conjunction with the [SHIFT] key to enter characters on the screen, for writing test programs, names, numbers, and other operator inputs. Each key enters the character shown above it (in white) unless [SHIFT] was pressed and released before, in which case the letter shown below (in color) is entered. The character will automatically repeat at a rapid rate if key is depressed for more than one second.
24	[I/O]	Key	[SHIFT] [I/O] sequence is used while the TRUTH TABLE screen is displayed, to toggle the assignment of a bidirectional or tristate pin from input to output, and vice versa.

Table 1-2
REAR CONTROLS AND CONNECTORS

(Refer to Figure 1-2.)

Ref	Name	Description	Function
1	POWER J22	22-pin connector.	Power-supply connections, via cable supplied, to pin electronics module.
2	Ground connector	No. 6-32 stud.	Safety ground, which must be directly connected to earth ground, to supplement the "third" wire of power cord.
3	Power connector	Safety shrouded 3-wire plug conforming to International Electrotechnical Commission 320.	AC power input. Use the appropriate power cord, with Belden SPH 386 socket or equivalent. The GenRad 4200-2850 power cord (supplied) is rated for 125 V.
4	Fuse	Fuse in extraction post holder, labeled F1 10A 250 V. SLOW BLOW	Short circuit protection. Use Bussman Type MDL or equivalent, 10 A, 250 V rating.
5	VOLTAGE SELECTOR	Two-position slide switch.	Adapts power supply to line-voltage ranges, as indicated (90-125, 180-250 V ac). Be sure to set correctly before connecting power cord.!
6	CRT BRIGHTNESS CONTROL	Screwdriver-adjusted potentiometer.	Adjustment of display brightness (clockwise rotation for brighter screen).
7	FOOTSWITCH connector	3-pin connector.	Connection to foot switch for auxiliary "start" control.
8	20mA PORT I/CRT	Socket, 24-pin; receives Amphenol "Microribbon" plug, P/N 57-30240.	Data output (test results) to printer or other serial terminal and to auxiliary display screen. (See item 14.)
9	HANDLER CONTROL	Socket, 24-pin, receives Amphenol "Microribbon" plug P/N 57-30240 or equivalent.	Connection to component handler. Conveys handler ready, PASS/FAIL, and sorting (bin) information.
10	IEEE-488 INTERFACE	Socket, 24-pin, receives IEEE-488 interface cable.	Input/output connections according to IEEE Std. 488-1978. Functions: complete remote control (all keys), output of test results as specified by the test program or by keyboard entry (on SYSTEM OUTPUT MODE screen).
11	TAPE	36-pin connector.	Connection to tape drive unit (for service).
12	DIGITAL CONTROL BUS (B)	50-pin connector.	Connection, via cable supplied, to pin electronics module (connector B). Connectors "A" are keyed differently from "B".
13	DIGITAL CONTROL BUS (A)	50-pin connector.	Connection, via cable supplied, to pin electronics module (connector A).
14	RS232 PORT I	24-pin connector.	EIA standard RS232 interface. Internal switch selects either item 8 or item 14 for port I.
15	LINK RS 232 PORT II	Not provided on 1732-974X.	

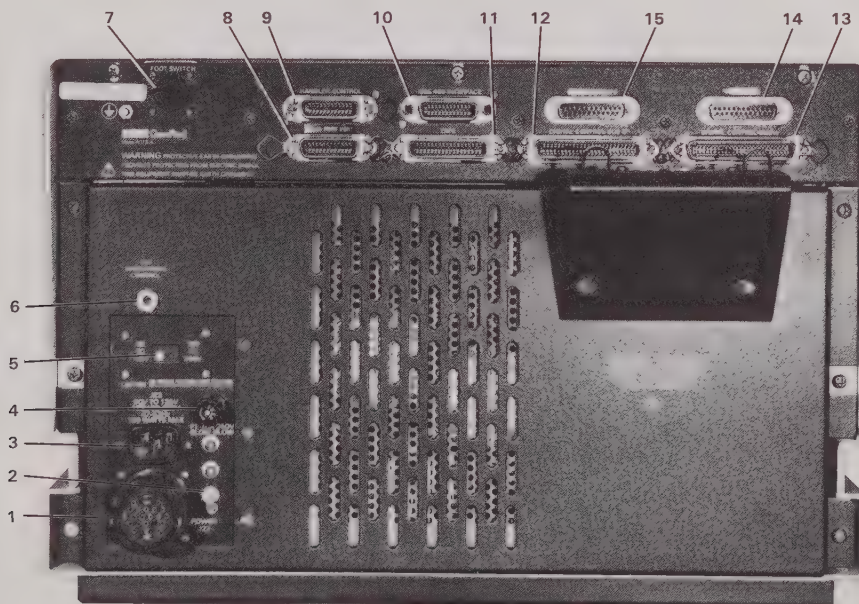


Figure 1-2. Rear view, showing connectors, fuses, and controls.

1.4 ACCESSORIES

1.4.1 List

The accessories are listed in two tables. Table 1-3 indicates those items which are supplied with the system and Table 1-4 lists those which are available only on order. GenRad part numbers in which the 5th digit (just after the hyphen) is "9" designate items that are commonly purchased by our customers.

1.4.2 Socket Adaptors

A suitable socket adaptor provides the appropriate interface between the DUT and the test system. (The device is plugged into the socket adaptor, which was previously

plugged into the pin electronics module and locked there.) A ready-to-use socket adaptor is supplied, and others can be assembled using kits obtained from GenRad. The socket adaptor kits and sockets (and a few ready-to-use special-purpose socket adaptors) are listed in the tables of accessories.

1.4.3 Program Library Tapes

Prerecorded test-program tape cartridges are available from GenRad, for many standard types of digital ICs. For a listing, refer to the program-library index.

Table 1-3
ACCESSORIES SUPPLIED WITH SYSTEM

Quantity	Description	Part Number
1	Power cord 198 cm (6.5 ft) long, 3-wire AWG No. 14, with molded connector bodies. One end, fitted with a Belden SPH-386 socket, fits the instrument; the other end conforms to ANSI standard C73.11-1966 (125 V max). U.L. listing.	4200-2850*
1	Intrasystem power cable, 1.2 m (48 in.) long, with round 22-pin connectors.	1732-0320
1	Intrasystem digital control cable, 1.24 m (49 in.) long, with 50-pin connectors.	1732-0300
1	Intrasystem digital control cable (similar to 1732-0300 but not interchangeable).	1732-0310
2	Operating system tape cartridge.	1732-0401
1	Conversion adaptor board for using OVP module and standard socket adaptors with Kelvin systems.	1732-4778
1	Device program tape cartridge (containing test programs for 74LS161A).	1732-0402
1	Ready-to-use 16-pin socket adaptor (suitable for 74LS161A synchronous 4-bit counter, a sample of which is included).	1732-4026
2	Blank tape cartridge (for storage of additional test programs or results).	1765-3020
1	Socket kit, includes 4-lever-operated zero-insertion-force sockets (for 14- and 16-pin DUTs) and a receptacle for each.	1732-3920
2	Holder for 12 tape cartridges (matches binder).	5301-6010
1	Instruction manual (includes Device Program Index, 1732-0124)	1732-0104
1	Service manual set (Vol 1, Vol 2)	1732-1800
1 set	1732 System OVP tapes A, B, B1, C, D, E, for use with the special OVP socket adaptors listed on the next 4 lines.	1732-1505
1	Driver-cross socket adaptor	1732-4061
1	Pin-ground socket adaptor	1732-4062
1	Functions socket adaptor	1732-4063
1	Pin-leak socket adaptor	1732-4064

* Recommended replacement: Belden No. 17504.

Table 1-4
ACCESSORIES AVAILABLE FROM GenRad

Description	Part Number
Auxiliary display screen (9-inch CRT) with cable.	1732-9620
Drive/sense option (plug-in board serves 8 additional pins).	1732-9610
Manual handler (for convenient binning of DIP devices).	1732-9710
Foot (Start) switch and cable.	1732-9681
Same, for older systems without FOOTSWITCH connector.	1732-9680
Prerecorded test program cartridges. (Refer to program-library index.)	----
Socket adaptor kit (no sockets 4 adaptors) for non-TTL devices	1732-9615
Socket adaptor kit (no sockets 2 adaptors) for TTL devices	1732-9692
Sockets (Lever-operated zero-insertion-force type), with receptacle for each (except the last), as follows*	
14-pin, Textool 214-3339-00-0602 and 214-3592-00-0605	1732-9670
16-pin, Textool 216-3340-00-0602 and 216-3593-00-0605	1732-9671
18-pin, Textool 218-3341-00-0602 and 218-3594-00-0605	1732-9672
20-pin, Textool 220-3342-00-0602 and 220-3595-00-0605	1732-9673
22-pin, Textool 222-3343-00-0602 and 222-3596-00-0605	1732-9674
24-pin, Textool 224-3344-00-0602 and 224-3597-00-0605	1732-9675
28-pin, Textool 228-3345-00-0602 and 228-3598-00-0605	1732-9676
40-pin, Textool 240-3346-00-0602 and 240-3599-00-0605	1732-9677
42-pin, Textool 242-4262-00-0602 and 242-4282-00-0602	1732-9678
48-pin, Textool 248-4775-00-0602 and 248-5195-00-0602	1732-9679
Socket adaptor (assembled) for 16-pin static RAMs.	1732-9616
Socket adaptor (assembled) for 16-pin dynamic RAMs.	1732-9617
Set of 4 blank tape cartridges (for storage of additional test programs or results)	1731-9670
Holder for 12 tape cartridges (matches binder).	1731-9608
Handler interface kits (see paragraph 5.2)	(Inquire)
Printers and cables are available, configured for RS232 or 20-mA loop, for 110 V or 220 V	(Inquire)
Service contracts are available	(Inquire)
Service kit (diagnostic tapes and manual, AVP adaptor, extender boards)	1732-9640
1731/32 service spares kit (I/O boards, keyboard, tape drive and display kits)	1732-9693
1732 service spares kit (distribution, control boards, power supply)	1732-9696
Spare parametric board	1732-9686
Spare dynamic RAM board (64 K)	1732-9694
Spare CPU board	1732-9695
Spare drive/sense board	1732-9610
Automatic-handler interfaces	(Inquire)
Video tape, introduction and operation (1/2 in. VHS)	1732-9625
Same (3/4 in. U-matic)	1732-9626

* Obtainable from Textool Products, Inc., 1410 Pioneer Dr, Irving, TX 75061.

Installation – Section 2

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2.1 UNPACKING AND INSPECTION

If the shipping carton is damaged, ask that the carrier's agent be present when the instrument is unpacked. Inspect the instrument for damage (scratches, dents, broken parts, etc). If the instrument is damaged or fails to meet specifications, notify the carrier and the nearest GenRad field office. (See list at back of this manual.) Retain the shipping carton and the padding material for the carrier's inspection.

2.2 BASIC SYSTEM SETUP

Figures 2-1, 2-2

2.2.1 Environmental Requirements

The overall environmental specifications for the 1732 Digital IC Test System are as follows.

- Operating Temperature: 0 to 40° C
- Non-operating Temperature: -40 to 55° C
- Humidity: 80% @ 35° C*

CAUTION

KEEP VENTS FREE. (See below.) Do not operate if damp. If equipment is cold, warm moist air can cause condensation. Allow 3 hours drying time in the work area before connecting power.

Be sure all vents are free. Allow no obstacles closer than 25 cm (10 in.) to the vents on the pin electronics module. If air does not flow through that module when power is switched on (fan may be inoperative), switch power off and obtain service.

2.2.2 Setup and Connections

The instrument is supplied in a bench configuration, i.e., in two cabinets with resilient feet for placement on a table. The pin electronics module is provided with a tilting pedestal and connects to the control/display module via 120-cm (four foot) cables so that it can be placed on the same table or mounted directly on a nearby parts handler. The overall dimensions are given in Figure 2-1. Make the basic setup as follows.

a. Set the two modules about a foot apart (or place the pin electronics module on top of the control module), making certain that the ventilation openings are completely free of obstruction.

b. Connect the program-display unit (PDU) to the the pin electronics module (PEM), using the three intrasystem cables, as follows. Notice that the digital control cables

are keyed. Do NOT attempt to force incorrectly mated connectors together.

1. Power cable 1732-0320, from PDU POWER J22 to PEM J401 POWER SUPPLY.
2. Digital control cable 1732-0300, between the two connectors labeled DIGITAL CONTROL BUS A.
3. Digital control cable 1732-0310, between the two connectors labeled DIGITAL CONTROL BUS B.

Do not interchange or cross the digital control cables.

c. Secure the power cable by turning the locking collar supplied in each connector pair. Secure each digital control cable by snapping the wire retainers into the slots provided and also by use of the brackets and dual clamps provided with the system.

2.3 POWER-LINE CONNECTION

Figure 2-3

Voltage. The power transformer primary windings can be switched, by means of the line voltage switch on the rear panel, to accommodate ac line voltages, as labeled, at a frequency of 50 or 60 Hz, nominal. Set this switch to match the measured voltage of your power line.

CAUTION

Never change switch setting with voltage applied to the system.

The instrument is fitted with a power connector that is in conformance with the International Electrotechnical Commission publication 320. The three flat contacts are surrounded by a cylindrical plastic shroud that reduces the possibility of electrical shock whenever the power cord is being unplugged from the instrument. In addition, the center ground pin is longer, which means that it mates first and disconnects last, for user protection. This panel connector is a standard three-pin grounding-type receptacle, the design of which has been accepted world wide for electronic instrumentation. The connector is rated for 250 V at 6 A. The receptacle accepts power cords fitted with the Belden type SPH-386 connector.

The associated power cord for use with that receptacle, for line voltages up to 125 V, is GenRad part no. 4200-2850. It is a 198-cm (6.5-ft), 3-wire, 14-gauge cable with connector bodies molded integrally with the jacket. The connector at the power-line end is a design that conforms to the "Standard for Grounding Type Attachment Plug Caps and Recep-

* Except where noted for low input-current measurement.

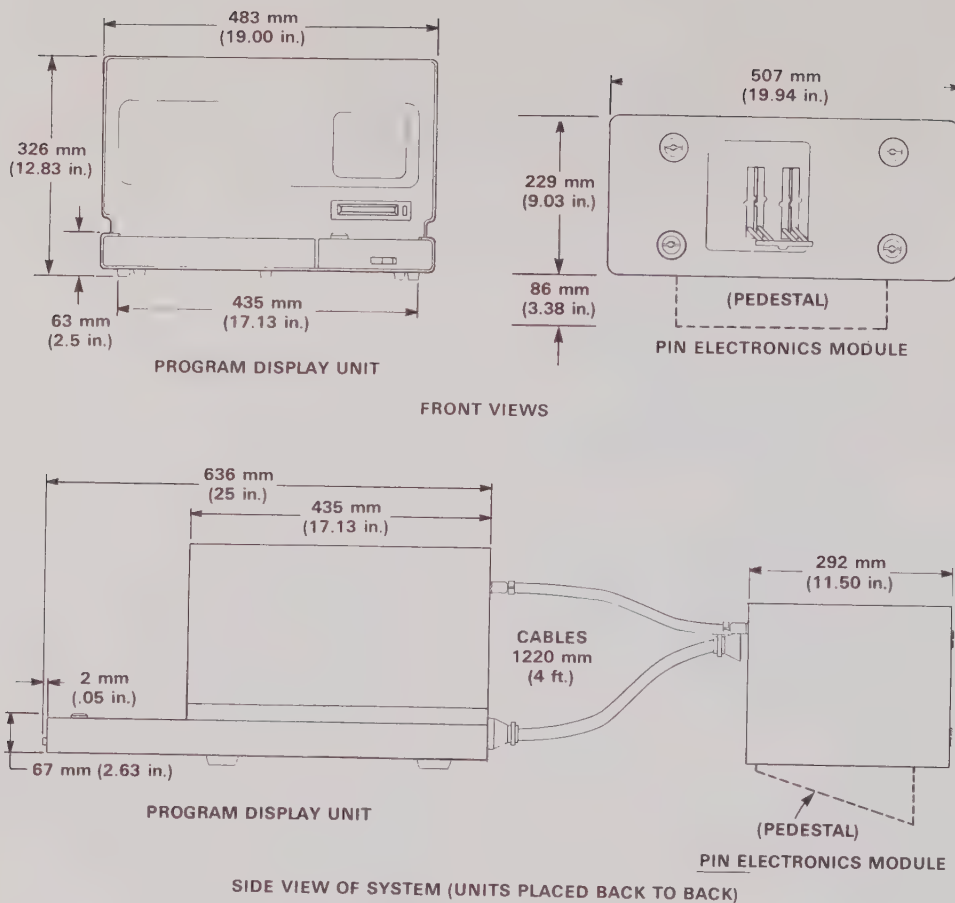


Figure 2-1. Dimensions.

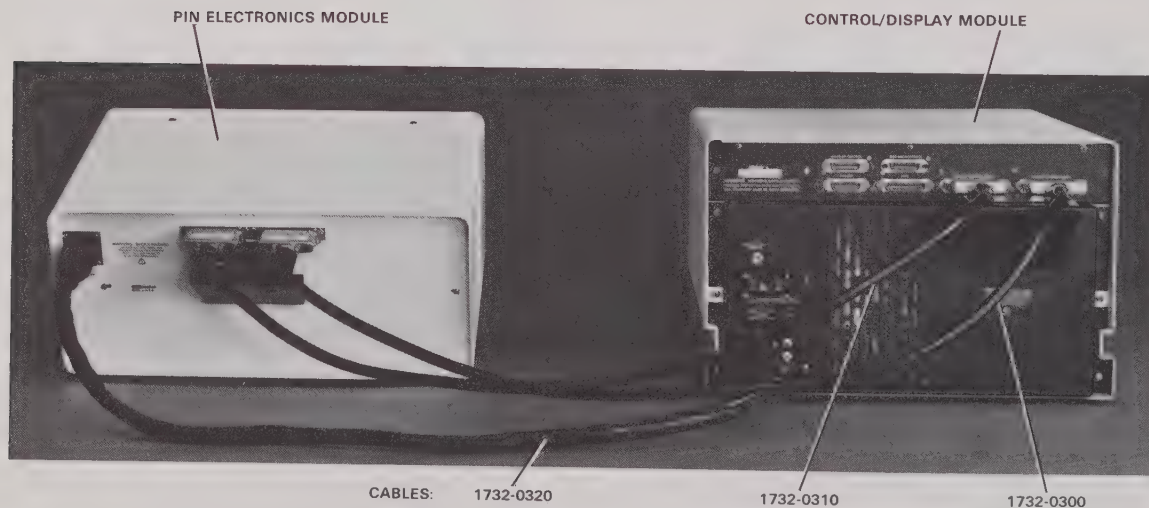


Figure 2-2. Basic system setup, showing cables at rear.

tacles", ANSI C73.11-1966, which specifies limits of 125 V and 15 A. This power cord is listed by Underwriters Laboratories, Inc., for 125 V, 15 A.

If your power line voltage is in the higher range (up to 250 V), be sure to use a power cord that is approved for 250

V. The end that connects to the test system should have a connector of the type that is on the power cord supplied; the other end, an approved connector to mate with your standard receptacle. A typical configuration for a 250-V, 15-A plug is illustrated in the figure.

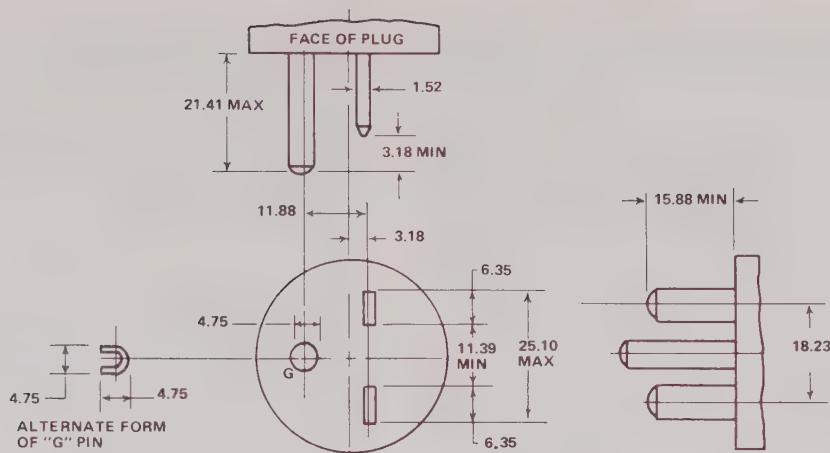


Figure 2-3. Configuration of a 250-V, 15-A plug. Dimensions are in mm.

If a fuse must be replaced, be sure to use a "slow blow" fuse of the current and voltage ratings shown on the rear panel, regardless of the line voltage.

Frequency. The system is factory set to accommodate power-line frequency of 60 Hz. For 50 Hz, a switch on the I/O No. 2 board should be changed. Refer to the service manual, paragraph 2.9.

2.4 LINE-VOLTAGE REGULATION

The accuracy of measurements accomplished with precision electronic test equipment operated from ac line sources can often be seriously degraded by fluctuations in primary input power. Line-voltage variations of $\pm 15\%$ are commonly encountered, even in laboratory environments. Although most modern electronic instruments incorporate some degree of regulation, possible power-source problems should be considered for every instrumentation setup. The use of line-voltage regulators between power lines and the test equipment is recommended as the only sure way to rule out the effects on measurement data of variations in line voltage.

2.5 HANDLER CONTROL

See also Section 5.

2.5.1 Automatic Handler

Control signals needed to control the operation of an automatic device handler are provided at the HANDLER CONTROL connector on the rear panel of the 1732 Test System. Refer to Table 1-2 for the appropriate connector to use in making a cable. Refer to Table 2-1 for the key to signal names, functions, and pin numbers.

The output signals come from the bus drivers that pull each signal line to a low voltage (approx. 0.4 V) when that signal is active and to a higher voltage (approx. 3.4 V) when inactive.

CAUTION

Provide protection from voltage spikes over 7 V.

The input signal (RDY) is also active low and requires a driver, which must pull the signal line down below 0.7 V, but not less than 0.0 V, i.e., not negative. The logic-low current is approximately 27 mA. For the inactive state (logic high), the external circuit must pull the signal line above

Table 2-1
HANDLER INTERFACE CONNECTOR PIN IDENTIFICATION

Signal Name	Pin No.*	Function (All signals "active low")
GND	1,	Ground connection.
RDY	2	Input to the test system, indicates that the peripheral equipment (handler) has the DUT in position and ready to be tested.
DONE	3	Output from system, indicates that the test program has been completed.
Bin 1, 2, 3, 4, 5	4, 16, 5, 17, 6 (respectively)	Output from system, indicates which bin the previously tested DUT belongs in.
FAIL (bin 0)	15	Output, indicating that the DUT has failed to meet at least one bin requirement in the program just run.

* Pin numbers refer to HANDLER CONTROL connector, on the rear panel of the test system, main unit.

+2.4 V, but not above +5 V. An integrated-circuit line driver is recommended for the handler to use in controlling the RDY line. For other configurations, see para 5.2.

2.5.2 Manual Handler

A Manual Handler Assembly, 1732-9710 is available as an option to the 1732 Test System. The assembly is mounted onto the pin electronics module by a single screw, and is used by the operator as an aid to testing and binning devices. Interface is by a cable which plugs into the HANDLER CONTROL socket on the rear of the test system. The interface signals are the same as for an automatic handler.

2.5.3 Footswitch

A footswitch assembly (1732-9681) is available for use with the test system. This option provides a remote start capability. Its cable plugs into the FOOTSWITCH socket and it controls the handler interface RDY line.

2.6 IEEE-488 INTERFACE

See also Section 5.

2.6.1 Purpose

You can connect this instrument into a system (containing a number of devices such as instruments, apparatus, peripheral devices, and generally a controller or computer) in which each component meets IEEE Standard 488-1975, Standard Digital Interface for Programmable Instrumentation. A complete understanding of this Standard (about 80 pages) is necessary to understand in detail the purposes of

the signals at the IEEE-488 INTERFACE connector at the rear panel of this instrument. Commendable introductions to the Standard and its application have been published separately, for example: "Standard Instrument Interface Simplifies System Design," by Ricci and Nelson, *Electronics*, Vol 47, No. 23, November 14, 1974. Another article is "IEEE-488: Promise and Practice," by M.A. Gipe, *Electronic Packaging and Production*, Vol 18, No. 9, September, 1978.

NOTE

For copies of the Standard, order "IEEE Std 488-1978, IEEE Standard Digital Interface for Programmable Instrumentation," from IEEE Service Center, Department PB-8, 445 Hoes Lane, Piscataway, N.J. 08854.

Each device is connected to a system bus, in parallel, usually by the use of several stackable cables. Refer to Section 5 for a diagram of a hypothetical system. A full set of connections is 24 (16 signals plus shield and ground returns), as tabulated below and also in the Standard. Suitable cables, stackable at each end, are available from Component Manufacturing Service, Inc., West Bridgewater, MA 02379, U.S.A. (Their part number 2024/1 is for a 1-meter-long cable.)

This instrument will function as either a talk/listen or a talk-only device in the system, depending on internal switching. "Talk/listen" mode denotes full programma-

Table 2-2
IEEE-488 INTERFACE KEY

Pin No.	Signal Name	Function or Significance
6	DAV	Low state: "data is available" and valid on the DI01...DI08 lines.
7	RFD	Low state: at least 1 listener on the bus is "not ready for data."
8	DAC	Low state: at least 1 listener on the bus is "not done accepting data."
11	ATN	"Attention", specifies 1 of 2 uses for the DI01...DI08 lines, as follows. Low state: controller command messages. High state: data bytes from the talker device.
9	IFC	"Interface clear." Low state: returns portions of interface system to a known quiescent state.
10	SRQ	"Service request." Low: a talker or listener signals (to the controller) need for attention in the midst of the current sequence of events.
17	REN	"Remote enable." Low state: enables each device to enter remote mode when addressed to listen; (Remote-control commands are conveyed while ATN is high.) High state: all devices revert to local control.
5	EOI	"End or Identify." "END" if ATN is in high state, then, low state of EOI indicates end of a multiple-byte data transfer sequence.* "IDY" if ATN is in low state; then, low state of EOI activates a parallel poll.**
1	DI01	The 8-line message data bus, which conveys interface messages (ATN low state) or device-dependent messages (ATN high state), such as remote-control commands from the controller or from a talker device.
2	DI02	
3	DI03	
4	DI04	
13	DI05	
14	DI06	
15	DI07	
16	DI08	
12	SHIELD	Ground
18-24	GND	Ground lines

* "END" is typically sent concurrently with the delimiter "linefeed" character that terminates the string(s) of data output from the test system.

** IDY is not implemented in this test system.

bility and is suited for use in a system that has a controller or computer to manage the data flow. The "handshake" routine assures that the active talker proceeds slowly enough for the slowest listener that is active, but is not limited by any inactive (unaddressed) listener. "Talk/only" mode is suited to a simpler system — e.g., test system and printer — with no controller and no other talker. Either mode provides measurement results to the active listeners in the system.

The handshake cycle is the process whereby digital signals effect the transfer of each data byte by means of status and control signals. The cycle assures, for example, that the data byte has settled and all listeners are ready before the talker signals "data valid." Similarly, it assures that all listeners have accepted the byte before the talker signals "data not valid" and makes the transition to another byte.

2.6.2 Interface Functions

The following functions are implemented in the 1732 Digital IC Test System. Refer to the Standard for an explanation of the function subsets, represented by the identifications below. For example, T5 represents the most complete set of talker capabilities, whereas PPO means the absence of a capability.

- SH1, source handshake (talker)
- AH1, acceptor handshake (listener)
- T5, talker (full capability, serial poll)
- L4, listener (but not listen-only)
- SR1, request by device for service from controller
- RL2, remote control (no local lockout, no return-to-local switch)
- E1, open collector driver
- PP0, no parallel poll
- DC1, device clear implemented
- DT1, device trigger (to start measurement)
- C0, no controller functions.

2.6.3 Signal Identification

Refer to Table 2-2 for a key to signal names, functions, and pin numbers. Further explanation is found in the Standard. The first three signals listed take part in the "handshake" routine, used for any multiline message via the data bus; the next five are used to manage the flow of information; the last eight constitute the multiline message data bus.

2.6.4 Codes and Addresses

The device-dependent messages, such as instrument programming commands and measurement data (which the digital interface exists to facilitate), have to be coded in a way that is compatible between talkers and listeners. They have to use the same language. Addresses have to be assigned, except in the case of a single "talker only" with one or more "listeners" always listening. The Standard sets ground rules for these codes and addresses.

In this instrument, codes for input and output have been chosen in accordance with the rules. The address (for both talker and listener functions) is user selectable, as explained below.

This test system is originally supplied in the talk-only mode, with its IEEE-488 address set to 05. To change between talk-only and talk/listen modes and/or to change the address requires manipulation of an internal switch, as described in the service manual.

WARNING

Because of shock hazard and presence of electronic devices subject to damage by static electricity (conveyed by hands or tools), disassembly is strictly a "service" procedure.

NOTE

Manual operation is possible in either mode. However, if the internal switch is set for talk/listen, this system must be controlled via the IEEE-488 bus. The extended-system controller can enable local control of all devices in the extended system, including this test system.

2.7 SERIAL INTERFACE

See also Section 5.

2.7.1 General

The 1732 test system contains a serial interface port that is configured as a 20-mA loop. Selection of the type of 20-mA operation, active or passive, is made by wire connections in the interface cable. An EIA RS-232 Standard interface is also available as a factory-installed option or retrofit kit. (Inquire if you are interested.)

2.7.2 The 20-Milliampere Current Loop

The 1732 serial port consists of two circuits, a transmitter and receiver, that interface to an 8251 USART (universal synchronous-asynchronous receiver-transmitter). Basically, a 20-mA-loop circuit operates in one of two modes, active or passive. The circuit is active if it contains the source of the current that is switched on or off to represent the data, in which case it must communicate with a passive circuit. Alternately, the circuit is passive if it has no such source, in which case it must communicate with an active circuit. In other words:

1. an active transmitter must talk to a passive receiver;
2. an active receiver must listen to a passive transmitter;
3. a passive transmitter must talk to an active receiver;
4. a passive receiver must listen to an active transmitter.

A 20-mA-current port is usually configured with its circuits in the same mode (ie., both transmitter and receiver active or both passive). Accordingly, the test system is usually set up in either of two configurations:

1. Active mode:
 - Active transmitter, for use with passive external receiver;
 - Active receiver, for use with passive external transmitter;
2. Passive mode:
 - Passive transmitter, for use with active external receiver;

Passive receiver, for use with active external transmitter.

To configure the port for each of the 4 possibilities, make the appropriate set of connections as follows, within the cable that you assemble for the installation.

Active transmitter

- a. Connect -OUT (J6 pin 15) to the external device -IN.
- b. Connect +OUT (J6 pin 3) to the external device +IN.
- c. Connect OUTRET (J6 pin 4) to ground (J6 pins 1, 16) and connect them to the external-device ground.

Active receiver

- a. Connect +IN (J6 pin 14) to the external device +OUT.
- b. Connect -IN (J6 pin 2) to the external device -OUT.
- c. Connect INRET (J6 pin 13) to ground (J6 pins 1, 16) and connect them to the external-device ground.

Passive transmitter

- a. Connect -OUT (J6 pin 15) to the external device -IN.
- b. Connect OUTRET (J6 pin 4) to the external device +IN.

Passive receiver

- a. Connect -IN (J6 pin 2) to the external device -OUT.
- b. Connect INRET (J6 pin 13) to the external device +OUT.

Refer to Table 1-2 for the appropriate connector to use in making a cable. Refer to Table 2-3 for the key to signal names, functions, and pin numbers.

CAUTION

Each current source must be voltage limited so that the loop's transmitter is not damaged when it opens the circuit. Refer to specifications at the front of this manual. If the receiver contains inductive loads (relays) they should have protection diodes for the same

Table 2-3
20-mA PORT I INTERFACE KEY

Signal Name	Pin No.	Function
+ OUT	3	Current source available for "OUT" loop.*
-OUT	15	"OUT"-loop signal (to peripheral device).
OUT RET	4	"OUT"-loop return signal.
+ IN	14	Current source available for "IN" loop.*
-IN	2	"IN"-loop signal (from peripheral device).
IN RET	13	"IN"-loop return signal.
GND	1, 16	Ground connections.

* Current sources are each +12 V dc behind 510 ohms.

2.7.3 RS-232 Serial Interface

The RS-232 interface is standard on systems 1732-9740 through 9744 and is available as an option (P/N 1732-9200) on earlier systems.

To operate the interface, SERIAL INTERFACE must be selected on the output screen, and a jumper on the processor board must be repositioned from the factory setting, which is for 20-mA current loop. See Section 2 of the service manual. The RS-232 interface is configured as shown in Table 2-4.

The DATA SET READY line can be used to throttle data transmission from the 1732. Switching this line negative (-3 V to -25 V) disables transmission. Switching it positive (+3 V to +25 V) or releasing it enables transmission.

Table 2-4
RS-232 PORT I INTERFACE KEY

Pin	Signal Name
1	Chassis ground
2	Transmit data (output)
3	Receive data (input)
4	Request to send (output)
5	Clear to send (input)
6	Data set ready (input)
7	Digital ground
20	Data terminal ready (output)

2.7.4 Baud Rate

The speed with which the test system transmits data can be selected internally, and should be set to be compatible with the peripheral device. The test-system receiving speed should be chosen, similarly (so that each bit of the incoming messages can be recognized). To set the transmission and receiving speeds, refer to service manual paragraph 2.9.

WARNING

Because of shock hazard and presence of electronic devices subject to damage by static electricity (conveyed by hands or tools), disassembly is strictly a "service" procedure.

2.8 AUXILIARY DISPLAY SCREEN (CRT)

To install an auxiliary cathode-ray-tube display monitor, connect from the TTY/CRT connector on the rear panel. Use the CRT described in Table 1-4 or refer to Table 1-2 for the connector to use in making a cable. Refer to Table 2-5 for the signal names, functions, and pin numbers.

Table 2-5
CRT INTERFACE KEY

Signal Name	Pin No.	Function
VIDEO	22	Composite video signal.
VGND	24	Video-signal ground.
VSYNC	12	Vertical synchronizing signal.
HSYNC	21	Horizontal synchronizing signal.
+12 V	23	Power-supply bus, +12 volts.
PGND	10, 11	Power-supply ground.
CHGND	5, 6, 17, 18	Chassis ground.

2.9 ANTISTATIC TEST SETUP

Many types of IC, such as "MOS" devices, can be severely damaged or have their useful life shortened by the static electricity from contact with a person or hand tool. The person may be unaware of the tiny current pulse that ruins his IC. The following precautions are recommended to minimize the chance of such damage.

**HANDLING PRECAUTIONS
FOR ELECTRONIC DEVICES**

SUBJECT TO DAMAGE BY STATIC ELECTRICITY

Static sensitive parts should be transported in conductive (antistatic) envelopes or carriers. Place them and the test system on a work surface defined as follows.

The work surface, typically a bench top, must be conductive and reliably connected to earth ground through a safety resistance of approximately 250 kilohms to 500 kilohms. Also for personnel safety, the surface must NOT be metal. (A resistivity of 30 to 300 kilohms per square is suggested.) Avoid placing electrical parts on insulators, such as books, paper, rubber pads, plastic bags, or trays.

Ground the frame of tester, directly to earth ground. Accordingly (to avoid shorting out the safety resistance) be sure that the grounded tester has rubber feet or other means of insulation from the work surface.

Exclude, from this work surface or area, any hand tools and other items that can generate a static charge. (Examples of forbidden items are non-conductive plunger-type solder suckers and rolls of electrical tape.)

Before handling any static sensitive parts, ground yourself reliably, through a resistance, to the work surface. Use for example a conductive strap or cable with a wrist cuff, which must make electrical contact directly with your

skin; do NOT wear it over clothing. (Resistance between skin contact and work surface through a commercially available personnel grounding device is typically in the range of 250 kilohms to 1 megohm.)

Avoid circumstances that are likely to produce static charges, such as wearing clothes of synthetic material, sitting on a plastic-covered or rubber-footed stool (particularly while wearing wool), combing your hair, or making extensive erasures. These circumstances are most significant when the air is dry.

Handle any static sensitive IC package (typically to connect or remove it from the DUT socket) WITHOUT touching the contact pins. For storage or transportation, enclose such parts in conductive envelopes and/or carriers. Remove the items from such containers only with these precautions or equivalent.

Operation—Section 3

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3.1 INTRODUCTION

3.1.1 General

This section presents information necessary for operating the 1732 Digital IC Test System. Most control actions are prompted by the software and can be implemented via keyboard commands. The operating system generates a series of video display screens which serve as a step-by-step guide. In addition to providing system status information and instructions, the screens display open input fields in reverse-video (brightened) format at selected stages of operation. By "filling in the blanks" and observing the response displayed on this screen, the operator is prompted through the necessary control decisions.

In general, a minimum of operator control is required for routine device testing. Once the operating system software and an appropriate test program have been loaded from tape, all that is required to run a test is to connect the device to be tested via a socket adaptor and press the START button. The advantages of an interactive system become more evident, however, as more detailed input is required to utilize the full range of system capabilities. In particular, the dialog between operator and display screen simplifies the task of programming by reducing it to a predefined sequence of keyboard inputs.

3.1.2 Magnetic Tape Cartridges

A minimum of two tape cartridges is required for operation of the 1732 system: a system software cartridge, and a device programs cartridge.

System Software Cartridge. This tape contains the 1732 operating system software which determines, for example, what the operator's screens look like, what options he has in using them, and how the system will execute test programs.

Device Programs Cartridge. This tape contains test programs. Each test program comprises all the specifications, data, and choice of options necessary to test a specific type of device under operating system control.

For the purpose of operator familiarization and system checkout, GenRad supplies a device program tape with a pre-recorded test program for IC type 74LS161A. Additional programs can be added to this tape. Pre-recorded device program tapes are available from GenRad, as listed in the 1732 Sample Programs Manual, which also includes complete representative sample programs to help you make up your own program tapes. Blank tape cartridges can be formatted under operating system control and then used to record device test programs or test results. Refer to Tape Control (para 3.5) for a detailed description of system tape handling capabilities.

3.1.3 Socket Adaptors

A socket adaptor is required as interface between the device under test and the pin electronics module of the 1732 system. There is a socket adaptor which is wired to provide universal circuit requirements for each pin configuration of DUTs. Special requirements such as additional jumpering, passive components, or active devices for LSI testing are also easily accommodated. Socket adaptor kits are available from GenRad. (See Table 1-4.) Instructions for assembling socket adaptor kits are given in para 3.9.

A ready-to-use socket adaptor, wired for a 16-pin device is supplied with the 1732 system, and is intended for use with the pre-recorded 74LS161A test program.

3.1.4 Precautions

Refer to the front of this manual for a summary of cautions and warnings and for instruction on safety ground connection.

To avoid damage to the DUT, observe the instructions in para 2.9., Antistatic Test Setup. Also, proceed with caution when first operating the system after a change (such as calling up a new test program, revising test data in one, or installing a new socket adaptor). If the first several devices that are tested fail, stop testing and recheck for a possible error in program preparation or socket-adaptor fabrication.

3.1.5 Local and Remote Control

Local control (manual operation) is enabled in the talk-only mode, as this system is originally supplied, unless a "go to remote" command via the serial interface has established remote control. If internal switching is changed to enable talk/listen mode, normal locally controlled operation is possible provided also that the output-mode screen does NOT select the IEEE-488 bus for output and, of course, provided that the IEEE-488 controller is NOT programmed to enable remote control. (See below.)

Talk-only mode enables local control, all serial interface features, and output of data via the IEEE-488 bus to one or more compatible "listen only" devices such as printers. The IEEE-488 handshake may constrain operation in some way. For example, a slow printer may limit measurement rate.

Remote control and programming of this test system via serial interface (20-mA loop) are generally possible in talk-only mode and conditionally possible in talk/listen mode. This condition is that the IEEE-488 bus controller has NOT issued a command to enable remote control. Refer to Section 5.

Remote control and programming of this system via the IEEE-488 bus is generally possible only if internal switch selection has been made to enable talk/listen mode (see para. 2.6) and this mode is implemented with a suitable controller in an extended system. Refer to Section 5. Then all operations are controller initiated by remote commands or device-dependent commands. When the IEEE-488 controller enables remote control, it supercedes all manual and serial-interface control.

The rest of Section 3 describes local control, i.e., manual operation. For more detail about local and remote control, refer to paragraph 5.4.1.

3.2 BASIC OPERATING PROCEDURE

This paragraph gives procedures for loading the 1732 operating system software and testing a specific device under routine circumstances. It is assumed that a pre-recorded test program for the device under test (DUT) exists on a program tape, and that a socket adaptor has been prepared. Additional instructions and exercises are included to familiarize the new user with the basic operation of the system. The new user should perform these procedures using the pre-recorded program tape and prepared socket adaptor supplied by GenRad.

3.2.1 Routine Operation

Steps a, b, and c are routine procedures for loading the operating system software.

CAUTION

Never operate the system without adequate cooling; see below.

Vents should be unobstructed. Verify that there is exhaust air flow at the right side of the pin electronics module (by feeling, listening, or preferably by watching a piece of yarn that you attach to the grille). If this air flow stops, switch power off immediately and obtain repair service.

a. Switch the POWER ON and observe that the POWER ON indicator lights (red) and, for about 45 seconds, a series of character-set displays flash across the screen. The

system is doing a series of core self tests. Then this message appears on the display screen.

INSERT SYSTEM TAPE

b. Insert the system software cartridge, if it is not already in the receptacle. Immediately, the message appears:

PRESS KEYBOARD TO CONTINUE

c. Press [CONTINUE] key promptly (or any other key, but NOT the START button). Notice that you have only about 10 seconds to respond or the system assumes that there is a fault in the keyboard. If so, the message "CORE SELF CHECK 8, NO KEYBOARD" will appear and the system will wait; then press [CONTINUE]; the core self test will automatically restart as in step a; repeat steps b and c. The message:

LOADING appears on the display screen while the operating system is being loaded into memory (somewhat more than a minute). Then, the general information screen will be displayed (para. 3.4).

NOTE

There is an audible sound made by the tape drive while it is running. Become familiar with this sound and be alert to it whenever you operate the system. While the tape drive is running, wait; do NOT continue keyboard operations. However, if the tape drive runs for a long time (over 5 minutes), eject the tape, confirm that it is the one that you want, and restart the procedure.

Steps d through k are routine procedures for testing a device, once the operating system has been loaded.

NOTE

For the new user, the following instruction is recommended: Use the pre-recorded device program tape supplied by GenRad (step d), type in "74LS161A" as the program name in step g, and test a device type 74LS161A (steps h through j).

d. Press the eject button to the right of the tape cartridge receptacle and eject the currently installed cartridge. Select an appropriate program tape cartridge and verify that the tape is write-protected, i.e., that the RECORD bar is set in the direction opposite to its arrow. The RECORD bar should be set to RECORD (write-enabled) only if changes to the programming or file organization of the tape are planned.

e. Insert the program tape cartridge in the tape cartridge receptacle.

f. Press the [PROGRAM CALL] key and observe that the program call screen is displayed (para 3.5).

g. Using the alphanumeric keys on the keyboard, type in the name of desired device test program. (This is a calculator-type keyboard. Press the associated character key to enter any character printed in white. Press the [SHIFT] key and then the character key to enter any character printed in color. Use the [DELETE] key to cancel wrong characters.) Then press the [ENTER] key and observe that two messages appear in sequence, indicating that the specified device test program has been read into memory:

READING...
OPERATION SUCCESSFUL

NOTE

For other than successful tape operations, consult Table 3-1 for an explanation of action to be taken.

h. With the zero-insertion-force connector on the pin electronics module open (lock bar to the right), install the appropriate socket adaptor by aligning the 4 guide pins with the corresponding sight holes, engaging the right side first, and seating the adaptor fully. Then, lock the connector by moving the lock bar to the left.

i. Plug the DUT into the socket adaptor. Typically, for manual testing, the DUT socket is also a zero-insertion-force type. Raise its lever away from the pin electronics module to open this connector; press the lever back to lock it. The DUT should be oriented so that the #1 pin is upper left (nearest the lever). Refer to paragraph 3.10 about contact cleaning.

j. Press the START button to begin testing the DUT. The test will proceed and results will be displayed and output according to the modes set up by the program currently residing in memory. The PASS (green), FAIL (red), and

Table 3-1
TAPE OPERATION MESSAGES

Message	Comment
CARTRIDGE NOT IN PLACE	Tape cartridge not properly seated in tape cartridge receptacle. Eject and re-insert the cartridge.
WRITE PROTECTED	Write operation attempted on write-protected tape. Eject cartridge, move RECORD bar on cartridge in direction of its arrow and repeat operation.
BAD TAPE IN DRIVE (or UNFORMATTED TAPE IN DRIVE)	Tape does not have proper format for your purpose. With exception of GenRad-supplied system software and device program tapes, format operation must be performed on all tapes prior to their use with system.
TAPE ERROR	Error occurred during read or write. Try operation again or try another tape.
NO SUCH FILE (or FILE NOT FOUND)	File name specified for tape operation is not on tape directory. Check directory for exact alphanumeric name of intended file.
FILE ALREADY DELETED	Delete operation was attempted on already deleted file.
FILE WAS DELETED	Read operation was attempted on a deleted file.
FILE WAS NOT DELETED	The "restore" command was used on an existing file that has not been deleted.
NOT ENOUGH SPACE FOR FILE	File block count exceeds block space remaining on tape. Compress tape to make more space or write file on another tape.
DIRECTORY IS FULL	Directory will accommodate up to 50 file names, including "deleted" files. (The directory space is generally adequate for all files that can be accommodated.)
FILE NAME ALREADY EXISTS	File name specified for record operation already exists on tape directory. File name must be unique on any one tape.
NOT A PROGRAM FILE	Program call operation was attempted on results file. Correct the file name or mode of operation.
NOT A RESULTS FILE	Tape operation in results mode attempted on program file. Correct the file name or mode of operation.
CANNOT FIND END OF PROGRAM	End of program file not detected. Read operation unsuccessful.
UNEXPECTED END OF TAPE	End of tape detected before tape operation completed.
BAD DIRECTORY ON TAPE	Attempt to read tape directory unsuccessful. Try operation again. Tape may require re-formatting and re-recording.
ERROR WHILE WRITING DIRECTORY TAPE MAY BE LOST	Tape may still be usable; try again. However, refer to "fatal error" message, below.
FATAL ERROR --- TAPE LOST	A destructive interruption (such as ejection of cartridge or loss of power) occurred while the system was changing the directory. The data on tape cannot be recovered; reformat the tape for new uses.

OPEN (red) lights on the console also provide a quick-look indication of results.

k. To repeat testing of the DUT, repeat step j.

To test additional devices of the same type, remove the DUT and repeat steps i and j as required. To test a device of a different type, repeat steps f through j, if the associated program is on the currently installed tape; repeat steps d through j, if it is not. To shut down operation, switch the POWER OFF.

The test sequence which occurs during step j above is only one combination of several optional modes of operation. For a detailed discussion of how the program determines testing, display, and output modes and how these may affect the operator, refer to System Setup Modes (para 3.6). The new user should proceed to Practice Exercise (below).

3.2.2 Practice Exercise

This exercise is recommended for the new user as a preliminary to further study in this section. It assumes that steps a through j of Routine Operation (above) have been performed by testing a type 74LS161A device with the GenRad-supplied program. The following procedures provide additional hands-on experience and introduce certain fundamentals of test program structure and system operation. More detailed treatment of these topics, with illustrations of typical display screens, is presented elsewhere in this section.

a. Press the [DESCRIBE] key and observe that the describe screen is displayed. This screen defines how the test program currently in memory "sees" the DUT. Notice that the 74LS161A has 16 pins, each of which has been identified according to a code defined along the left margin of the screen. Also notice that "# OF GROUPS" has been defined as six. This means that six distinct groups of test conditions will be applied to the 74LS161A to test it parametrically.

b. Press the [GROUPS] key and when the reverse-video (brightened) field appears at the top of the screen, press the [1] key to view the screen which defines the test parameters for group 1. In the same way, use the [GROUPS] key with the [2] key and then with the [3] key (etc) to display the remaining groups of parametric test conditions.

c. Press the [TRUTH TABLE] key to display the truth table screen. Notice that the 16 pins are identified across the top of the table and data lines are numbered as steps along the left margin. These steps define the sequence in which the indicated binary data patterns are applied to the input pins and verified at the output pins of the DUT to test it functionally.

d. Press the START button on the console to test the 74LS161A again (as in step j of Routine Operation). The DUT is tested both parametrically and functionally according to the data defined in the describe, parameters, groups, and truth table screens. Results in terms of pass or fail and bin information are displayed as each test group is completed. Results from one group of tests may be displayed for only a short time, being replaced by later results as they become available; only the results of the last test group remain displayed for inspection.

The test program, as supplied, may be set up for the optimum mode of operation under certain circumstances.

Suppose, however, that you want to know the results of parametric testing in detail for each test group. This would require changes of run mode and display mode in your program, as follows.

e. Press the [RUN] key to view the run-mode screen. Press the [ENTER] key and observe that the reverse-video (brightened) input field shifts position on the screen. Now press the [ENTER] key repeatedly and shift the brightened field until it includes the triangular pointer opposite ALL GROUPS FIRST FAILURE, which is the current run mode of the program. Next, using the [down-arrow] key, move the pointer until it is opposite the desired run mode: STOP AFTER EACH GROUP.

f. Press the [DISPLAY] key to view the display screen and notice that the triangular pointer in the brightened input field is opposite PASS/FAIL/BIN. Use the [down-arrow] key to position the pointer opposite the desired display mode: PARAMETRIC RESULTS. Now press the [ENTER] key to shift the input field opposite "1—8" and press the [CHANGE UNIT] key to set a pointer in the field, thereby selecting the designated pins. Next press the [down-arrow] key to move the input field opposite "9—16" and again press the [CHANGE UNIT] key to set a pointer in the field. Accordingly, parametric results will be displayed for all 16 pins of the 74LS161A.

g. Press the START button to test the device and notice that this time the parametric results of test group 1 remain displayed for pins 1—8. Press the [ENTER] key to view the results for pins 9—16. Press the [CONTINUE] key to resume testing and then display the results of test group 2 in the same manner. Repeat the same keyboard commands for test group 3.

The test program that now resides in memory is the same as the original program except that it has been modified to display parametric results in detail. In order to retain this modified version for future use, proceed as follows:

h. Eject the program cartridge, set the RECORD bar on any suitable program cartridge (one that is available for program recording) in the direction of its arrow (write-enable), and install this cartridge.

i. Press the [PROGRAM RECORD] key and observe that the program record screen is displayed with a brightened field ready for input. Using the alphanumeric keys, type in a name, say, "X74LS161" for the modified program. Now press the [ENTER] key to brighten the comment field and type in a comment, say, "PRACTICE.MOD". Press the [ENTER] key a second time to record the program on tape and observe that two messages appear in sequence at the bottom of the screen:

WRITING...

OPERATION SUCCESSFUL

CAUTION

Do NOT eject the tape cartridge while tape drive is running (unless it fails to stop in 5 minutes). Interruption of a critical portion toward the end of the writing process can cause irrevocable loss of all programs on tape.

j. Eject the program cartridge, set the RECORD bar in the direction opposite to its arrow (write-protected), and reinstall the cartridge.

k. Press the [TAPE OPERATION] key and observe that the tape operation screen is displayed with the triangular pointer in a brightened field. If it is not already positioned there, use the [up-arrow] or [down-arrow] key to position the pointer opposite GENERAL TAPE OPERATION. Now press the [ENTER] key to brighten the next field and, in the same manner, position the pointer opposite LIST TAPE DIRECTORY. Press the [ENTER] key a second time to execute the tape operation and observe that the message

READING X appears at the bottom of the screen, followed by a display of the tape directory screen. This screen lists the contents of the currently installed tape and allows you to verify that it now contains the modified program X74LS161.

The new user should now proceed to study the remaining paragraphs of this section. Further exercises similar to the one just completed are recommended as a means for learning new operational procedures. For example, by performing steps a through g of Routine Operation (above), practice program X74LS161 could be called into memory at any time and then used to practice keyboard control, experiment with different modes of operation, make further program modifications, etc.

3.2.3 Duplication of the Operating System

It is recommended that you keep two copies of the system software on tape. If one of the copies is damaged or otherwise lost, make another copy from the good one as follows.

a. Obtain a blank cartridge, preferably new. If it was previously used or formatted, be sure to "bulk" erase it to remove all recorded data. Slide the RECORD bar in the direction of its arrow (write enabled).

b. Load the operating system software into system memory, as in Routine Operation, steps a, b, c, above, using the known good system tape.

c. Eject the cartridge and insert the blank, write-enabled cartridge instead.

d. Press the [AUXILIARY] key. Use the [down-arrow] key to move the cursor on the auxiliary screen to select "debug" and the [ENTER] key to obtain the debug screen.

e. After the debug screen has been called up, press [SHIFT] [W] [SHIFT] [X] keys to initiate tape operation, which requires about 5 minutes. During this process, the screen displays a bright square to the right of the letter W. Completion of the operation is indicated by the square moving to a position under the letter W.

f. After the tape operation is completed, eject the cartridge, remove its RECORD bar—writing permanently disabled—and label the cartridge clearly for identification.

Notice that the duplicated system software is equivalent in every practical way to the original except as follows. Whereas the original displays the word LOADING for about a minute (see Routine Operation, step c), the duplicated software will display the word LOADING for only a few seconds, followed by the debug screen, which remains while the tape is being read; after that, the general information screen will appear.

3.3 KEYBOARD CONTROL

Operation of the system is controlled primarily at the keyboard and most control actions are software-prompted or interactive. That is, you enter commands or data accord-

ing to information on the display screen; the software, in turn, updates the information in response to your action, thereby prompting your next action, etc. This paragraph is a general introduction to keyboard commands and interactive data entry. Specific instructions, as they apply to the individual video display screens, are given in associated screen descriptions.

3.3.1 Keyboard

The keyboard is shown in Figure 1-1. In this text, all labels will appear in upper-case characters and key labels will be enclosed in brackets []. Some of the keys function as characters and control keys, others as screen keys.

Character and Control Keys. The lower portion of the keyboard contains the character and control keys. To select a character or function labeled (above the key) in white, press the associated key. To select a character or function labeled (below the key) in color, press the [SHIFT] key and release it; then press the associated key. The function of the character keys is to enter alphanumeric data in the video display screens.

Control key functions are summarized in Table 3-2. For details, see Interactive Data Entry.

Table 3-2
CONTROL-KEY FUNCTIONS

Key(s)	Function
[CHANGE UNIT]	Cycles through the options available in a cursor field.
[DELETE]	Deletes data in an alphanumeric cursor field.
[ENTER]	Stores in memory the data contained in a cursor field.
[◀ ▶ ▲ ▼]	(Referred to in the text as the [left-arrow], [right-arrow], [up-arrow], or [down-arrow] key.) Shifts the location of the cursor field on the screen in the direction indicated.
[+ / -]	Toggles the sign of numerical data in a cursor field.
[CONTINUE]	Causes the system to resume a programmed test sequence after a pause (para. 3.6).
[SHIFT] [EDIT]	Activates the editor mode for interaction with the truth table screen.
[SHIFT] [I/O]	Toggles the assignment of a bidirectional pin from input to output, or vice versa, when used with the truth table screen.

You can initiate an automatic repeat function by pressing and holding a control or character key for two seconds. Thereafter, the function (control or character entry) repeats rapidly until the key is released.

Screen Keys. The upper portion of the keyboard contains the screen keys which control specific video display screens. The keys are grouped and labeled according to four basic functions; see Table 3-3.

In general, the labels of the screen keys correspond directly to the screens they call. Thus, the [DESCRIBE] key calls the describe screen. However, the [SHIFT] key can also be used with the [PARAMETERS] or [GROUPS] keys to call corresponding "alternate" program screens, and the [AUXILIARY] key calls up a menu of screen choices.

Table 3-3
SCREEN-KEY FUNCTIONS

Key	Function
[DESCRIBE] [PARAMETERS] [GROUPS] [TRUTH TABLE]	PROGRAM. The program screens control the input of "fill in" data in test programs.
[AUXILIARY]	This screen serves as access to several special purpose screens.
[PROGRAM CALL] [PROGRAM RECORD] [TAPE OPERATION]	The tape control screens control tape file management.
[RUN] [DISPLAY] [OUTPUT]	SYSTEM SETUP MODES. These screens control selections in the run, display, and output modes of operation.

3.3.2 Interactive Data Entry

Input Fields. The video display screens are a programmed to accept data in certain fields and in a certain sequence. The currently active field, or cursor field, is brightened to indicate that it is open for input. Any information that the field contains, or that is typed in, is displayed in dark characters. So long as the information is displayed in this mode, called the reverse-video mode, it is only potentially entered. You can delete or change the information in a variety of ways, but it is not actually entered, or input into memory, until the proper input command is issued.

Usually, pressing the [ENTER] key or the [right-arrow] key will input potential data. In certain cases a specific character key or any arrow or screen key will also cause input. The most general rule is the following: in a programmed screen sequence, commands which close one field and open the next field also cause data to be input from the field being closed. Successful input is indicated when the display mode of the input data goes from reverse video back to normal video (bright characters on a dark field).

The video display screens provide two general types of fields for data input: option fields and alphanumeric fields. Option fields may be further classified as pointer, scroll, or enable types. In general, option fields display a set of predetermined options from which you specify one or more as input. Alphanumeric fields require a character or set of characters as input.

Option Fields.

- Pointer option.
- Scroll option.
- Enable option. See below.

The pointer-option field appears as a vertical reverse-video field containing a single triangular pointer. The field is located to the left of a list of two or more options. Use the [up-arrow] or [down-arrow] key to position the pointer opposite the desired option. Press the [ENTER] key to input your choice. As an example, the tape operations screen contains a pointer-option field for the options:

GENERAL TAPE OPERATION and
RESULTS CALL/RECORD

The scroll-option field appears as a reverse-video field containing one of a series of options, typically numerical values or units. Press the [CHANGE UNIT] key to display the next option available in the field. Press and release the [CHANGE UNIT] key repeatedly to scroll through all the op-

tions. Use the [SHIFT] and [CHANGE UNIT] keys to scroll in reverse order. Press the [ENTER] key to input the currently displayed option as your choice. As an example, the describe screen contains a scroll-option field labeled C0, which permits choice of a clock frequency from a series of available frequencies.

The enable-option field appears as single-character, reverse-video field opposite a single option. The field either contains a triangular pointer, indicating the option is enabled (chosen), or it is blank, indicating the option is disabled (rejected). Press the [CHANGE UNIT] key to enable or disable the option. Generally, press one of the arrow keys or the [ENTER] key to input your choice. As an example, the display-mode screen contains a column of enable-option fields for pin designation. The options are labeled "1—8", "9—16", etc.

Alphanumeric Fields. In general, to enter data in an alphanumeric field, simply type the appropriate characters and then press the [ENTER] key. Some fields are pure numeric; they will accept sign, decimal point, and digits only. Additional rules and restrictions are as follows.

1. Initial entry. If a field already contains data when it is opened, all former characters are replaced by the first new character typed.
2. Sign. Use the [+ / -] key either just before or just after typing a numerical entry, to toggle the sign from positive to negative or vice versa.
3. Deletion. To delete the last (right-hand) character from an entry you are typing, press the [DELETE] key. If the [DELETE] key is pressed before data is typed in a newly opened field, all characters in the field are deleted.
4. Size. Each field has a specific length (in reverse video) corresponding to the max character count. If you type more characters, something overflows.
5. Overflow protocols. In comment, program name, password, or other field where the alphabet is accepted, the display is left-justified when typed in, overflow is at the right, and "least-significant" characters can be lost. However, in a purely numeric field, the display is right-justified, overflow is at the left, and "most-significant" characters, including decimal point, can be lost. (Sign is always preserved in an overflow situation.)
6. Characters allowed. In certain fields, the software will reject all but a special set of characters, or all but numerical values within certain limits, etc. In such cases, the screen refuses to display any invalid characters or responds with a question mark (?).
7. There is no key for blank or space (an invalid character). In a comment field, use the decimal point [.] as a substitute.

3.4 VIDEO DISPLAY SCREENS

3.4.1 General

Table 3-4 outlines briefly how to call up each screen. The table is arranged in the order of the calling keys, with reference to paragraph numbers below. (Descriptive text is arranged in functional order.)

Table 3-4
OUTLINE OF KEYSTROKES THAT ACCESS SCREENS

Keystrokes	Screens (Text Paragraph Numbers)
[DESCRIBE] key	Describe screen (3.7.2)
[PARAMETERS] key	Parameters group-1 screen (3.7.3)
[SHIFT] [ALTERNATE PARAMETERS] keys	Alternate parameters group-1 screen (3.7.4)
[GROUPS] [2] keys	Parameters group-2 screen (3.7.5)
[SHIFT] [ALTERNATE GROUPS] [2] keys (similarly for groups 3, 4, 5, 6)	Alternate-parameters group-2 screen (3.7.5)
[TRUTH TABLE] key	----- Truth-table screen (3.7.6)
[AUXILIARY] key	Auxiliary screen-selection screen (3.6.6)
• [ENTER] key	• Gate/strobe screen (3.7.7)
• [down-arrow] [ENTER] keys	• Serial interface options screen (3.6.9)
• [down-arrow] [ENTER] keys	• Test statistics screen (3.6.7)
• [down-arrow] [ENTER] keys	• (See "Redisplaying Results", para 3.6.6.)
• [down-arrow] [ENTER] keys	• ("Debug", primarily for GenRad use)
[PROGRAM CALL] key	Program call screen (3.5.4)
[PROGRAM RECORD] key	Program record screen (3.5.5)
[TAPE OPERATION] key	Tape operation screen (3.5.6)
[RUN] key	Run-mode screen (3.6.1)
[DISPLAY] key	Display-mode screen (3.6.2)
• [ENTER] key	• After the test, pass or fail screen (3.6.3)
• [down-arrow] [ENTER] keys	• After the test, result summary screen (3.6.4)
• [down-arrow] [CHANGE UNIT] [ENTER]	• After test, parameter results screen (3.6.5)
[OUTPUT] key	Output-mode screen (3.6.8)

Each of the video display screens is unique in function. Some only provide information, but most are interactive and contain embedded input fields. These fields are programmed to accept data of a certain type and in a certain sequence. Normally, when an interactive screen is initially called, the first input field in the programmed sequence is displayed in reverse video. The keyboard command that inputs data to the CPU from the first field also closes it and opens the next field. This action returns the first field to normal video and displays the next field in reverse video. Accordingly, by following the movement of the reverse-video cursor field and issuing the proper sequence of input commands, you can cycle through all the input fields in a screen.

3.4.2 Introductory Procedure

As a preliminary exercise, the new user is advised to call a program into memory (i.e., perform steps a through g of Routine Operation, para 3.2) and proceed to examine a particular screen. We shall use the run-mode screen as an example. Proceed as follows.

- a. Press the [RUN] key to view the screen.
- b. Press the [ENTER] key a few times and notice you can move the cursor field without entering new data or altering current data.
- c. Press the [right-arrow] key and notice it has the same effect. It moves you through the input fields in the normal (forward) sequence.
- d. Press the [left-arrow] key a few times and notice that the sequence is reversed and you can return to previous fields.
- e. Continue to press and release the [ENTER] key and notice that the movement is cyclic. That is, after the last field in the screen, you return to the first field in the screen.
- f. Continue to cycle through the screen a second time and notice that, when the cursor field passes under "Bin

1", "Bin 2", etc., it stays on the upper row of the "bin" columns.

g. Press the [down-arrow] key to move down to the next field in the same bin column. Press the [up-arrow] key to return to the previous field. Press the [down-arrow] key repeatedly and notice that, once again, the movement is cyclic. That is, after the bottom field in the column you are returned to the top field.

The above exercise illustrates the most general rules of cursor field control. There are a number of exceptions and the user should refer to the appropriate screen description, when using a particular screen for the first time.

NOTE

Details of data entry are not repeated in the following screen descriptions. Refer to para 3.3, above.

3.4.3 General Information Screen

Figure 3-1

The general information screen appears after the operating system software has been loaded (Routine Operation, para 3.2) and also after abortion of a test being run. It identifies the version of the operating system that is in effect and gives brief instructions to the operator.

3.4.4 Other Screen Descriptions

An illustration and description of each video display screen are included where they apply in the operational instructions for tape control, system setup modes, and program functions, below. Input specifications for all interactive screens are given in detail. Input fields are identified by their associated screen labels (see paragraph heads in upper-case italics below) and are discussed individually with regard to data function and method of keyboard entry. The order of discussion is the same as the normal (forward) programmed sequence for each screen.

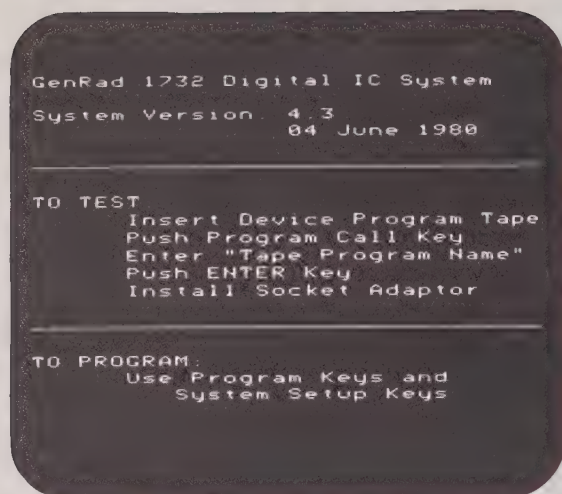


Figure 3-1. General information screen, automatically displayed after the operating system tape has been read.

3.5 TAPE CONTROL AND RELATED SCREENS

The mass storage capabilities of the system are based on cartridge-type magnetic tape. Each tape cartridge provides access to 92K bytes of storage. Tape operations are controlled via the tape control screens and are not programmable. Any tape control command is executed by the system when the command is input at the keyboard.

The operating system, itself automatically loaded from a separate cartridge, provides read, write, and file management capability for two types of tape files: (1) program files, and (2) result files. Both types of file can coexist on the same cartridge, although, in practice, the user may wish to keep them separately on "results tapes" and "program tapes". The alphanumeric name of a file must be unique on any one cartridge.

Write Protection. On each cartridge, there is a sliding bar labeled RECORD. Slide it in the direction of the arrow to permit recording, or the other way to prevent recording. If the bar is missing, recording is prevented.

3.5.1 Program Files

Each program file contains one test program, i.e., all of the applications software necessary to test one type of device. The terms "program" and "program file" are used interchangeably when referring to tape operations. A program file can have either of two sources: It can be developed and recorded by the user under operating system control, or it can be obtained directly from GenRad on a pre-recorded program cartridge (para 3.1). The size of program files varies considerably. Typically, a program cartridge contains programs for over fifteen different devices. However, the program for a microprocessor device may require an entire cartridge. Read and write operations for program files are controlled by the program call screen and program record screen, respectively.

Tape Program Name. The tape program name, otherwise known as the program file name, is not necessarily the same as the test program name; but for simplicity they can be identical. Refer to Program Record Screen and Describe Screen, below.

3.5.2 Result Files

Each result file contains results of the last group of the last test. The format of the results depends on the option in effect in the display-mode screen during the test. Read and write operations for result files are controlled by the CALL RESULT and RECORD RESULT commands, respectively, in the tape operation screen. Also in this screen, the SEND ALL RESULT FILES TO SYSTEM OUTPUT command can be used to transfer results from tape to the IEEE-488 bus and/or 20-mA current loop. This option provides for an alternative method of data logging. For example, instead of burdening an external unit, say a computer or peripheral, with test results in real time, the results can be saved on tape cartridge and then transferred to that unit in a single operation at the end of the work day.

Result File Name. The result file name consists of two parts: the base (which for simplicity can be all or part of the program name) and the group. The result-file name may be entered via the tape operation screen. The system automatically appends a decimal point and the number of the group just tested. On any given tape, for each result file that is recorded, the name base remains unchanged (until a different one is entered). Because the eleventh and twelfth characters of the result-file base name are ignored, we recommend that the base be limited to 10 characters.

3.5.3 File Management

The following general file management operations are controlled by the tape operation screen and apply to both program and result files, and to any tape cartridge (except the system software cartridge, which should *never* be altered by the user).*

List Directory. The LIST TAPE DIRECTORY command lists the contents of an installed tape, including file names, comments, and block storage accounting. Result file names are displayed in reverse video.

Format. The FORMAT TAPE command performs a block-by-block check of a tape and formats it to receive program and result files. This permits the user to prepare blank or used tapes (the operation erases previous data) for use with the system. However, the recommended procedure is to erase previously used tapes in a demagnetizer before formatting.

The tape is formatted for 92 blocks, each capable of storing 1K bytes of data, regardless of the fact that (usually) there is room for more. The 92-block standard format minimizes the chance that any tape-duplicating effort might be thwarted by a slight shortage of storage space on a blank tape.

NOTE

Files are destroyed by either the FORMAT TAPE command or (after flagging by DELETE PROG/RES) the COMPRESS TAPE command.

Delete and Restore. The DELETE PROG/RES and RESTORE PROG/RES commands set and remove flags at specified tape files, thereby deactivating these files and restoring them to active status, respectively, as required.

* Any alteration automatically raises a flag.

Flagged files are not actually deleted until the tape is compressed.

Compress. The COMPRESS TAPE command permanently deletes flagged files and compresses the remaining active file organization.

3.5.4 Program Call Screen

Figure 3-2

Press [PROGRAM CALL] to call this screen. The program call screen is used to call a test program into system memory for the purpose of device testing, program management, or program modification. A program tape cartridge should be installed before proceeding.

TAPE PROGRAM NAME =. Enter the name of a program that is on the installed program tape. The existence of the program on tape, and the exact spelling, can be verified by inspecting the tape directory screen.

Alphanumeric field (up to 12 characters). Press [ENTER] to input the name and initiate the following action: the system searches for the specified program and reads it from tape into system memory. Tape operation messages are displayed at the bottom of the screen. (See Table 3-1 for an explanation of tape operation messages.)

3.5.5 Program Record Screen

Figure 3-3

Press [PROGRAM RECORD] to call this screen. It is used to record a test program on a program tape. A formatted, write-enabled program tape should be installed and the program to be recorded should reside in system memory at the time that this operation is initiated.

TAPE PROGRAM NAME =. Enter the name under which the program in memory is to be recorded on tape. This name must differ from all the names in the tape's directory. It is entered in the tape directory and becomes the reference for subsequent calls to this program. (See Program Call Screen.)

NOTE

The tape program name is usually (for convenience) the same as the program name (in the describe screen) and often the same as the type "number" of the DUT. However, all three of these can be different if you prefer.

Alphanumeric field (up to 12 characters). Press [ENTER] to input the name and open the next field.

COMMENT =. User's comment associated with the tape program name. This comment, together with the name, is recorded in the tape directory. (See Tape Directory Screen.)

Alphanumeric field (up to 15 characters). Press [ENTER] to input the data and initiate recording. Tape operation messages are displayed at the bottom of the screen. (See Table 3-1 for an explanation of tape operation messages.)

Do NOT eject the tape cartridge during the recording process. (See para 3.2.)

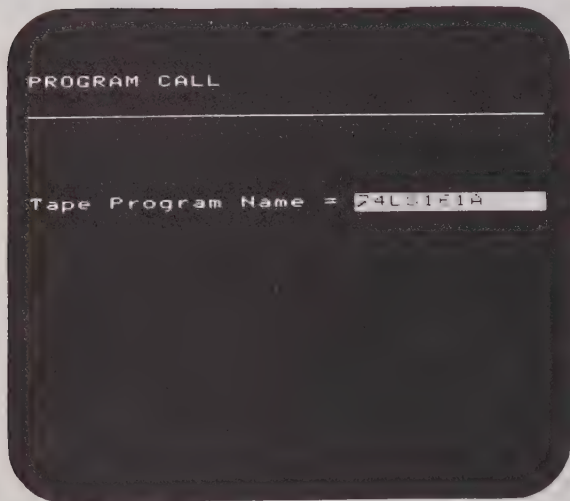


Figure 3-2. Program call screen. Use the alphanumeric field for the name of the program you want read from tape.

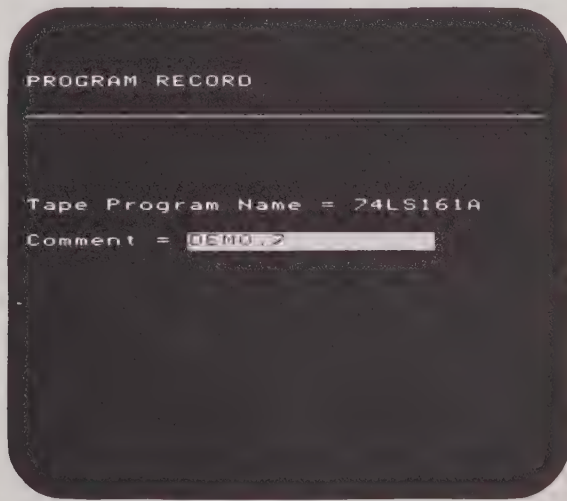


Figure 3-3. Program record screen. The tape program name is independent of the program name (describe screen); however it is often convenient to make these names identical. They can, of course be based on the DUT type "number." The comment is for your convenience and will appear with the tape program name in the tape directory (screen), but not in the program call screen. Comment should not exceed 15 characters (even though some early versions of this screen allow 16).

3.5.6 Tape Operation Screen

Figure 3-4

Press [TAPE OPERATION] to call this screen. It is used to control the management of magnetic tape files. An appropriate tape cartridge must be installed before executing any commands via this screen. Tape operation messages are displayed at the bottom of the screen. Successful execution is indicated by the message "OPERATION SUCCESSFUL". If an operation is other than successful, refer to Table 3-1 for an explanation. Input specifications are as follows.

The MODE field is a pointer-option field presenting a choice of two basic modes of tape operation. Use the [up-arrow] or [down-arrow] key to position the pointer at your choice. Press [ENTER] to input your choice and proceed to subsequent options.

1. GENERAL TAPE OPERATION. A general mode of operation, which handles both program and result files.
2. RESULTS CALL/RECORD. A special mode of operation which handles result files only. These modes are explained below.

GENERAL TAPE OPERATION Mode.

If you chose the GENERAL TAPE OPERATION mode, use the [up-arrow] or [down-arrow] key to position the pointer at one of the following commands.

LIST TAPE DIRECTORY. Display the tape directory screen (described elsewhere). Press [ENTER] to execute this command. If OUTPUT is enabled, a printed copy of the directory is produced.

DELETE PROG/RES. Flag a program or results file of specified name for deletion. This deactivates the file until it is either permanently deleted by a COMPRESS TAPE command, or restored to active status by a RESTORE PROG/RES command.

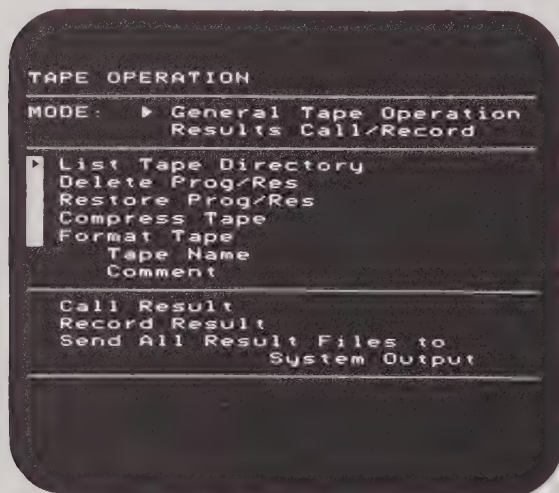


Figure 3-4. Tape operation screen. Each of the "►" symbols represents a pointer that can be moved to any one of two or more options. An alphanumeric field becomes available, to the right on the line, if the selected option requires an associated file (tape program) name. "Prog/Res" designates the name of a test-program or results file; "Result", the name of a result file. Because "format" destroys all files on the tape and "compress" destroys the files that have previously been named for deletion, each of these commands evokes a "Do you really..." message, which must be answered with a "Y" before the operation will proceed. Other (self-explanatory) messages may appear in the bottom part of the screen.

Press [ENTER] to open the associated alphanumeric field (up to 12 characters) and then type in the name of the file to be flagged for deletion.

Press [ENTER] a second time to execute the DELETE PROG/RES command.

RESTORE PROG/RES. Restore to active status (i.e., remove the flag from) a file of specified name that has been flagged for deletion.

Press [ENTER] to open the associated alphanumeric field (up to 12 characters) and then type in the name of the file to be restored to active status.

Press [ENTER] a second time to execute the RESTORE PROG/RES command.

COMPRESS TAPE. Permanently delete all files that have been flagged for deletion and compress the remaining active file organization.

Press [ENTER] to initiate this command and observe that the following message is displayed at the bottom of the screen as a reminder that, once this command is executed, files flagged for deletion can no longer be restored.

DO YOU REALLY WANT TO COMPRESS THE TAPE?

Type the letter Y (yes) to execute the COMPRESS TAPE command. If you type N (no) or press any other key, the cursor returns to the beginning of this screen.

FORMAT TAPE. Format and check the tape, block by block; label it with a tape name and comment. All previously recorded data are lost.

Press [ENTER] to open the TAPE NAME field.

TAPE NAME. Tape identification name which will appear in the heading to all tape directory displays of this tape. (See tape directory screen, below.)

Alphanumeric field (up to 12 characters). Press [ENTER] to input the name and open the COMMENT field.

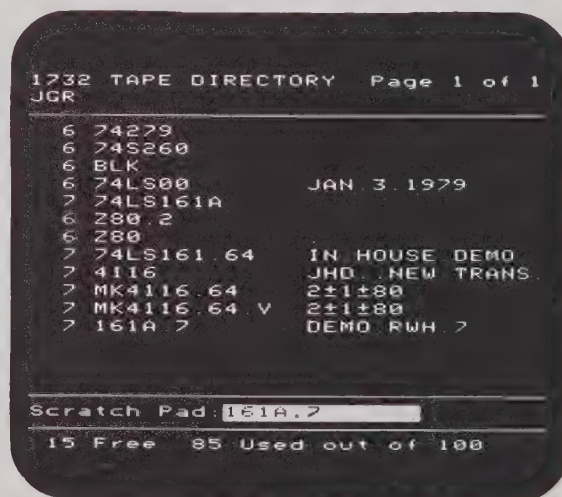


Figure 3-5. Example of a tape directory with program files only. (Result files would be shown in reverse video.) The screen lists tape files totaling 78 blocks and indicates that 85 blocks are used. (Probably a 7-block file has been "deleted" but not destroyed by compressing.)

COMMENT. User's comment, which will be included in the heading to all tape directory displays of this tape.

Alphanumeric field (up to 16 characters). Press [ENTER] to input the comment and observe that the following message appears at the bottom of the screen as a reminder that, once this command is executed, all data previously recorded on this tape are lost.

DO YOU REALLY WANT TO FORMAT THIS TAPE?

Type the letter Y (yes) to execute the **FORMAT TAPE** command. If you type N (no) or press any other key, the cursor returns to the beginning of this screen.

RESULTS CALL/RECORD Mode.

If you chose the **RESULTS CALL/RECORD** mode, use the [up-arrow] or [down-arrow] key to position the pointer at one of the following commands.

CALL RESULT. Read a result file or specified name (base name and group number extension) from tape into memory. To view a results screen, choose the screen type on the **DISPLAY MODE** screen, select "Results" on the **AUXILIARY** screen, and press [ENTER]. If the test was performed under "fast test" conditions (Pass/Fail selected on the **DISPLAY** screen and **OUTPUT** enabled), only the Pass/Fail results screen is valid; the **RESULTS SUMMARY** and **PARAMETRIC RESULTS** screens contain non-valid data.

If IEEE or 20 mA is enabled on the **OUTPUT MODE** screen, the results are sent out immediately after the tape is read.

RECORD RESULT. Record the results of the most recent test group in a result file of specified name.

Press [ENTER] to open the associated alphanumeric field and then type in the desired result-file base name, using no more than 10 characters (see para 3.5.2).

Press [ENTER] a second time to execute the **RECORD RESULT** command. When in the "Fast Test" mode, only the pass/fail screen results are valid. Summary and parametric screen results are not valid.

SEND ALL RESULT FILES TO SYSTEM OUTPUT. In order to record test results of all groups on tape, proceed as follows. Set the **RUN MODE** screen to Stop After Each Group. Press [START]. When the group 1 results appear, go to the **TAPE OPERATION** screen, key in the base name, and press [ENTER]. The first group is now recorded. Press [CONTINUE] to display the group 2 results and record them as above. A test group may be skipped by pressing [CONTINUE] twice. The resulting files have the same base name with the group numbers as extensions.

3.5.7 Tape Directory Screen

Figure 3-5

This screen is called by the **LIST TAPE DIRECTORY** command in the tape operation screen and displays the contents of a currently installed tape. The heading to each page of the directory contains the tape name, descriptive comment, and page number. Program files are listed by name (12-character fields) and may have associated comments at the right on the same lines (15-character fields). Result files are listed by name only and appear in reverse video. The number of blocks occupied by each file is shown to the left of the file name. Accounting for total block space appears on the bottom line of the screen. Notice that the sum of blocks "free" and blocks "used" will be less than the block total if bad blocks were detected when the tape was formatted.

The tape directory screen lists up to 15 files per page. To view the next page of the directory, press [ENTER]. When on the last page, press [ENTER] to return to the first

page. Press another screen key to exit from this screen.

The **LIST TAPE DIRECTORY** command causes the name of the presently installed tape to be written into system memory (where other information, such as a test program from a different tape, may also reside).

SCRATCH PAD. Alphanumeric field, up to 12 characters. The tape directory screen provides this input field near the bottom of the screen, for your convenience. Any name entered here is automatically entered in the name field of the program call screen and the appropriate name fields of the tape operation screen. Thus, while referring to the tape directory, you can type the name of a file you plan to operate on and subsequently, when you call the screen that initiates that operation, you will find the name already entered.

3.6 SYSTEM SETUP MODES AND SCREENS

The system provides a variety of programmable options, which control the system modes of operation. The options for a particular program are selected via the system setup modes screens and determine the run mode and the mode for display and output of test results at the time the program is executed.

Of the three display modes, the pass/fail/bin mode is the fastest. Additional software run time is required to quantify results for the results summary and parametric results modes.

The three selectable control modes for an external parts handler (1) operate the handler continuously, (2) stop it after a specified number of consecutive fails, or (3) turn it off. For more information on handler operation, see below and refer to Section 5 of this manual.

3.6.1 Run Modes

The options selected in the run-mode screen determine how a program runs and may affect the control actions required of the operator. In general, a test is programmed as a sequence of test groups (as defined in the parameters screen and groups screen), each with distinct results available as output. Typically, the operator presses the **START** button to initiate the test sequence and observes the following events. The following message is superimposed in reverse video on the screen currently displayed, while the first test group is run.

TESTING

On completion of the first group, the results screen for that group is displayed and the **TESTING** message is superimposed on that screen while the second test group is run, and so on until the results screen for the last test group is displayed (without the **TESTING** message), indicating that the test has been completed.

Generally, only the results of the last group remain displayed. The operator can then press **START** to test the next device. If **START** (also labeled **ABORT**) is pressed before the test sequence is completed, however, the test is aborted and the system displays the general information screen.

The programmable options in the run-mode screen generally implement some variation of the run mode just described; these options are discussed individually, below. In addition to the options that directly concern the operator when a program runs, the run-mode screen also controls the subgroup test sequence, functional step specification, bin requirements, and keyboard lock.

Run-Mode Screen

Figure 3-6

Press [RUN] to call this screen. The data entered in the run-mode screen determine the system's modes of testing. In addition, the screen provides access to keyboard lock. Input specifications are as follows:

TEST SEQUENCE (C, K, F, P). Sequence of performing continuity, Kelvin, functional, and parametric types of tests. One, two, three, or all of these test types can be designated in any sequence, which then applies to all groups. However, if the sequence contains continuity and/or Kelvin tests, they are performed before the F and P tests, regardless of the screen-entered sequence.

Bin n (F P). Bin-requirement table for functional (F) and parametric (P) type testing.

Table of enable-option fields. Press [CHANGE UNIT] to toggle options in each field. Use the [up-down] arrow or [down-arrow] key to move to the next field within each column of fields. Use the [left-arrow] or [right-arrow] key to move from one column of fields to the next. When in the last column, use the [right-arrow] or [ENTER] key to open the next field outside the table.

Bin Requirements. The binning software allows the user to sort devices into 6 different bins (5 Pass and 1 Fail). Each bin is defined by a set of functional and parametric tests in one or more groups. Specification of bin requirements is done by entering the symbol "►" in the "F" and "P" columns for each appropriate group (see Table 3-5).

Table 3-5
EXAMPLE OF BIN SPECIFICATIONS

	Bin 1 F P	Bin 2 F P	Bin 3 F P	Bin 4 F P	Bin 5 F P
G 1	►►	►►	►	►	
R 2	►►				
O 3	►►	►►	►►		
U 4	►				
P 5	►►	►►	►►	►►	
S 6	►►				

If a device fails either the continuity or Kelvin tests, or if there is a power-supply shutdown in any of the groups, or if no bins are specified, bin 0 (the Fail bin) is selected. This procedure is referred to as "bin on pass."

For example, assume the test results given below occurred. According to the bin requirements in Table 3-5, bin 3 would be selected. Bin 4 would never be selected, even if all the tests specified in bin 4 passed. This is because the 1732 selects the lowest-numbered bin in which all specified subgroups pass. Since bin 3 is a subset of bin 4, bin 3 is selected first. In general, less stringent requirements should be specified for higher-numbered bins.

		Functional	Parametric
G	1	pass	fail
R	2	pass	pass
O	3	pass	pass
U	4	xxxx	pass
P	5	pass	pass
S	6	fail	pass

FUNCTIONAL: STEP. Step number in the truth table at which functional testing is to begin. Default is 0. Your selection applies to all groups.

Alphanumeric field (up to 4 characters). Only numbers 0 to 4094 are allowed. Press [ENTER] to input the data and open the next field.

TO. Step number in the truth table at which functional testing is to end. "End" indicates last step of truth table. Default is "End". Your selection applies to all groups.

Alphanumeric field (up to 4 characters). Only numbers 0 to 4094 or the letter E are allowed. Press [ENTER] to input the numerical data and open the next field, or type the letter E to input the word "End", automatically opening the next field.

Test Until... Modes. The next field is a pointer option field, presenting a choice of five basic modes for testing a DUT. Use the [up-arrow] or [down-arrow] keys to position the pointer at any one choice. Press [ENTER] to input your choice and open the next field.

1. **ALL GROUPS FIRST FAILURE.** Testing stops on the first failure. If no failure, all groups are run once.
2. **ALL GROUPS.** All groups are run once, regardless of failure. Select this option if binning is used.
3. **STOP AFTER EACH GROUP.** Testing stops after each group, permitting visual inspection of group-test results. Press [CONTINUE] to run the next group. Press START to start again with first group.
4. **TEST CONTINUOUSLY TO FAILURE.** Testing continues through all groups and recycles until first failure. This choice or the following one are useful for test-program debugging.
5. **TEST CONTINUOUSLY.** Testing continues through all groups and recycles until aborted. To abort, press the ABORT button (also labeled START) and hold it down for 2 seconds.

KEYBOARD (IS/NOT) LOCKED. Software lock which, when locked, inhibits keyboard entry of data into PROGRAM and SYSTEM SETUP MODES screens of the program currently in system memory. Excepted are the screen keys, the GROUP number field of the group screen, and the lock itself, which is accessible via a password on the run-mode screen. (all tape control screens and functions remain unlocked). Once the program is stored on tape in the locked state, it is effectively secured from change by any person not in possession of the password. Thus, at supervisory discretion, testing can be restricted to standardized modes of operation.

Scroll-option field (2 options). Press [CHANGE UNIT] to toggle the option. Choose "IS" to lock or "NOT" to unlock the keyboard. Press [ENTER] to input your choice and open the next field.

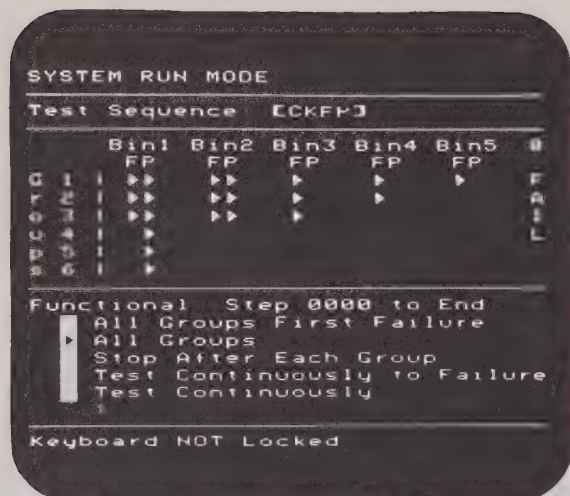


Figure 3-6. Run-mode screen. Each triangle symbol in the binning requirements table is a “pass” requirement, separately designated for functional and parametric tests. Both start and finish step numbers for functional testing can be entered at the positions shown 0000 and END. In this example, testing will continue through all groups (regardless of any failure); you need a START signal to initiate testing; and the keyboard is NOT locked.

(XXXXXX). Password used to lock or unlock the keyboard.

Unlabeled alphanumeric field (up to 6 characters). Press [ENTER] to input the password. The resulting action depends on the state of the keyboard lock, as explained below.

Locking the Keyboard. When the keyboard is unlocked, the first field in the locking sequence is the scroll-option field (IS/NOT). To lock the keyboard, proceed as follows:

a. Using the [CHANGE UNIT] key, choose “IS” and then press [ENTER] to open the password field.

NOTE

When you lock the keyboard, it is important to make a note of the password for subsequent reference. While the keyboard is locked, changes to the program via the program and system setup modes screens are prevented. Loss of password necessitates reprogramming from scratch to implement such changes.

b. Type in a password if none is displayed. Otherwise, either retain the displayed password or type in a new one. To actually lock the keyboard, press [ENTER]. This action stores and, at the same time, erases the currently displayed password. Notice that at any time before pressing [ENTER] this second time, it is possible to return to the (IS/NOT) option field (use the [left-arrow] key) and unlock the keyboard. The purpose of this feature is to minimize the chance of accidentally locking the keyboard.

Unlocking the Keyboard. When the keyboard is locked, the only open field in the run-mode screen is the unlabeled password field. To unlock the keyboard, proceed as follows.

a. Type the password in the blank open field.
b. Press [ENTER] to input the password. If the password entered matches the password in memory, the scroll-

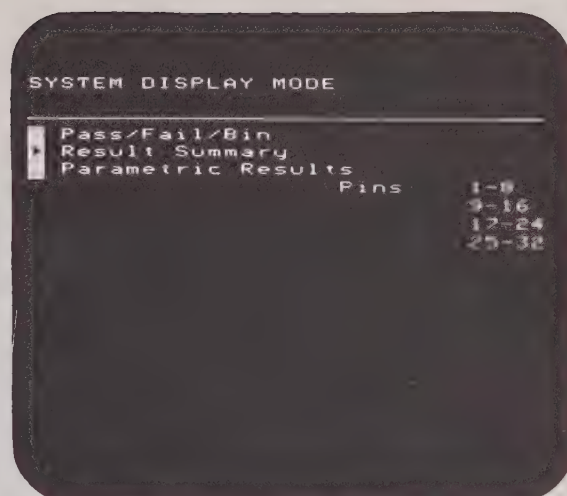


Figure 3-7. Display-mode screen. The triangular pointer can be moved to any of 3 options. If you select PARAMETRIC RESULTS, you can also select one or more 8-pin ranges to be displayed (up to the highest-numbered pin shown in the describe screen).

option field (IS/NOT) is automatically opened and set to “NOT”, thereby unlocking the keyboard. If a match is not achieved, the password field remains open and you can try again.

3.6.2 Display-Mode Screen

Figure 3-7

Press [DISPLAY] to call this screen. The display-mode screen presents a choice of three video display modes for test results. Use the [up-arrow] or [down-arrow] key to position the pointer opposite your choice. Press [ENTER] to input your choice.

PASS/FAIL/BIN. Results are displayed in the format of the pass screen or fail screen. If the run-mode selection (see above) is TEST CONTINUOUSLY, the pass or fail screen appears after each group, reporting the results of that group only. However, for ALL GROUPS, the results are withheld until the test program is completed; then the pass or fail screen appears, reporting final results, complete with bin assignments.

RESULT SUMMARY. Results are displayed in the format of the result summary screen.

PARAMETRIC RESULTS. Results are displayed in the format of the parameter results screen. Choice of this option entails the pins options (below.)

PINS: 1—8, 9—16, etc. The pin ranges indicate the pin results that will be displayed in the parameter results screen. If no pins are chosen, an error message is displayed at the bottom of the screen.

Column of enable-option fields (up to 6). Each pin range is a separate option. Press [CHANGE UNIT] to toggle each option. Use the [up-arrow] or [down-arrow] keys to move within the column of options. Press [ENTER] or another screen key to input your final choice.

NOTE

After a test has been run and the results displayed according to the programmed display mode, you can obtain additional results displays without repeating the test; refer to "Redisplaying Results" in para 3.6.6.

3.6.3 Pass and Fail Screens **Figures 3-8,3-9**

The pass/fail/bins mode is one of the three results formats selectable in the display-mode and output-mode screens. This mode displays either a pass screen or a fail screen at the completion of each test group, depending on the test results. The group number is indicated on each screen and, on fail screens, the failures are categorized C, K, F, or P to indicate failure in the continuity, Kelvin, functional, or parametric test, respectively. The bin assignment of the DUT is shown at the bottom of the last pass or fail screen, i.e. on completion of the last group in the test sequence. Bin assignments of 1 to 5 are highlighted in reverse video. Zero (0) bin assignments are indicated in normal video.

3.6.4 Result Summary Screen **Figure 3-10**

This is one of the three results formats selectable in the display-mode screen and output-mode screen. The result summary screen tabulates pass/fail results of continuity, functional, and parametric types of tests for each test group, for all DUT pins. Complete parametric results for any one pin can be displayed on command.

The test program name and group number of the test results appear at the top of the screen. In the event of a functional failure, the number of the truth-table step at which failure occurred is displayed on the next line. The main table has a row for each pin that was defined in the describe screen and 4 columns C, K, F and P for the continuity, kelvin, functional, and parametric types of tests, respectively. A failure in any of these tests is flagged in the appropriate row and column by a single-character, reverse-video field. The only field for keyboard entry is PIN, as follows.

PIN. Pin number for which you want all parametric results displayed. The default is pin 1.

Alphanumeric field (up to 2 characters). Only numbers 1 to n are allowed where n is the "# of PINS" defined in the describe screen. Press [ENTER] to input the number and display the desired results.

Notice that the measured parameter values appear along the left margin. Only parameters appropriate to the selected pin are displayed—IIL and IIH for an input pin, Vi and Ii for a power supply pin, etc. Values flagged as failures appear in reverse video.

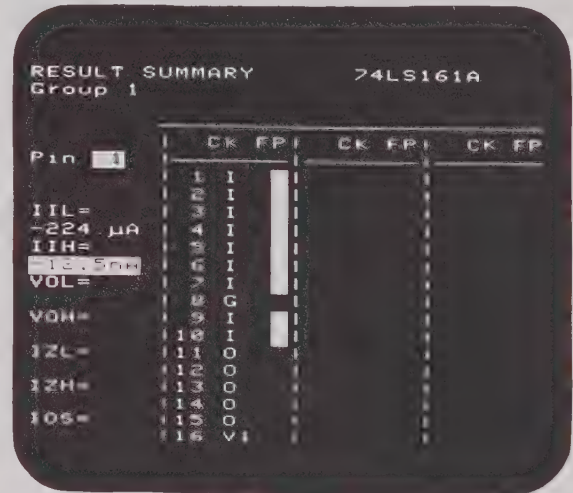


Figure 3-10. Result summary screen. In the heading are the program name (describe screen), the test group being summarized (output mode screen), and the step number of functional failure (if any). Pin 1 has been specified for a display of measured parametric results, which appear tabulated at the left. The main table summarizes any continuity, functional, and parametric failures, by flagging them with reverse-video blocks at the pertinent pin numbers. In this example, there are parametric failures at all input pins, including the parametric failure of IIL at pin 1.

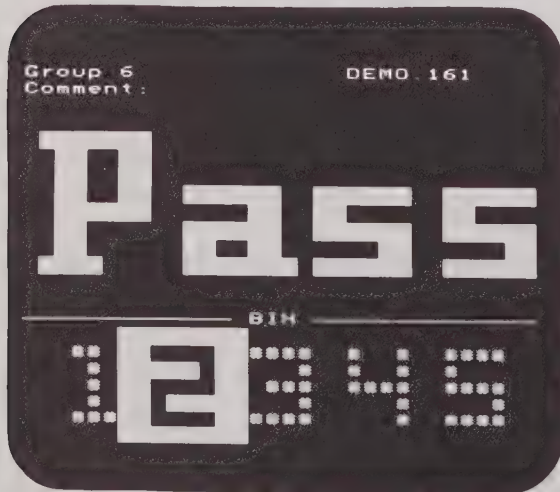


Figure 3-8. Pass screen, example for group 6, with bin-2 requirements satisfied.



Figure 3-9. Fail screen, example for 74LS161A with continuity-test failure in group 6.

3.6.5 Parameter Results Screen

Figure 3-11

This screen is one of the three results formats selectable in the display-mode screen and output-mode screen. The parameter results screen displays measured parameters for up to eight pins at a time. If selected in the output-mode screen, results for all the DUT pins are output. If selected in the display-mode screen, only results for those pins selected in that screen are shown (in groups of 8 pins). Press [ENTER] to view results for the next eight pins. Volts or amperes are the assumed units of measurement; only the multipliers (m, u, or n) are indicated. Values flagged as failures appear in reverse video.

3.6.6 Auxiliary Screen Selection

Figure 3-12

Certain special-purpose screens, ones that have no unique key assignment, are called indirectly by use of the auxiliary screen, which you call with the [AUXILIARY] key. Position the pointer by the name of the desired screen; press [ENTER]. The special screens include: a choice of results ("Redisplaying Results," described below), test statistics, serial interface, gate/strobe, and debug (primarily for GenRad use). To exit from any such screen, press another screen key such as [DESCRIBE].

Re-displaying Results. The display options are normally pre-selected on the displaymode screen, become part of the test program, and take effect when the program is executed. That is, the results of the most recent test group are automatically displayed in the selected format and remain in memory until replaced by results from a subsequent test group. If the "Fast Test" mode has been selected on the run-mode screen, the Summary and Parametric results are not valid. The most recent results may be redisplayed in a different mode without re-running the test, provided that the "Normal Speed" mode has been selected on the run-mode screen and the run sequence has stopped. This condition is met after the last group of any run, or after any group when the run mode is "stop after each group". The re-display procedure is as follows:

- Press the [DISPLAY] key to call the display-mode screen and select the desired display mode.
- Press the [AUXILIARY] key and then the [down-arrow] key to select "Results."
- Press [ENTER] to re-display the test results in the newly selected mode.

By this method, for example, results originally flagged as FAIL in the pass/fail/bin mode can be re-examined in detail by choosing the parametric results or result-summary display mode.

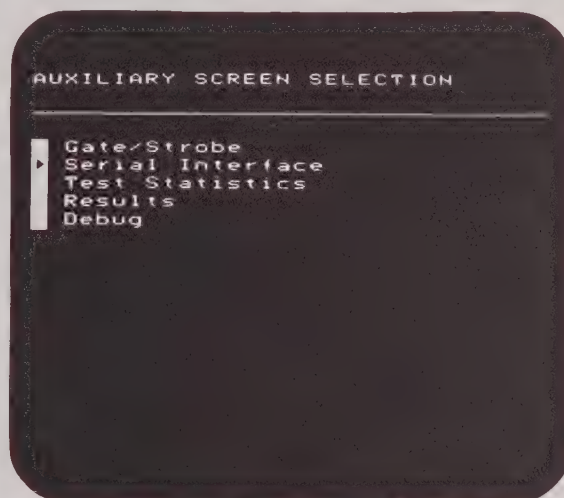


Figure 3-12. Auxiliary screen, called up by the [AUXILIARY] key, provides a "menu" of special-purpose screens. After the cursor has been positioned at your choice, use the [ENTER] key to see that screen.

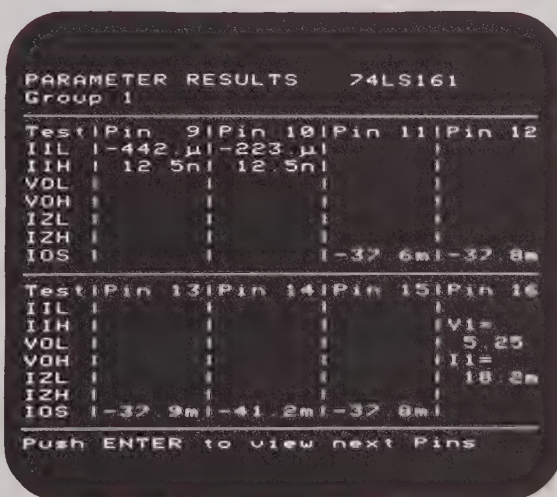
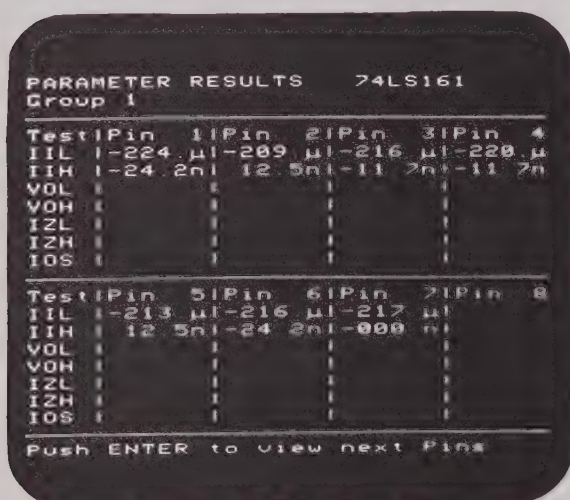


Figure 3-11 a, b. Parameter results screens, example for 74LS161. The heading shows program name and group number, as in the result-summary screen heading. The main table presents measured parameters as indicated, for up to 8 pins per display. Units of measurement are assumed (amperes and volts), but the multipliers (m, u, n) are displayed.

3.6.7 Test Statistics Screen

Figure 3-13

Press [AUXILIARY] to obtain the "menu" of auxiliary screens. Use the [down-arrow] key to position the cursor at TEST STATISTICS; press [ENTER] to obtain the test statistics screen.

This screen presents a summary of test results since the last time its counter was reset. The main display includes total numbers of tests completed, passed, failed, and the number of DUTs assigned to each bin. These groups numbers are incremented whenever all groups are tested.

RESET CLOCK. Cursor field for manual entry of (present) time.

Press [ENTER] to enable entries, as below.

DAY, MONTH, YEAR, HOUR, MINUTE

Enter 2-digit number for each in sequence. Hours are 00 to 23. (To correct an error, use [DELETE] and/or [left-arrow] keys.) When the display is correct, press [ENTER] to set the real-time clock to this time.

RESET COUNTER. Cursor field for manual resetting of totals.

Press [ENTER] to accomplish the resetting.

3.6.8 Output-Mode Screen

Figure 3-14

Press [OUTPUT] to call this screen. The output-mode screen is used to control system output at the IEEE-488 and 20-mA interfaces so that test programs (screen by screen) and results data can be supplied to a printer or other peripheral equipment. The output-mode screen also establishes the conditions for stopping tests while the extended system includes an external parts handler. Refer to Section 5. Screen input specifications are as follows.

All the input fields under the labels ENABLE, SCREEN COPIES, RESULTS FORMAT, and GROUPS are enable-option fields. Press [CHANGE UNIT] to enable or disable each option individually.

ENABLE

However, if neither IEEE nor 20 mA is enabled, the [ENTER] command moves you to HANDLER options. If either IEEE or 20 mA or both are enabled, [ENTER] moves you to the SCREEN COPIES options.

IEEE. Send data on the IEEE-488 bus.

Press [down-arrow] to input your choice and open the next field.

20 mA. Send data on the 20-mA current loop.

Press [ENTER] to input your choice and open the next field.

SCREEN COPIES

The data formats are the same as given in the pertinent screen descriptions. Program data are sent promptly after initiation by appropriate keystrokes. Typically, program data for a device test program can be sent to an external unit as header information prior to datalogging of test results. If neither TRUTH TABLE nor ALL OTHERS is desired, press [ENTER] to move to the RESULTS FORMAT options.

TRUTH TABLE. Send truth-table data as output.

Press [down-arrow] to input your choice and open the next field.

ALL OTHERS. Send all other program screen data as output. This includes the following screens: describe, gate/strobe, parameters (all), alternate parameters, display mode, run mode, and output mode.

Press [ENTER] to input your choice and initiate sending data. When output is completed, you are returned to this screen with both SCREEN COPIES options disabled.

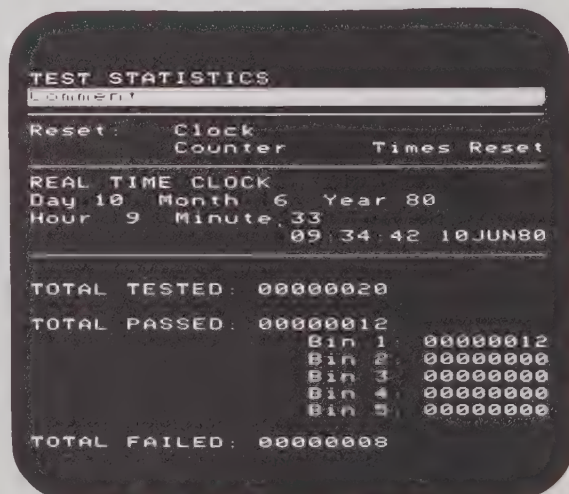


Figure 3-13. Test statistics screen. The main display area shows totals of tests completed, those passed and those failed, and how many assignments have been made to each bin. These counts can be manually reset to zeroes to begin new totals, but in so doing the system automatically increments the "times reset" number. Under REAL TIME CLOCK are 2 lines for setting the clock to the desired starting condition and a third line for continuous display of hours: minutes: seconds dayMONTHyear. All time data is numerical except "MONTH", and even that is entered as a number initially.

RESULTS FORMAT

Options selected here cause test results to be sent as system output in the indicated screen formats. Output takes place automatically as results become available during a test sequence.

PASS/FAIL/BIN. Send as pass or fail screen data.

Press [down-arrow] to input your choice and open the next field.

RESULTS SUMMARY. Send as results summary screen data.

Press [down-arrow] to input your choice and open the next field.

PARAMETRIC RESULTS. Send as parameter results screen data.

Press [down-arrow] to input your choice and open the next field.

FAILURES ONLY. Send failed results only, according to the formats indicated above.

Press [ENTER] to input your choice and open the next field.

GROUPS n. Send results for the indicated groups only. Up to n groups can be selected where n is the "# OF GROUPS" defined in the describe screen.

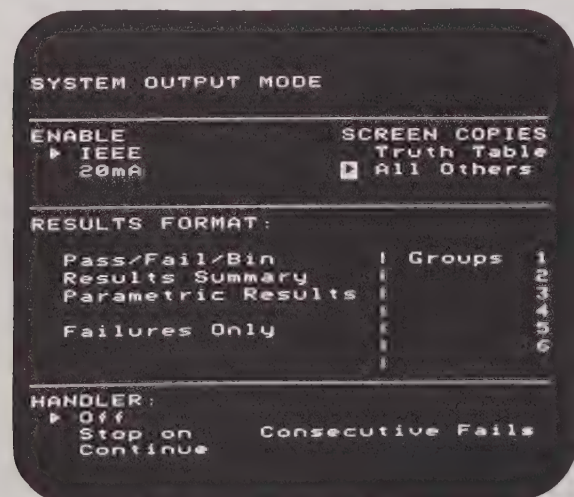


Figure 3-14. Output-mode screen. If you select either of the options under ENABLE (use the [CHANGE UNIT] key), you can select either (1) one or both options under SCREEN COPIES (then [ENTER] key will initiate output action) or (2) any options under RESULTS FORMAT. (Then the output is automatically provided as it becomes available during testing.) Under HANDLER, the pointer can be set at any one of three options, the second of which includes a number field (1...99). Under HANDLER DEBOUNCE (not shown in this photograph, not featured before software version 4.4) the options are ON and OFF.

Column of n fields. Use the [down-arrow] key to move down the column of fields. Press [ENTER] to move to the HANDLER options.

HANDLER

Any one of the HANDLER options is selectable in the pointer-option field. Use the [up-arrow] or [down-arrow] key to position the pointer at your choice. Press [ENTER] to input your choice.

OFF. The handler is turned off.

STOP ON (XX) CONSECUTIVE FAILS. The handler halts operation after a specified number of failures. Choice of this option entails a numerical input.

Alphanumeric field (numbers 1 to 99 are valid.).

CONTINUE. The handler operates continuously.

3.6.9 Serial Interface Options Screen

Figure 3-15

Press [AUXILIARY] to obtain the "menu" of auxiliary screens. Use the [down-arrow] key to position the cursor at "Serial Interface"; press [ENTER] to obtain the serial interface options screen.

This screen displays several options in the serial interface message codes, particularly the determination of characters to be used for line termination, padding (for delay between lines) and start (printing).

LINE TERMINATION. Choice between 2 character strings: carriage return with or without linefeed. Pointer option field. Use [up-arrow] or [down-arrow] key to make selection and [ENTER] to input that choice and open the next field.

PAD CHARACTER. Choice among 3 non-printing characters to be used for padding, as identified on the screen. Pointer option field like the preceding one. However after entry of the choice, the next field to open is the following.

NUMBER TRANSMITTED. Numeric field. Enter the number of pad characters that you want to be sent after each line, to function as a time delay.

START CHARACTER. Choice between 2 character strings to be used as a "start" command (typically required by printers). Pointer option field, in which the second option must be further defined as follows.

KEYBOARD. Alphanumeric field for a 2-character hexadecimal number of your choice. After completing the choice (and entry, if required) press [ENTER].

PARITY SELECT. Choice among 3, as follows: NO, ODD, and EVEN. Pointer option field. Use [up-arrow] or [down-arrow] key to make selection and [ENTER] key to input your choice.

3.7 PROGRAM FUNCTIONS AND SCREENS

3.7.1 General

The 1732 system PROGRAM screens define basic test program structure and prompt the programmer through the process of "filling in" program specifications. In general, data entry is simplified by the menu-type format of these screens and no programming language is required. A small set of special instructions and commands is used exclusively in the truth table screen to provide subroutine, looping, and editing functions.

A set of worksheets is provided at the end of Section 4 and also in the Sample Programs Manual, as an aid to program development. Generally, the programmer should plan the program on copies of these worksheets before entering it via the PROGRAM screens. A discussion of program generation, including instructions for filling out worksheets, is given in Section 4 of this manual.

Sync frequency relationships

Internal sync selection is an important example of the interdependence of hardware and software in program planning. Clock CO is chosen in the describe screen; but a jumper on the socket adaptor determines which divisor—1, 2, 4, 8 or 16—acts on clock CO to generate the sync. (Sync frequency is applied to the DUT; in other words, the truth-table steps are executed at this rate. A coded entry for "SYNC" in the describe screen is necessary to provide the CPU with the chosen divisor.)

For any divisor, there is a set of several—up to 15—sync frequencies that can be obtained. The selection of clock frequency CO, in the describe screen, determines the particular sync frequency of that set. Using the CO span of 1 to 8 MHz, you can select sync frequencies of 62.5 kHz to 2 MHz. Refer to paragraph 4.3 for illustration.

3.7.2 Describe Screen

Figure 3-16

Press [DESCRIBE] to call this screen. The data entered in the describe screen provide the initial definition of the DUT, as "seen" by the device test program. Input specifications are as follows.

NAME. Test program name. It is generally, but not necessarily, the same as the DUT type designation.

Alphanumeric field (up to 12 characters). Press [ENTER] to input the data and open the next field.

COMMENT. User's comment. The entry is for information only; it does not affect the software.

Alphanumeric field. The word "Comment" disappears when the first character is entered, leaving space for 32 characters. Press [ENTER] to input the data and open the next field.

OF PINS = . Total number of pins (up to 48) on the DUT.

Alphanumeric field (up to 2 characters). Only numbers 1 to 48 are allowed. Press [ENTER] to input data and open the next field.

OF GROUPS = . Number of test groups (up to 6). Each test program consists of a number of test groups, each of which corresponds to a distinct group of parametric test conditions, as defined in the parameters screen and groups screen.

Alphanumeric field (1 character). Only numbers 1 to 6 are allowed. Press [ENTER] to input the data and open the next field.

CO. Clock frequency. A choice of 15 frequencies is available, ranging from 1 to 8 MHz. The default value is 4 MHz. The corresponding period (ns) is also displayed for each choice.

Scroll-option field. Press [CHANGE UNIT] to scroll through the options. Press [ENTER] to input your choice and open the next field. The options are as follows:

8.00	3.20	2.00	1.45	1.14
5.33	2.66	1.78	1.33	1.07
4.00	2.29	1.60	1.23	1.00

SYNC. Sync clock frequencies. The options are as follows, where the default is C4:

EXT — External sync (not generated by the system)
C1 — CO/1 (i.e., CO)

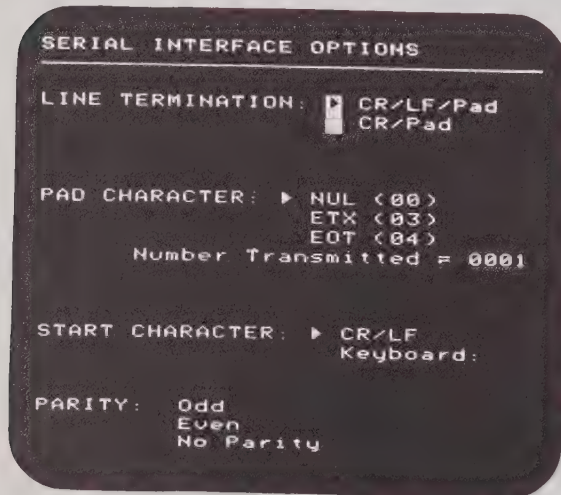


Figure 3-15. Serial interface screen. For line termination, choose which of two sequences will be used to terminate each line of serial data. The term PAD refers to one of three choices under PAD CHARACTER which is automatically repeated. Specify also the number of pad characters to be sent as "pad", for the purpose of time delay. (They are not recognized by standard printers.) Choose also between a commonly used start command or any 2-digit hexadecimal number that you enter after the word KEYBOARD as a start command.

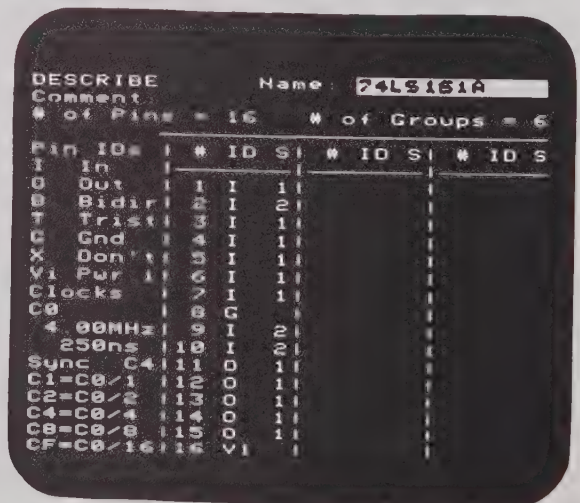


Figure 3-16. Describe screen, example for 74LS161A. The test program NAME and optional comment occupy the first two lines. The maximum # OF PINS is 48; max # OF GROUPS is 6; and highest value of CO is 8.00 MHz. The combination of CO and the SYNC divisor must not specify a sync frequency greater than 2 MHz. Note that the listing of pin IDs in the left column of this screen may not include C1, because of space limitation. However, a pin can be clocked directly by giving it an ID of C1, C2, ... or CF, and by making the corresponding connection in the socket adaptor.

- C2 — CO/2 (i.e., CO divided by 2)
- C4 — CO/4 (i.e., CO divided by 4)
- C8 — CO/8 (i.e., CO divided by 8)
- CF — CO/16 (i.e., CO divided by 16).

Scroll-option field (up to 6 options). Press [CHANGE UNIT] to scroll through the options. Press [ENTER] to input your choice and open the next field.

NOTE

The sync clock selection cannot be implemented by data entry alone; it must also be wired on the socket adaptor board. (See "Sync frequency relationships" above and also paragraphs 3.9 and 4.3.)

ID S. Pin identification (ID) and pin set (S). The column of numbers (1, 2, 3...) identifies the pins. Each pin has an ID and an S field to the right.

ID must be specified by a 1- or 2-letter code, as follows:

- I — Input
- O — Output
- B — Bidirectional
- T — Tristate
- G — Ground
- X — Don't care
- Vi — Voltage source, where i = 1, 2, or 3 designates one of the device power supplies.
- Ci — Clock, where i = 1, 2, 4, 8, or F designates the clock frequency or one of its submultiples.

NOTE

The assignment of any particular pin to G, Vi, or Ci cannot be implemented by data entry alone; it must also be wired on the socket adaptor board (para 3.9).

Pin set (S) can be either 1 or 2. This assigns a pin to either of two separate sets of parametric test conditions available in each test group. Pins identified G, X, V, or C cannot be assigned to a pin set.

The ID and S fields constitute an alphanumeric table. Typing the appropriate character(s) in one ID field causes a default value to be entered in the corresponding S field and opens the next ID field, such that progress from first pin to last pin is automatically prompted. Do *not* use the [ENTER] key before the table is completed. Otherwise the cursor returns to the first field in this screen.

An invalid character entered for ID or S is ignored by the system and not displayed. To change or correct data, overwrite the unwanted characters with the desired characters. Do *not* use the [DELETE] key in this table, except in the one case discussed below.

Entry of I, O, B, or T in an ID field automatically enters a default value of 1 in the corresponding S field. To assign a pin to pin set 2, use the [left-arrow] key to return to the S field and then over-write the 1 with a 2. Entry of G, X, V, or C in an ID field automatically invalidates any entry in the corresponding S field.

Typing a V or a C in an ID field extends the field for a second character. After V, one of the numbers 1, 2, or 3 is valid to designate one of the device power supplies. After

C, one of the characters 1, 2, 4, 8, or F is valid to designate the clock frequency or one of its submultiples.

If you enter a V or a C in error at the first character position of an ID field, you can press the [DELETE] key to remove the wrong character and restore the previous ID and S fields. This is the *only* case where use of the [DELETE] key is allowed in this table. If you enter an invalid character at the second character position of an ID field, the screen displays a question mark (?) which can be overwritten in the usual manner. If you press the [ENTER] key or any screen key while at the second position of an ID field, a default value of X is entered as the pin ID.

To move through this table without entering data, use the arrow keys. Use the [up-arrow] or [down-arrow] key to move within the column of ID fields or within the column of S fields. Use the [left-arrow] or [right-arrow] key to move between an ID and an S field. Accordingly, you can cycle through fields that have already been filled in and make changes or corrections.

NOTE

If the truth table has been filled in (even partially) before you change the ID of any pin, the following procedure is necessary.

a. To accommodate any changed ID, if the truth table is reasonably short, use the change command in edit mode (paragraph 3.7.6) to reenter the data into system memory from every line, thus:

```
[TRUTH TABLE] [SHIFT] [EDIT]
[C] [ENTER] [0] [ENTER] [ENTER]
[C] [ENTER] [1] [ENTER] [ENTER]
[C] [ENTER] [2] [ENTER] [ENTER]
... etc, throughout the truth table
[SHIFT] [EDIT]
```

b. However, if the truth table is long, record and recall the program, thus:

```
[PROGRAM RECORD] (new name for program)
[ENTER] [ENTER]
```

```
After the OPERATION SUCCESSFUL message,
[PROGRAM CALL] (same program name) [ENTER]
```

3.7.3 Parameters Screen

Figure 3-17

Press [PARAMETERS] to call this screen. The data you enter in the parameters screen specify the test parameters for group 1 of the test program. Input specifications are as follows.

SUPPLIES STEP. Step number in the truth table at which the power supplies are to be tested.

Alphanumeric field (up to 4 characters). Only the numbers 0 to 4094 are allowed. Press [ENTER] to input the data and open the next field.

The remainder of the screen defines the functional and parametric test parameters in terms of voltage and current values, as follows.

VOLTAGE (Vi=). Supply voltage level(s) for this group, where i = 1, 2, or 3 designates as voltage source one of the three device power supplies. (See Specifications at the front of the manual.)

TEST LIMIT (Ii=). Current limit(s) for the designated power supply test(s). Any measured result in excess of the limit is flagged as a failure.

I-MAX. Maximum current limit(s) for the designated power supplies. Any measured result in excess of the maximum causes shut-down of the associated power supply. If no value is specified here, the default value is the test limit (above).

Note that I-MAX determines the power-supply range (R-sense) and this in conjunction with the test limit li determines DVM range, as explained under "Test Limit and I-max Selection" in paragraph 4.2.

The parameters specified as *test limits* appear (or are entered) in the left-hand column, under S1 and S2 (pin set 1 and 2, respectively). The terms "low level" and "high level" in these definitions refer to logic voltage levels.

- IIL** Current, for an input pin at low level, VIL applied.
- IIH** Current, for an input pin at high level, VIH applied.
- VOL** Voltage, for output pin at low level, IOL drawn.
- VOH** Voltage, for output pin at high level, IOH drawn.
- IZL** Leakage current, tristate pin in the "off" (high-impedance) state, VZL applied.
- IZH** Leakage current, tristate pin in the "off" state, VZH applied.
- IOS** Short-circuit current, min and max limits, for output pin at high level, VOS applied.

The parametric *test condition* corresponding to each of those limits appears to the right. Each condition is preceded by the symbol @:

- VIL** Low-level voltage, for an input pin.
- VIH** High-level voltage, for an input pin.
- IOL** Low-level current, for an output pin.
- IOH** High-level current, for an output pin.

- VZL** Low-level voltage for tristate pin in the "off" state.
 - VZH** High-level voltage for tristate pin in the "off" state.
 - VOS** Voltage (usually zero) for short-circuit test of an output pin at high level.
- Refer to para 4.3 for more detailed definitions.

Functional *test conditions* appear (or are entered) in the far-right column. These are the nominal values of the drive levels for logic high and low for all pins in this set, for all functional tests in this group: VIL, VIH, IOL, and IOH. (Sense levels are VOL and VOH, from column 1.)

Pin set 2 repeats the format of pin set 1. For further discussion of parametric testing, refer to Section 4.

All the parameter input fields are alphanumeric (up to 4 characters including a decimal point). V1 and V2 must be positive while V3 must be negative. All other voltage fields accept the +/- option. Values for current should be specified without sign, since current polarities are determined from associated voltage conditions by the software. Certain parameter fields include a scroll option field for choice of units.

To enter any parameter in an input field, type in the desired number with the sign (according to the restrictions explained above). If the unit is not correct, use the [CHANGE UNIT] key to scroll to the correct unit before pressing the [ENTER] key to input the data and open the next field.

Refer also to paragraph 4.3.

3.7.4 Alternate Parameters Screen Figure 3-18

The alternate parameters screen is called by the keyboard command [SHIFT][ALTERNATE PARAMETERS] and

PARAMETERS Group 1 74LS161A			
SUPPLIES Step 0005			
Voltage	Test Limit	I-max	
V1= 5.25 V	I1= 32.0mA	100. mA	
V2=	I2=		
V3=	I3=		
S1		Param	Func
IIL 400. µA	@VIL 400. mV	800. mV	
IIH 20.0µA	@VIH 2.70 V	2.00 V	
VOL 400. mV	@IOL	4.00mA	
VOH 2.70 V	@IOH	400. µA	
IZL	@VZL		
IZH	@VZH		
IOS 20.0mA	100. mA @VOS	800. mV	
S2		Param	Func
IIL 800. µA	@VIL 400. mV	800. mV	
IIH 40.0µA	@VIH 2.70 V	2.00 V	
VOL 400. mV	@IOL	4.00mA	
VOH 2.70 V	@IOH	400. µA	
IZL	@VZL		
IZH	@VZH		
IOS			

Figure 3-17. Parameters screen, example for 74LS161A. On the first line, the system automatically displays the name entered in the describe screen. On the second line, STEP specifies the truth-table step number where DUT currents are measured at the power-supply pins and compared to the TEST LIMITS I1, I2, and I3, I-MAX values are the power-supply shutdown specs, beyond which current at any step will abort the entire test. Under pin sets 1 and 2, parametric test conditions go in the second column, test limits in the first column. However, for functional tests, the driving parameters go in the third column (input voltages, output currents) and the two output voltage levels that demark low and high logic states go in the first column. The VOS entry is properly part of the second column, but is displaced because IOS includes both lower and upper limits.

ALT PARAM Group 1 161A.7			
Parm Step 0000 to End		Parm Func	
Voltage	Test Limit	K1	K1
V1= 5.25 V	I1= 32.0mA	K2	K2
V2=	I2=	K3	K3
V3=	I3=	K4	K4
S1		Param	Func
IIL 200. µA	@VIL 400. mV	800. mV	
IIH 10.0µA	@VIH 2.70 V	2.00 V	
VOL 200. mV	@IOL	4.00mA	
VOH 4.50 V	@IOH	400. µA	
IZL	@VZL		
IZH	@VZH		
IOS 20.0mA	100. mA @VOS	800. mV	
S2		Param	Func
IIL 400. µA	@VIL 400. mV	800. mV	
IIH 20.0µA	@VIH 2.70 V	2.00 V	
VOL 200. mV	@IOL	4.00mA	
VOH 4.50 V	@IOH	400. µA	
IZL	@VZL		
IZH	@VZH		
IOS			

Figure 3-18. Alternate parameters screen, example for 74LS161A. The area shaded gray in this illustration (not shaded on the real display) is the area of data that cannot be entered or altered in this screen. (Do so on the parameters screen.) The unshaded area under S1 and S2 accommodate an optional min limit to be paired with the max limit on the parameters screen (conversely for VOH). None of the relays K1...K4 is selected for either parametric or functional tests. [Note: A few early 1732 systems lack the capability to set pairs (max/min) of limits for parametric measurements. Those systems recognize the single limit (parameters screen) as max or min, as is appropriate to the parameter.]

allows the user to specify an additional test limit for any of the parameters IIL, IIH, VOL, VOH, IZL, and IZH in both pin sets. Thus, in combination with the parameters screen, a means is provided for specifying a maximum and minimum test limit for any parameter except IOS, which has both maximum and minimum limits on the parameters screen. Initially, the screen displays the values that were specified on the parameters screen. Only those parameters listed above can be altered to specify additional limits — “max” for VOH, “min” for the others, i.e. larger and smaller values than are recorded on the parameters screen.

The alternate parameters screen also permits the user to designate inclusive truth-table steps and relay switching for each test group. Input specifications for these functions are as follows.

PARM STEP. Step number (in the truth table) at which parametric testing begins.

TO. Step number at which parametric testing ends. If no numbers are entered, the default values are 0 to “End”.

Two alphanumeric fields (up to 4 characters each). Only numbers 0 to 4094 or the letter E for “End” are allowed. Press [ENTER] to input the data and open the next field in each case.

PARM (K1...K4). K1 to K4 refer to the four relays that may be required to make special-purpose connections (as wired on the socket adaptor board). Selecting one or more of these options selects the relay(s) that you want energized during all parametric tests in this group.

Column of 4 enable-option fields. Press [CHANGE UNIT] to toggle the option. Press [up-arrow] or [down-arrow] to open the next field in this column. Press [ENTER] to open the next field outside this column.

FUNC (K1...K4). K1 to K4 refer to the four relays mentioned above. Select as required to make connections that you want made during all functional tests in this group.

Column of 4 enable-option fields. Data entry is the same as for parametric selection (above).

3.7.5 Group and Alternate Groups Screens

The data entered in any groups screen specify the test parameters for an additional group of the test program. When you press the [GROUPS] key or the [SHIFT] and [ALTERNATE GROUPS] keys, only the first line of the groups screen is displayed, showing an open input field at the group number position.

GROUP. Number indicating the group number of the parameters to be displayed.

Alphanumeric field (1 character). Only numbers 1 to n are allowed where n is the number that has been entered in the “# OF GROUPS” field of the describe screen. Type in a valid number to display the parameters; you need not press [ENTER]. If you press [ENTER] before the group number is entered, a default value of 1 is automatically entered as the group number.

Notice that pressing the [GROUPS] and [1] keys is equivalent to pressing the [PARAMETERS] key. Similarly, the command [SHIFT] [ALTERNATE GROUPS] [1] is the same as [SHIFT] [ALTERNATE PARAMETERS]. The parameter input fields are also the same as described for the parameters screen or alternate parameters screen.

The **first** time a particular group number is called for display, the parameter values specified for group 1 are automatically copied into the display and become the test parameters for this new group. [GROUPS] [n] copies values from the group-1 parameters screen; [SHIFT] [ALTERNATE GROUPS] [n] copies values from the group-1 alternate parameters screen. You can then alter the values as required, and the results will be preserved for subsequent calls to this group. Thus all higher numbered groups are modifications of group 1.

NOTE

This test system has established pairs of forced and measured parameters. If a device is specified with a force/measure pair that is inverted with respect to the 1732 norm, refer to the following explanation.

Normally, VIL is forced and IIL is measured, as shown in the parameters screen. However, some parameters are specified the other way around. For example, “input clamp voltage, VIK” is typically a specified range of voltage, measured when a certain current is forced. The method of programming the 1732 test system for such a specification is demonstrated by the following example.

The 74LS244 typically has a specification for VIK of -1.5 V at -18 mA . The current -18 mA is the condition; therefore one would prefer to force current and measure voltage. The voltage -1.5 V is a minimum, i.e., -1.4 V should pass but -1.6 V should fail.

To plan the program for this test, plan to force the marginal voltage (-1.5 V) and establish the specified current (-18 mA) such that the correct category of devices will pass. This current (-18 mA) must be a maximum limit so that all more-negative currents will pass. NOTE 1: -19 mA must pass because a device that draws -19 mA at -1.5 V would presumably drop something like -1.4 X V if forced to -18 mA . NOTE 2: very large negative currents, like -300 mA , must pass for the same reason. NOTE 3: the IIL limit which is entered on the parameters screen (normally referred to as a maximum) is really an absolute-value maximum; so it is a minimum in this case involving negative current. The true maximum limit in this example is entered on the alternate-parameters screen. It is important to program the limits as follows.

Assuming, for example, that the VIK test is to be done in group 5, call up the group-5 (parameters) screen; enter 200 mA for IIL and -1.5 V for VIL. (The sign of IIL is not programmable, but is automatically negative because VIL is negative.) Because the 1732 can measure IIL values only between -170 and $+170\text{ mA}$, this negative limit of -200 mA is effectively at negative infinity. On the group-5 alternate parameters screen, enter 18 mA for IIL. As explained before, this is effectively -18 mA , a maximum limit. (Note: if the measured value of IIL is -17 mA at -1.5 V , the test fails. Presumably, such a device, if forced with -18 mA would drop something like -1.5 X V , which is unacceptable.)

3.7.6 Truth-Table Screen

Figure 3-19

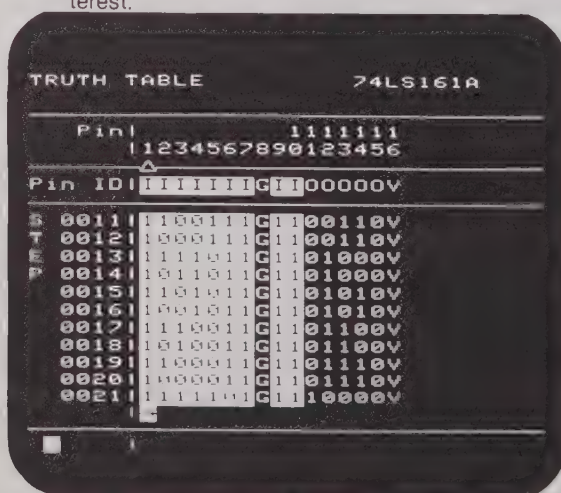
Press the [TRUTH TABLE] key to call up this screen. The heading automatically includes the program name and the full set of pin IDs as assigned on the describe screen.

The four basic types of entry in the truth-table screen are as follows. (See also paragraph 4.3.)

1. **Data line.** Defines logic state of DUT; carries a step number at left.

Any output pin will accept the entry [L] instead of a “common entry”. Use the L entry for any output state that you want to be defined automatically in the learn mode, using a known good device as DUT. (Any pin assigned to L should *not* be assigned a 0 or 1 logic state anywhere else in the truth table; only L or X; details in Section 4.)

1. A view of the truth table, centered on the line of interest.



3-22 OPERATION

2. A duplicate of that line in "edit" position, at the bottom.
3. A special cursor arrow above the edit line.
- b. To move the cursor, use [right arrow] and [left arrow] keys.

c. To change the indicated bit in the line, press [0], [1], [X], or if appropriate [SHIFT] [I/O], [T], or [L], as explained above. See Data Line Entries.

- d. To enter the edited line into the table, press [ENTER].

Insert. Basic command: "I" (used as follows).

Use this to displace any particular line in the truth table with another line that you will type in. The old line is NOT lost; it and the following lines all automatically take higher numbers to accommodate the new line. In step a below, [number] represents the old number of the displaced line, which becomes the new line's number. Be sure that the reverse-video block is showing in the corner of the screen before you enter the [I] and that the "I" is showing before you enter [number].

a. Press [I] [ENTER] [number] [ENTER]. The system responds by opening a field (with a cursor) in the correct columns for functional test details.

b. Enter [1] or [0], as desired, or (for pin type B or T only) enter [T] or [SHIFT] [I/O], in each position where the cursor points. If necessary to go back to previous entries, use the [DELETE] key.

c. After the new line has been completely written, press [ENTER] to insert it into the truth table.

The INSERT instruction "I" causes the inserted line to take the number following the "I" and every following step number is increased by one. For example, given a truth table that includes the following:

```
3  o o O o o O G o o O o o O V
4  o i O o i O G o i O o i O V
5  i i 1 i i 1 G i i 1 i i 1 V
```

You wish that after step 4, the truth table said

```
  i o O i o O G i o O i o O V
```

Because this is to come after step 4, the new line will be step 5. Therefore, key in (in EDIT mode):

```
I 5  i o O i o O G i o O i o O V
```

The new truth table will then look like this:

```
3  o o O o o O G o o O o o O V
4  o i O o i O G o i O o i O V
5  i o O i o O G i o O i o O V
6  i i 1 i i 1 G i i 1 i i 1 V
```

Note that the line that used to be step 5 is now step 6, and the inserted line is step 5, corresponding to the "I5" keyed in during the edit process.

If a command is inserted, the command will follow the step number. For example, if we take the "new" truth table above, and edit by the command:

```
I 3  W104
```

the truth table becomes:

```
3  o o O o o O G o o O o o O V
   W104
4  o i O o i O G o i O o i O V
5  i o O i o O G i o O i o O V
6  i i 1 i i 1 G i i 1 i i 1 V
```

Kill. Basic command: "K" (used as follows).

Use this to delete a particular command line only, leaving the associated data line intact. (Compare "delete", below.)

In step a below, [number] represents the number of that line. (For example, press [5] [6] for line 0056.) Be sure that the reverse-video block is showing in the corner of the screen before you enter the [K] and that the "K" is showing before you enter [number].

- a. Press [K] [ENTER] [number] [ENTER].

Delete. Basic command: "D" (used as follows).

Use this to delete any particular line in the truth table. If the particular line is a data line with an associated (following) command line, *both* are deleted. Notice that the association is always in this sequence: data, command. (Compare "kill", above.) In step a below, [number] represents the number of that line. (For example, press [5] [6] for line 0056.) Be sure that the reverse-video block is showing in the corner of the screen before you enter the [D] and that the "D" is showing before you enter [number].

- a. Press [D] [ENTER] [number] [ENTER].

New. Basic command: "N" (used as follows).

Use this to clear the truth table, i.e., to replace the entire truth table with another one that you will type out. Be sure that the reverse-video block is showing in the corner of the screen before you enter the [N].

a. Press [SHIFT][N][ENTER]. The system erases the displayed truth table and opens a field for a new one. The original truth table may be recovered by use of the Binary Code macro (see para 4.4.2).

b. Enter data lines as described above and command lines as described below, to provide the desired truth table.

c. After the new table has been completely written, including the "End" line (see below), press [ENTER] again.

Command Lines.

In general, command lines are truth-table program instructions other than data lines, and include such concepts as looping, calling a subroutine, waiting for a time interval, and demarking the end of the truth table. All are optional except the last one. Command lines are typed (and displayed) in code, as explained below. Each command line must follow one or two data lines. Do not attempt to type a command line as first line, nor to type two adjacent command lines.

Notice the difference between a truth-table "command line" (executed during a test of a DUT) and an "edit command" (to edit truth-table data and/or command lines.).

Jump. Basic command: "J" (used as follows).

Use this to cause the test program to jump from the present position in the truth table back (never forward) to a specified step designated "step number", proceed through the table forward to the present position, and repeat that loop a "rep number" of times before proceeding on to the next data line.

Be sure that you have two preceding data lines (completed with [ENTER]) before typing this command. Specifically, it is necessary to have a preceding step to which the jump goes and also to have *that* step preceded by a data line *without* any command line. (The system will display the command line with a space between the first two characters. Step numbers up to 4090 are acceptable.)

Jumps cannot be nested.

- a. Press [J] [step number] [+ / -] [rep number] [ENTER].

Subroutine. Basic Command: "S" (used as follows).

Use this to cause the test program to jump from the present position in the truth table to a specified step designated "step number", proceed through the table forward to a "return" command (see below), and then return to the present position and proceed to the next data line.

Subroutines can be nested, to a maximum depth of four.

Subroutines should be placed after the end "E" of the pertinent part of the truth table.

Be sure that you have completed the preceding data line (with [ENTER]) before typing this command. (The system will display the command line with a space between the first two characters; step numbers up to 4090 are acceptable.)

a. Press [S] [step number] [ENTER].

When subroutines are used, a "don't care" line (all Xs) must be placed after the end statement "E" and before the start of the subroutine. The subroutine call is not to the dummy line, but to the first line of the subroutine itself. A truth table might look like this, for example, from step 65 through the end of a subroutine:

```
0065  i i i o O G i 1 o o i v
0066  i o o o 1 O G i O i o 1 1 v
      S 70
0067  i i o o 1 1 G i O o i 1 O v
0068  o o o o O O G o O o o 1 1 v
      E
0069  X X X X X G X X X X X v
0070  i i i i 1 O G o O i i 1 O v
0071  o o o o O O G i 1 i i O O v
      R
```

Note that after step 66, we execute a subroutine starting at step 70, but step 69 has all Xs. (Without this line of Xs, the 1732 will stop at the "E" and fail to enter the subroutine.)

Return. Basic command: "R" (used as follows).

Use this to mark the end of the subroutine. (See above.) Be sure that you have completed the preceding data line (with [ENTER]) before typing this command.

. Press [R] [ENTER].

Wait. Basic command: "W" (used as follows).

Use this to cause the test program to wait at the present position in the truth table for "count number" of clock periods (normally one per step of the truth table) before proceeding on to the next data line.

Be sure that you have two preceding data lines (completed with [ENTER]) before typing this command. Specifically, it is necessary to locate the W command in the truth table so that the preceding data line has *no* associated command line. (The system will display the command line with a space between the first two characters; count numbers up to 4094 are acceptable.)

a. Press [W] [count number] [ENTER].

Zone. Basic command: "Z" (used as follows).

Use this as a debugging tool for test programs, especially for dynamic devices, by inserting a Z command after any data line (not already associated with a command line). Causes the test program to repeat continuously the zone of the truth table from step zero up to the Z command. (Acts like the J command with "step number" zero and an infinite "rep number".)

Be sure that you have completed the preceding data line (with [ENTER]) before typing this command. (The system will display the command line.

a. Press [Z] [ENTER].

End. Basic command: "E" (used as follows).

Use this to mark the end of the truth table and/or the end of a test sequence within the truth table. Be sure that you have completed the preceding data line (with [ENTER]) before typing this command.

a. Press [E] [ENTER].

Parametric testing (each group unique) and functional testing (all groups) can be started and stopped at any desired step numbers (up to 4090), the defaults being zero and "end." Any testing will stop at the pertinent stop step or any "E" command line encountered first. A truth table can have several "E" command lines; do NOT locate one (for any reason) earlier than the last parametric-test stop step, because parametric testing normally exercises the DUT from step zero to the pertinent start step; do place one at the very end of the truth table (as a precaution, after the last subroutine).

If your truth table is now complete, enter it into memory and exit from the edit mode by pressing [ENTER] [SHIFT] [EDIT].

3.7.7 Gate/Strobe Screen

Figure 3-20

Press [AUXILIARY] to obtain the "menu" of auxiliary screens. Use the [down-arrow] key to position the cursor at "Gate/Strobe"; press [ENTER] to obtain the gate/strobe screen.

The gate/strobe screen allows you to specify the timing in two independent sets of timing conditions, set A and set B. Timing is specified in 62.5-ns units of clock period. Input pins in each set will be driven at (essentially) the time of the corresponding "gate." Output pins in each set will be sensed at (essentially) the time of the corresponding "strobe."

Usually the sync clock (SYNC) is defined in the describe screen as a submultiple (C1...CF) of the clock frequency (C0). Accordingly, a call to the gate/strobe screen will show the frequency (Hz) under SYNC CLOCK and the period in units and seconds in the first row of the UNIT and SEC columns, respectively. The first open input field will be in the UNIT column of the gate timing line, set A.

UNIT. However, if the sync clock was defined as external (EXT) in the describe screen, then the first open input field in the gate/strobe screen is at the first row in the UNIT column, and the sync clock must be defined here. This is an alphanumeric field. Type in the total number of 62.5-ns units in the sync clock period and press [ENTER] or [down-arrow] to input the value. This action will display the corresponding frequency (Hz) and period (seconds) and open the input field in the UNIT field of the gate timing line, set A.

Notice that, in the system specifications, units are called "ticks."

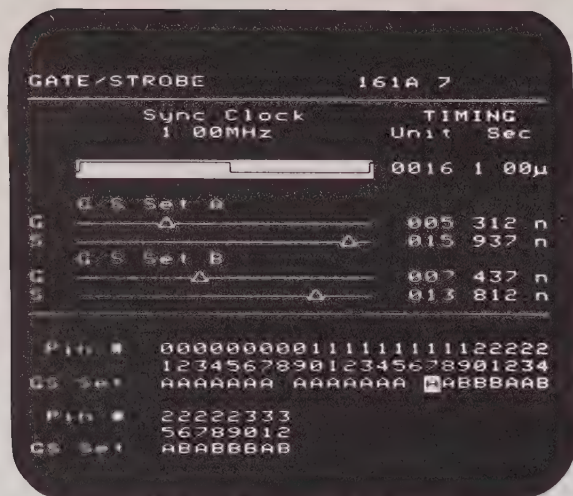


Figure 3-20. Gate/strobe screen example. Under "sync clock" is shown the frequency (see describe screen), from which the system derives the period (1 us) and number of 62.5-ns units (16) that are available for incrementing G and S. In this example, for set A, gate is set to minimum (5 units) and strobe to the max (15 units) for the sync clock, as shown graphically by pointer position and numerically under headings "unit" and "sec". Set B is similar, allowing you to choose different timing for specified pins. (To choose, either use [left-arrow] or [right-arrow] keys to move the pointer or enter the desired numerical values.) In the example, all pins except 8 and 16—which were assigned to ground and power supply—were at first defaulted to set A, until the program writer deliberately toggled certain ones to set B. (This screen can be ignored for most devices. The system then uses default values throughout.)

G/S SET A, G. The gate timing for set A is displayed as the value in the UNIT field and (at the same time) graphically as the position of the triangular pointer on the timing line. That is, movement from leftmost to rightmost position in 1-unit steps represents a linear increase from 5 units to two less than the total number of units in the sync clock period. Interaction between pointer position and the value in the UNIT field is automatic.

To specify the gate timing for set A, either type the desired number of units in the UNIT field, thus driving the pointer, or use the [right-arrow] or [left-arrow] key to position the pointer, thus incrementing or decrementing the value in the UNIT field. Press [ENTER] or [down-arrow] to input the desired value and open the next field. The timing in seconds is automatically displayed in the SEC column.

G/S SET A, S. The strobe for set A is specified and displayed similarly. However, "strobe" must be no less than "one unit larger than its companion gate", and no larger than "one unit less than the total sync clock period."

However, if the test involves changing any bidirectional or tristate pin from input to output function, make strobe no less than "two units larger than its companion gate," otherwise idle steps in the truth table (all outputs "don't care") are necessary to allow time for completion of such changes.

SET B. The above description applies also to timing for the gate and strobe in set B. This scheme permits you to position the four timing signals and view their relationships within the sync clock period. When first called, this screen shows default timing as 5 and 15 units for gate and strobe, respectively, for both set A and set B (except for sync clock less than 1000 ns, in which case, strobe is set automatically to conform to the rules below). The timing can then be altered as required within the following.

- Gate: 5 min to 312 max units
- Strobe: 7 min to 434 max units
- Strobe greater than gate
- Strobe less than total sync-clock units.

GS Set. This table assigns each DUT pin to either timing set A or B. Excepted are pins defined in the describe screen G, X, or Vi, which cannot be timed. Timing set A is the default for unassigned pins.

Table of scroll-option fields. Press [CHANGE UNIT] to toggle A to B, or vice versa. Press [right arrow] to move to a higher numbered pin. Press [ENTER] or another screen key to input the table of pin assignments.

3.8 MODIFYING A PROGRAM

Programs can be loaded from tape cartridge and modified with relative ease. While in memory, a program is completely accessible through the PROGRAM and SYSTEM SETUP MODES screens (provided, of course, the keyboard lock is NOT locked—see below), and any of the programmable variables can be altered by the data entry methods indicated in the pertinent screen descriptions.

To modify a program, simply perform steps a through g of Routine Operation (para 3.2) and proceed to call and alter the pertinent screens as required. An example of this procedure is given in steps e and f of Practice Exercise in para 3.2, where the user alters the system run and display modes of a particular program. Typically, you may wish to store some basic version of a program on tape and then alter the system modes as required, prior to run time. On the other hand, it may prove more efficient to store often-used versions in separate program files so they can be called and run immediately. The only requirement is that each program file name be unique. An example of this procedure is given in steps h through j of the Practice Exercise.

Table 3-6
TTL PROGRAM SERIES CONVERSION CHART FOR 74181

Series	Avail- ability	Iil	Iih	Vil	Vih	Parameter Vol	Voh	Izl	Izh	Ios
TTL	P									
TTL L	N									
TTL H	N									
TTL S	Y	X	X			X	X			
TTL LS	Y	X	X			*	X		X	X

P = Program is provided in the library.
Y = Yes, this device type is available on the market.
N = No, this device type is not available on the market.
X = A numerical change is required for this parameter.
* A more extensive change is required for this parameter.

3.8.1 Program Conversion

Modifying an existing program may be the most efficient means of developing a new but similar program. As an aid to the user, the 1732 Program Library includes with each prerecorded tape a parametric test plan or supplementary notes for developing additional programs from programs supplied in the library. Table 3-6 is an example.

From the above series of devices, only device type 74181 is programmed in the 1732 Program Library. For conversion to 74S181, you need only refer to the manufacturer's data sheet for the indicated parameters, and change them in the parameters screen or groups screen. The same applies for conversion to 74LS181, with the exception of the parameter VOL. In this case, the program-library documentation provides further information about any additional groups, functional steps, etc., required to test for VOL. For further information on program development, refer to Section 4 of this manual.

3.8.2 Keyboard Lock

Test programs can be protected from modification. A password-controlled software lock, called the keyboard lock, prevents any change to a particular program. It can be recorded on tape in the locked state, called, and used for testing, still in the locked state. This feature provides a measure of assurance that a test will be run in the manner intended, assurance that may be important in relation to quality control and security. The keyboard lock is controlled in the run-mode screen. See paragraph 3.6.

3.9 SOCKET ADAPTOR PREPARATION Figures 3-21, 3-22

3.9.1 Universal Socket Adaptor

The figures show a universal socket adaptor that has been prepared for a typical 40-pin DUT. Generally, preparation will require installation of jumpers to make the power supply, ground, and clock connections for a particular pin configuration of DUTs. Up to four relays and additional passive or active components can also be installed to apply special test conditions.

Power Supply Jumper. The power supply jumper is shown between PS1 and pin 40 of the DUT. The three power supplies PS1, PS2, and PS3 correspond to the

source voltages V1, V2, and V3 that should be identified in the describe screen and specified in the parameters screen; they can be jumpered to the DUT pins as required.

Ground Jumper. The ground jumper is shown between DUT GND and pin 20, which is the typical ground pin for 40-pin devices. DUT GND can be jumpered as required. Ground pins should be identified as "G" in the describe screen.

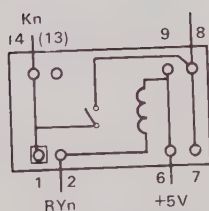
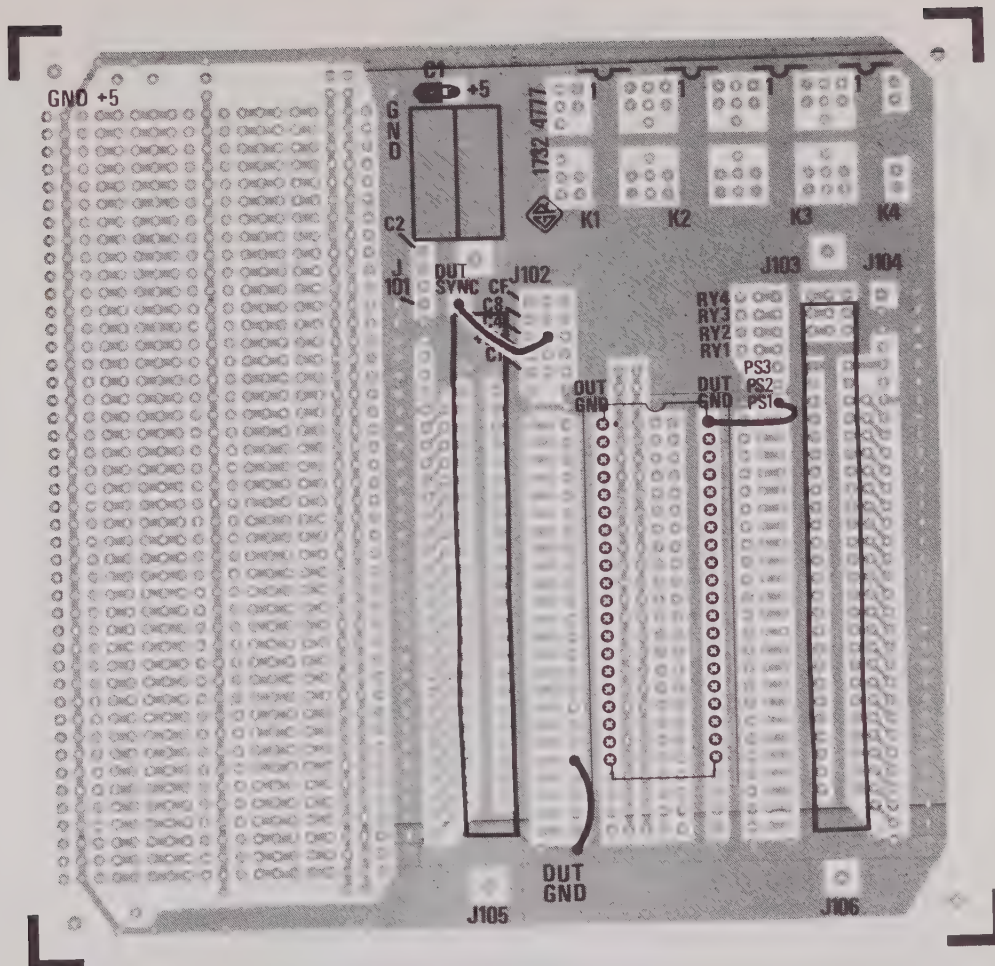
Clock Jumper. The clock jumper is shown between C4 and DUT SYNC. Clock frequency submultiples CO, CO/2, CO/4, CO/8, and CO/16 can be jumpered to DUT SYNC as required. When used, these options should be identified as C1, C2, C4, C8, and CF, respectively, on the describe screen.

Relay Installation. The socket adaptor board provides for installation of up to four relays (GenRad part no. 6090-2160 each or equivalent), powered by +5 V through the board. K1 through K4 are enabled by the signals at RY1 through RY4 on the board, which can be selected by options K1 through K4, respectively, in the alternate parameters screen. Relays can be installed and connected as required to apply special parametric and functional test conditions.

3.9.2 Socket Adaptor Fabrication

The 1732-9615 socket adaptor kit contains necessary parts, except sockets and receptacles, to assemble four universal socket adaptors. Compatible sockets and receptacles are listed in Table 1-4 and must be ordered separately. To assemble one complete socket adaptor, refer to the figures mentioned above and proceed as follows:

a. Inspect each of the four 32-pin connectors and notice that the pins are slightly shorter on one side than on the other. Install a connector in each of the four 32-pin locations labeled J101 through J104 on the socket adaptor board by inserting the shorter pins from the back (unlabeled side) of the board. Carefully solder each pin at the front of the board to secure the connector. With a multimeter, check that no pin is shorted to an adjacent pin or to ground. (The large etched area on the front of the board is ground and can be accessed at several points, including the topmost and bottommost holes on the left (front) side of the board.)



RELAY CONNECTIONS

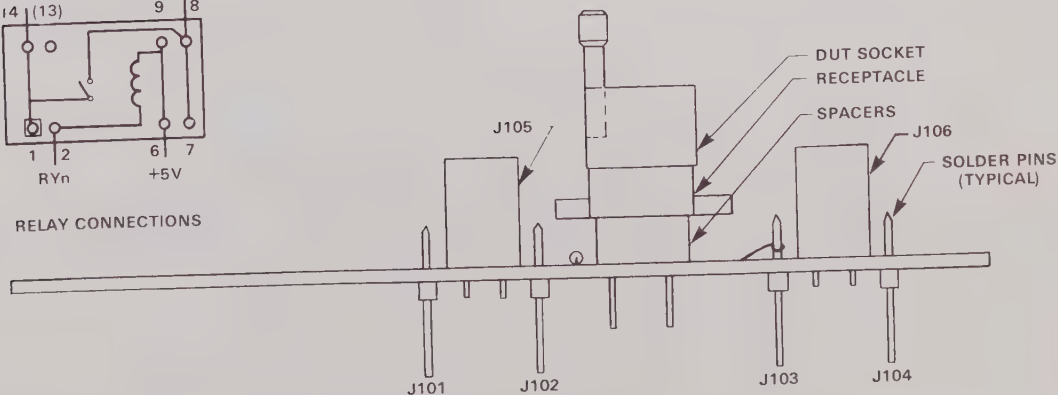


Figure 3-21. Socket adaptor board layout example, showing DUT socket outline, J105 and J106 outlines, and 3 jumpers in place. This board is supplied in kit 1732-9615.

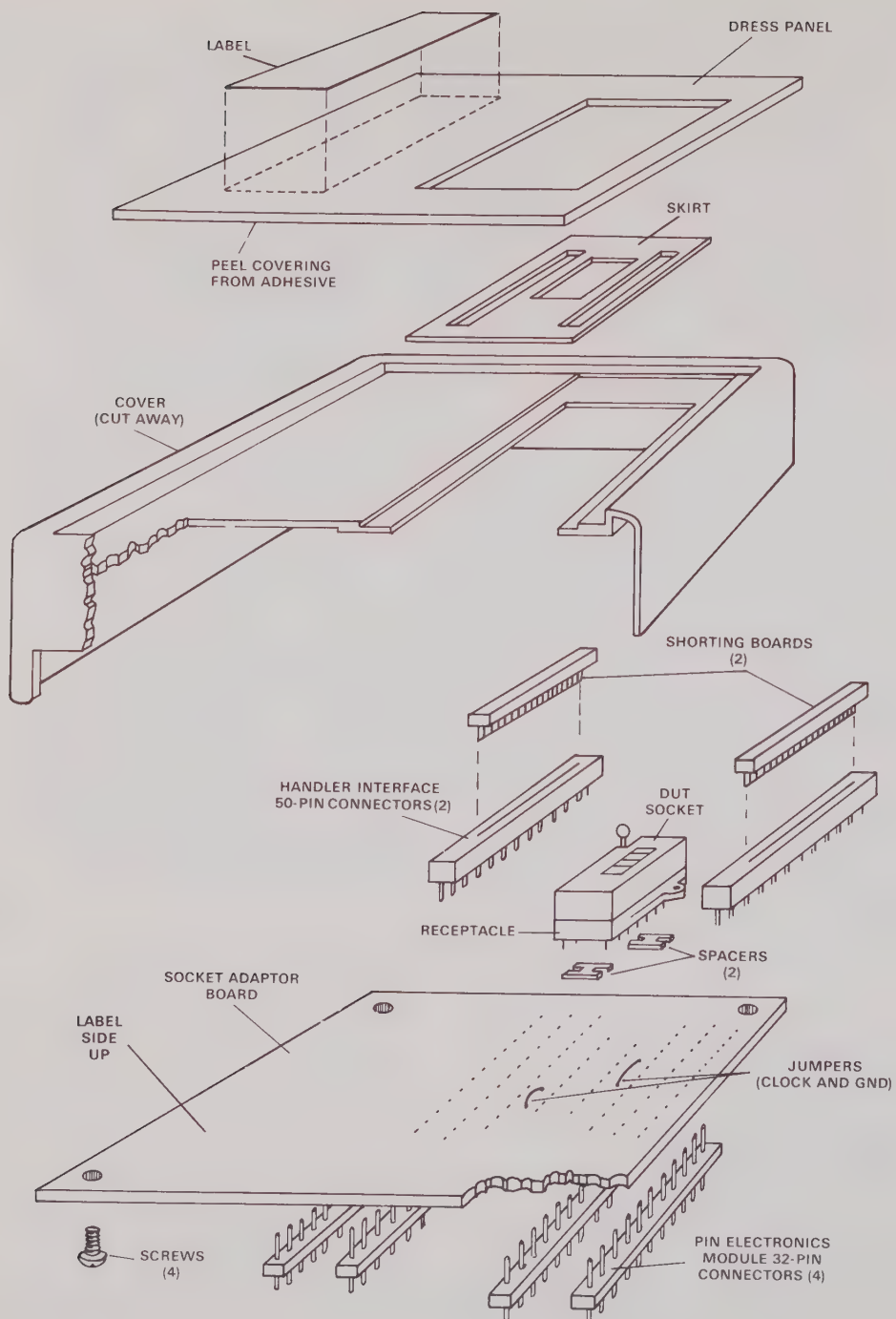


Figure 3-22. Exploded view of socket adaptor assembly including the circuit board and socket subassembly, which is shown in the preceding figure.

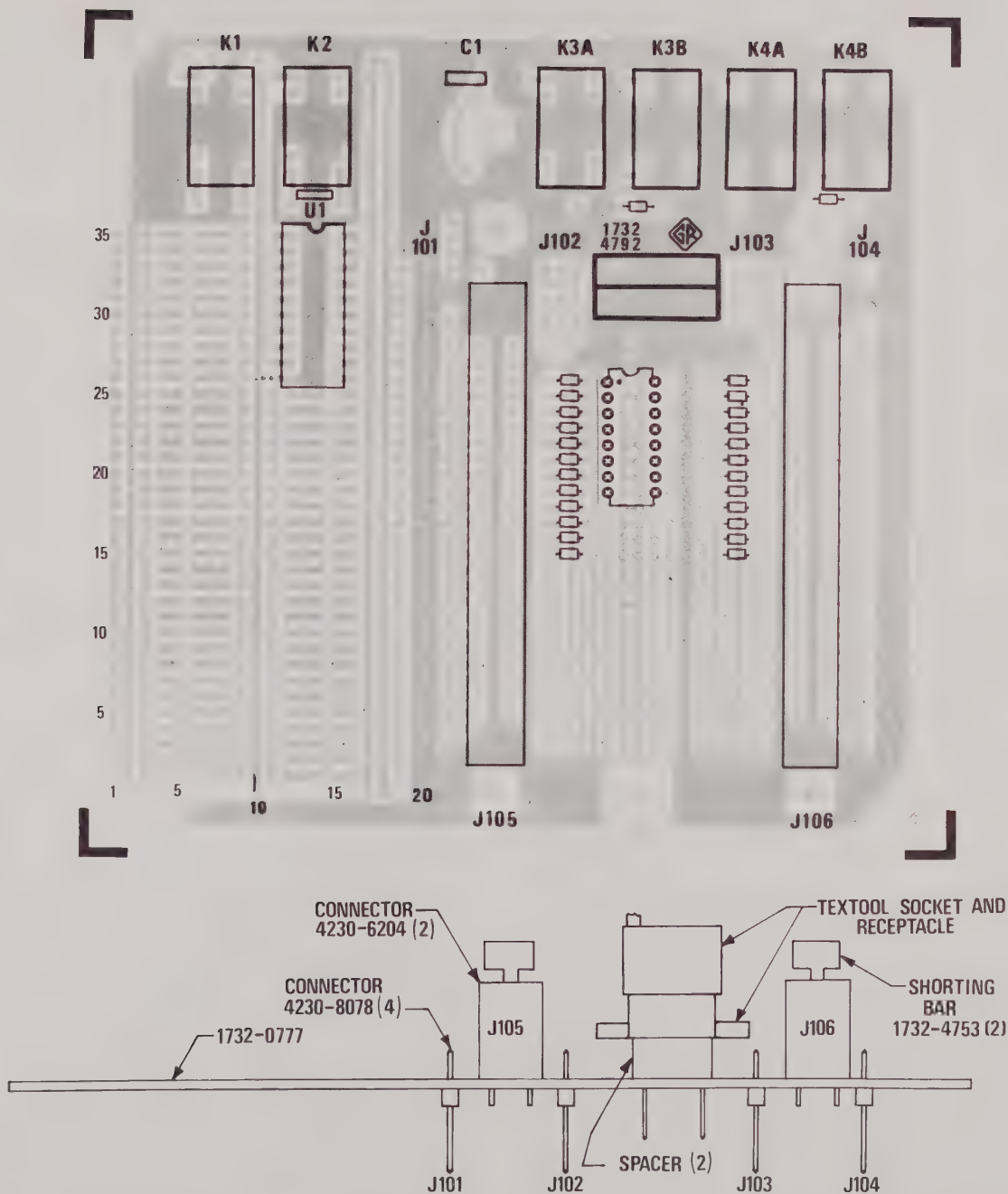


Figure 3-22A. Socket adaptor board example, showing DUT outline but no jumpers yet installed. Positions for 6 relays, J105, J106, and one IC (U1) are outlined. Ferrite beads (26 are shown) and perhaps capacitors may be provided, already installed. This board is supplied in kit 1732-9692.

b. Insert the two 50-pin connectors in the locations on the front side of the board labeled J105 and J106 and carefully hand solder them on the back side of the board. With a multimeter, check that no pin is shorted to an adjacent pin. On both connectors, only pins 1 and 2 should indicate a connection to ground.

c. Select a socket and receptacle appropriate for the device types to be tested with this socket adaptor. The socket is a lever-operated zero-insertion-force type. Two spacers from the socket adaptor kit are required to mount the receptacle so that, after complete assembly, the socket lever will have operating clearance. Insert a spacer over the next-to-last pin pair at each end of the receptacle (e.g., over pins 2 and 15, and 7 and 10 for a 16-pin socket). Position the DUT socket with pin 1 in the hole nearest the label "K1" in the leftmost row of holes (nearest J102) of the 5-row set of holes between J102 and J103, as shown in the accompanying socket adaptor board layout example. Insert the receptacle from the front of the board so that, when the receptacle is mated with the socket, the locking lever will be upper left, as shown in the figures. Solder the receptacle pins at the back of the board.

d. Press the socket into the receptacle so the two parts are properly mated. Remove the two small screws from the top of the socket and replace them with two longer screws (supplied with the receptacle) to secure the socket to the receptacle.

e. If the devices to be tested with this socket adaptor have stringent grounding requirements, one of the phosphor-bronze grounding springs supplied in the kit must be installed. Place the spring on the board with the grounding spring inserted in pin 8* of the DUT connector. Press the other end of the spring down onto the surface of the board and draw a line across the spring at the end of the board. Remove the spring and, with shears, cut off the spring on this line. Replace the spring in pin 8 of the DUT connector and solder the cut end carefully onto the exposed ground plane on the board.

f. Install jumpers, relays, and special components, as required. This information is supplied with the device library documentation. If a handler is not to be used, insert the two shorting boards (supplied) into J105 and J106. If a handler is to be used, set the shorting boards aside. J105 and J106 will receive the handler interface cables.

g. As shown in the figure, orient the assembled socket adaptor board so that the DUT socket and connectors J105 and J106 extend upward through the cut-out in the top of the cover, with the locking lever farthest from the cutout in the side of the cover. Align the four screw holes in the board corners with the bosses in the cover. Install four screws from the back of the board to secure the cover to the board.

h. Select and install, grained surface up, the dress panel (socket skirt) that fits precisely over the socket and into the lower step on the top of the cover. (A selection of socket skirt panels is supplied.)

i. Peel the covers from the adhesive strips on the larger (frame) dress panel and install the panel, adhesive down, on top of the socket skirt to secure it to the cover.

j. Type the proper socket adaptor identification (com-

patible device types, etc.) on the label supplied with the kit. Clean the place on the cover where the label will go; use alcohol for cleaning. Peel the covering from the adhesive, and affix the label to the socket adaptor.

3.9.3 Socket Adaptors for Program Library

Supplied with each tape of the 1732 program library is documentation that usually includes details for fabrication of the socket adaptor. Follow the general procedure given above. However, in certain cases, preassembled socket adaptors are recommended, which can be obtained from GenRad.

For an index to the program library, refer to the Index to Device Programs, supplied with the system.

3.10 SOCKET ADAPTOR CLEANING

For reliable connections, clean the socket-adaptor contacts as follows. (Neglecting to clean them eventually leads to apparent failures of good devices and erratic test results, typically differing each time the connector is separated and reconnected.)

a. Assemble these cleaning materials and equipment:

1. Reagent-grade isopropyl alcohol (isopropanol).

2. A small, clean, soft-bristle brush.

3. Compressed-air hose and nozzle intended for blowing dirt from machinery, or a squeeze-bulb blower.

b. Clean the pins of the socket adaptor as follows (unless they have been cleaned within a few hours) before mounting it on the pin electronics module. Brush alcohol onto the pins and dry them by blowing air directly on each pin.

c. Periodically, about every 15th time the socket adaptor is changed, clean the "ZIF" connectors of the pin electronics module as follows. With the contacts "open", brush alcohol across one connector so that some fluid penetrates the openings; then promptly blow air into all openings so that the alcohol is driven through. Repeat this procedure for each connector. Then continue to blow enough air to assure drying.

d. Clean the pins of any dirty DUT before insertion into the socket adaptor, as in step b.

e. Clean the DUT socket of the socket adaptor periodically, as in step c. The frequency required for this cleaning depends entirely on the overall cleanliness of the DUTs and the environment. If the system is in steady use, clean the DUT socket at least once a day.

3.11 CONVERSION ADAPTOR BOARD

Figure 3-23

The 1732-4778 adaptor is an interface between socket adaptors that directly fit 9700-series systems (2 connectors) and the pin electronics module of any system with four front connectors. Use this adaptor, for example, in the operation verification procedure (OVP) described in the service manual, Section 2.

3.12 DYNAMIC RAM SOCKET ADAPTOR AND TESTING

Figures 3-24 thru 3-26

3.12.1 Introduction

For testing random access memories (RAMs), we recommend use of a factory-assembled socket adaptor. The 1732-9617 socket adaptor has been designed specifically for use in testing dynamic RAMs. This adaptor tests the popular 4K, 16K, and 64K address multiplexed RAMs. It is shipped from the factory wired and configured for the MK4116, a 16K RAM. In order to change to other configurations such as 4K or 64K, a few jumper wires must be changed, as described below.

*On 16-pin DUT connectors pin 8 will be ground. Insert in appropriate pin in other DUT connectors.

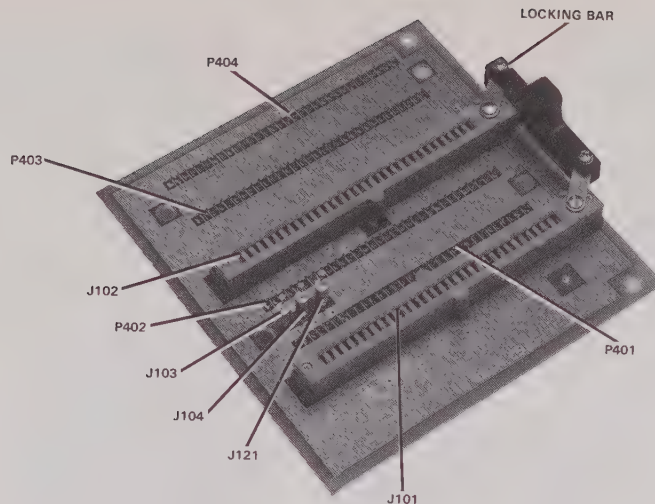


Figure 3-23. Conversion adaptor board.

3.12.2 Construction

The 1732-9617 socket adaptor uses a basic circuit board similar to that employed for the universal socket adaptor. Four connectors interface with the 1732 pin electronics module and carry drive, sense, voltage, and ground functions to the DUT.

The 1732-9617 adaptor contains suitable electronic circuitry. The four connectors on the back side of the adaptor mate with the four Kelvin connectors on the pin electronics module when the adaptor is installed. On the front of the board there are four blocks of wire-wrap pins labeled TB1, TB2, TB3 and TB4. Wire jumpers are used to configure the adaptor to the address scheme of the RAM being tested. These connections are detailed in paragraph 3.12.4. Also on this side of the board are two large black connectors (J105 and J106) which can be used to extend the DUT socket connections to an automatic handler. GenRad makes available custom interface cabling for most popular handlers.

Because of the active electronic circuitry required on the socket adaptor for testing the RAM, it is not possible to carry the Kelvin leads all the way through to an automatic handler. The actual Kelvin junctions are made in the RAM adaptor itself.

The 1732-9617 will accommodate DUT sockets with 0.3, 0.4, or 0.6-in. spacing. When soldering the device socket to the board, it must always be positioned in the holes to the far left and up.

3.12.3 Adaptor Circuitry

The block diagram describes this socket adaptor as supplied, configured for 16K RAMs. The only difference for other configurations is the number of address lines shown. A0 through A5 would be used for 4K RAM and A0 through A7 for 16K RAMs.

The addresses for the 4116 RAM are generated by a 14-bit counter, 7 bits for the row address and 7 bits for the column address. A two-into-one multiplexer is used to produce either the row or column address to the address inputs of the device under test (DUT). The RAS and CAS clocks, used to control the row address and column address strobes respectively, are produced by flip flops in the

timing control circuit. This timing is diagrammed with respect to the clock signal from the 1732. Other connections, such as DIN, DOUT and the read/write input, are made directly to 1732 driver/sensor (D/S) pins. It is important to note that all input/output pins of the DUT are disconnected from the adaptor circuitry during parametric tests. This is accomplished by CMOS switches, which isolate the adaptor electronics during parametric tests and then connect it during functional tests. Even though the 4116 is a 16-pin device, 24 D/S pins are required from the 1732. The "extra" D/S signals are needed to control timing in the adaptor. Table 3-7 lists the D/S pin number on the 1732 and its connection and function in the adaptor.

3.12.4 Conversions to Smaller or Larger RAMs

A set of jumpers on the board configure the socket adaptor for the size of RAM. Refer to Table 3-8 for details. Make the complete set of jumper connections required for the RAM to be tested. For example, the MK4116, MK4027, 2164, or 4164 RAM requires connections in the columns headed "16 K", "4 K", or "64 K", respectively.

3.12.5 Testing

Test programs are available from GenRad. Several 4 K dynamic RAM programs are available in the GenRad 1732 program library. These programs are directly compatible with the 1732-9617 socket adaptor if the jumper connections noted above are properly made.

Basically a test program such as that for the 4116 in the program library conducts tests in two distinct parts: parametric and functional testing. During parametric testing, the CMOS switches are opened to isolate the adaptor electronics (counters and timing circuitry) from the device pins. All pins are exercised for their high and low states while parametric measurements are made. Functional testing is performed by doing a march test through all RAM locations as follows:

- March through and write a 0 into each location as the counter increments through all address locations.
- March through, reading a 0 and then writing a 1 in each location.
- March through, reading a 1 and then writing a 0 in each location.

Table 3-7
FUNCTIONS OF DRIVER/SENSOR PIN CIRCUITS

D/S Pin No.	Signal Name	Function
1	-Reset	Resets counters to zero
2	-CON ADPT	Connects adaptor electronics to the DUT, for functional tests
3	+ CNT DWN	Control for "count down" on counter
4	-CNT ENB	Enables counter
5	-CYC ENB	Cycle enable for timing generator
6	X	Not used
7	Write-Low	Writes data to the RAM
8	Data In	Data into the RAM
9	Latch Data	Latches output data from RAM
10	Data Out	Data out from the RAM
11	RAS L	Row address strobe to the RAM
12	CAS L	Column address strobe to the RAM
13	X	Not used
14	X	Not used
15	X	Not used
16	X	Not used
17	A0	Address input 0 to the RAM
18	A1	Address input 1 to the RAM
19	A2	Address input 2 to the RAM
20	A3	Address input 3 to the RAM
21	A4	Address input 4 to the RAM
22	A5	Address input 5 to the RAM
23	A6	Address input 6 to the RAM
24	G	Ground

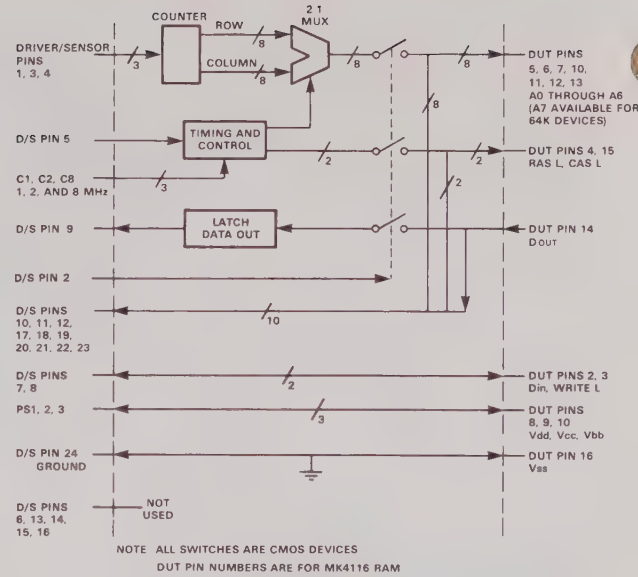


Figure 3-24. Dynamic RAM adaptor 1732-9617, block diagram. (See diagram 1732-4752-SD in service manual.)

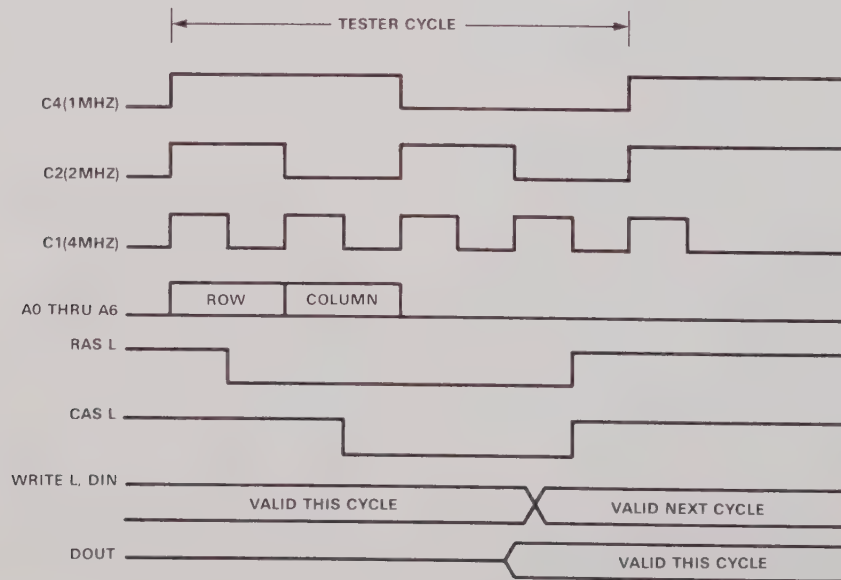


Figure 3-25. Timing diagram for 4116 RAM.

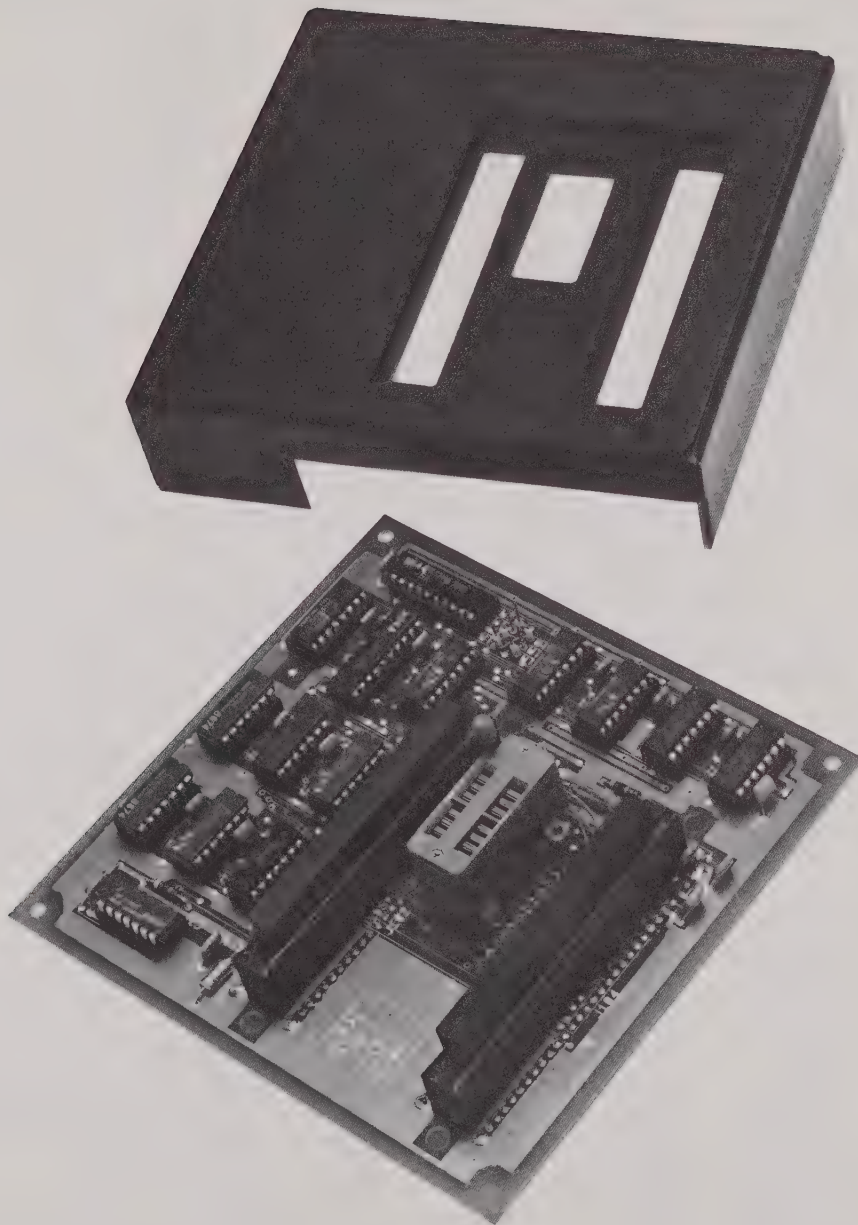


Figure 3-26. Dynamic RAM socket adaptor board and cover.

Table 3-8
ADAPTATION OF 1732-9617 FOR VARIOUS DYNAMIC RAM CONFIGURATIONS

Signal	From	16K (MK4416)* To	4K (MK4027) To	64K (2164) (4164) To
A0	TB1-1	TB2-5	TB2-5	TB2-5
A1	TB1-2	TB2-7	TB2-7	TB2-7
A2	TB1-3	TB2-6	TB2-6	TB2-6
A3	TB1-4	TB3-5	TB3-5	TB3-5
A4	TB1-5	TB3-6	TB3-6	TB3-6
A5	TB1-6	TB3-7	TB3-7	TB3-7
A6	TB1-7	TB3-4	---	TB3-4
A7	TB1-8	---	---	TB3-8
DATA IN	TB4-9	TB2-2	TB2-2	TB2-2
DATA OUT	TB4-8	TB3-3	TB3-3	TB3-3
RAS L	TB4-7	TB2-4	TB2-4	TB2-4
CAS L	TB4-6	TB3-2	TB3-2	TB3-2
VSS(GND)	TB4-2	TB3-1	TB3-1	TB3-1
VCC (+ 5) PS1	TB4-5	TB3-8	TB3-8	TB2-8
VDD (+ 12) PS2	TB4-4	TB2-8	TB2-8	---
VBB (-5) PS3	TB4-3	TB2-1	TB2-1	---
WRITE L	TB4-1	TB2-3	TB2-3	TB2-3
	TB3-2	---	TB3-4	---
Address	WT7	---	---	WT5
Selection	WT1	WT5	WT3	WT4
	WT2	WT6	WT5	WT6

*As configured by factory. For example, TB1 pin 1 is wired to TB2 pin 5; WT1 is wired to TW5.

Table 3-9
ADAPTATION OF 1732-9616 FOR VARIOUS STATIC RAM CONFIGURATIONS

Signal	From	2148/2114 (1K × 4)* To	2141 (4K × 1) To	EMM8108 (1K × 8) To	2102 (1K × 1) To
A0	TB1-1	TB3-5	TB3-1	TB3-7	TB3-8
A1	TB1-2	TB3-6	TB3-2	TB3-6	TB3-4
A2	TB1-3	TB3-7	TB3-3	TB3-5	TB3-5
A3	TB1-4	TB3-4	TB3-4	TB3-4	TB3-6
A4	TB1-5	TB3-3	TB3-5	TB3-3	TB3-7
A5	TB1-6	TB3-2	TB3-6	TB3-2	TB3-2
A6	TB1-7	TB3-1	TB4-2	TB3-1	TB3-1
A7	TB1-8	TB4-2	TB4-3	TB4-2	TB4-1
A8	TB1-9	TB4-3	TB4-4	TB4-3	TB4-2
A9	TB1-10	TB4-4	TB4-5	TB4-4	TB4-3
A10/DIO A	TB1-11	---	TB4-6	TB3-8	---
A11/DIO B	TB1-12	---	TB4-7	TB3-9	---
A12/DIO C	TB1-13	---	---	TB3-10	---
A13/DIO D	TB1-14	---	---	TB4-11	---
DIOE	TB2-1	TB4-5	---	TB4-10	---
DIOF	TB2-2	TB4-6	---	TB4-9	---
DIOG	TB2-3	TB4-7	---	TB4-8	---
DIOH	TB2-4	TB4-8	---	TB4-7	---
MUX/DIO0	TB2-5	---	TB4-8	---	TB4-6
CSL/CS**	TB1-15	TB3-8	TB4-9	TB4-5	TB4-4
WL/R**	TB1-16	TB4-9	TB3-8	TB4-6	TB3-3
DO0	TB2-6	---	TB3-7	---	TB4-5
+ 5V DUT	TB2-7	TB4-1	TB4-1	TB4-1	TB4-7
+ 12V DUT	TB2-8	---	---	---	---
-5V DUT	TB2-9	---	---	---	---
Ground	TB2-10	TB3-9	TB3-9	TB3-11	TB4-8
WT1 to WT2		Short	Open	Short	Short
WT3 to WT4		Open	Open	Short	Open
WT5 to WT6		Short	Short	Short	Short

* As configured by factory. For example, TB1 pin 1 is wired to TB3 pin 5; WT1 is wired to WT2.

** Signals that are active in the low or logic 0 state are generally identified by a suffix L as part of the signal name. The superscript bar is NOT used for this purpose.

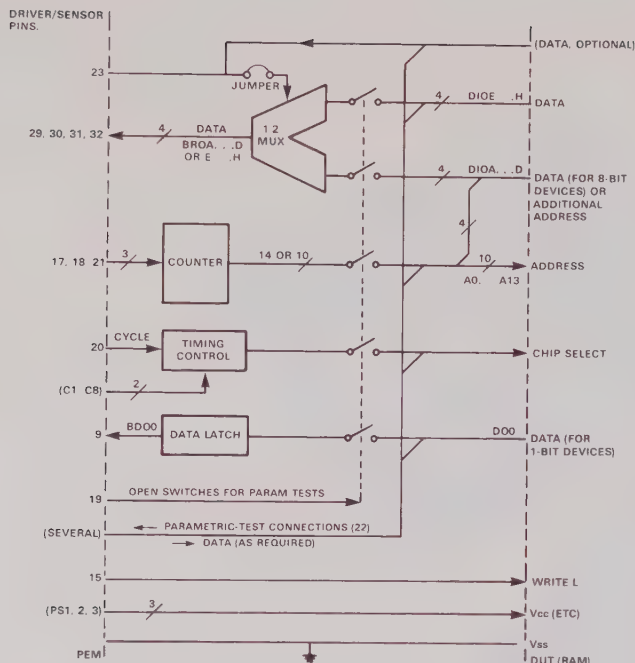


Figure 3-27. Static RAM adaptor 1732-9616, block diagram. (See diagram 1732-4751-SD in service manual.)

3.13 STATIC RAM ADAPTOR AND TESTING Figures 3-27 and 3-28

3.13.1 Introduction

The 1732-9616 is a fully assembled socket adaptor designed specifically for use in testing static random-access memory (RAM) on the 1732. This adaptor can be used for testing the popular address configurations such as $1K \times 4$, $4K \times 1$, $1K \times 8$, and $1K \times 1$. It is shipped from the factory wired and configured for the 2114, a $1K \times 4$ RAM. In order to change to other address configurations, jumper wires must be changed on the adaptor. Refer to paragraph 3.13.4.

3.13.2 Construction

The 1732-9616 socket adaptor uses a circuit board similar to that employed in the 1732-9617 dynamic RAM adaptor.

Because of the active electronic circuitry required on the socket adaptor for testing the RAM it is not possible to carry the Kelvin leads all the way through to an automatic handler. The actual Kelvin junctions are made in the RAM adaptor itself.

3.13.3 Adaptor Circuitry

Refer to the accompanying block diagram of the socket adaptor. In order to control the electronics of the adaptor, the number of drive/sense pins required for testing a device will always exceed the number of pins on the device itself. During parametric testing of the DUT, the electronics of the adaptor is disconnected from the device so that the dc parameters can be measured without any effect from the adaptor electronics. This is accomplished by CMOS switches which are open during parametric testing

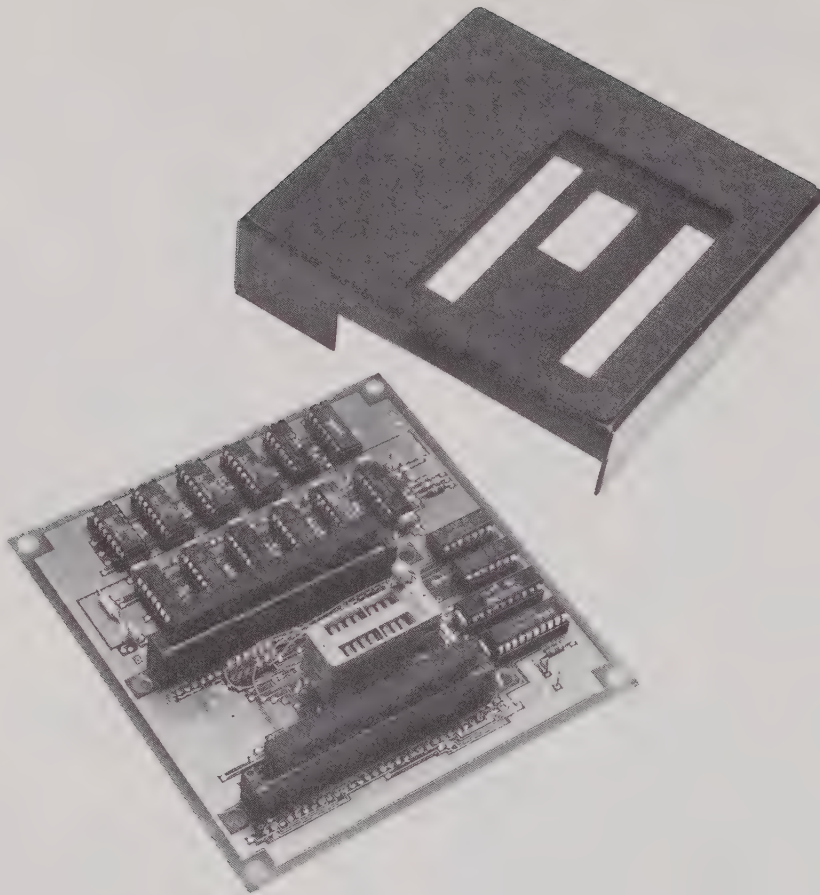
and closed during functional testing. A drive/sense pin is used to control these switches. Table 3-10 lists the 1732 drive/sense pin numbers, connections, and functions for testing a 2114 ($1K \times 4$) static RAM.

The addresses for a RAM under test are generated by a 14-bit counter, A0 through A13. It is important to note that the highest four address lines from the counter serve a dual purpose. They can be used for address inputs to the device or as data in/out lines. For RAMs that require addressing in excess of $1K$, where more than ten address lines are necessary, A10 through A13 could be used as address inputs.

For RAMs that contain more than four data I/O lines, A10 through A13 can be used as data lines. These eight data lines from 1732 drive/sense pins function as inputs when the tester is writing data into the RAM and function as outputs when reading RAM data out. When a RAM with eight-bit data is to be read, a two-into-one multiplexer is used to produce four bits at a time. This requires two steps in the truth table of the device test program. In one step, the four standard data I/O lines would be multiplexed through to the four BDO (Bus Data Out) lines and sensed by 1732 drive/sense pins. On the next step, the four address lines, now being used for data, would be multiplexed through and sensed. Static RAMs such as a $4K \times 1$ with only one bit of data, use the single latch for data transfer rather than the multiplexer.

Table 3-10
KEY TO SIGNALS ON DRIVE/SENSE PINS,
FOR 2114 STATIC RAM

D/S Pin on 1732	Signal Name	Function
1	A0	Address input 0 to the RAM
2	A1	Address input 1 to the RAM
3	A2	Address input 2 to the RAM
4	A3	Address input 3 to the RAM
5	A4	Address input 4 to the RAM
6	A5	Address input 5 to the RAM
7	A6	Address input 6 to the RAM
8	A7	Address input 7 to the RAM
9	A8	Address input 8 to the RAM
10	A9	Address input 9 to the RAM
11-14	X	Not used
15	WL/R	Writes or reads data to and from the RAM
16	CS/LCS	Chip select
17	RESETL	Resets counters to zero
18	CNT ENBL	Enables counter
19	CON ADAPT	Connects adaptor electronics to device
20	CYCLE	Input for chip select timing
21	UL/D	Control for count up or down on counter
22	X	Not used
23	V1	Supply voltage
24	X	Not used
25	DIO H	Data In/Out to and from RAM
26	DIO G	Data In/Out to and from RAM
27	DIO F	Data In/Out to and from RAM
28	DIO E	Data In/Out to and from RAM
29	BDO E	Latched data out from RAM
30	BDO F	Latched data out from RAM
31	BDO G	Latched data out from RAM
32	BDO H	Latched data out from RAM



Timing circuitry is built into this static RAM adaptor for controlling its data latches and chip select to the device. The 1732 system clock, divided by eight, is used to increment the address counter. This means that the frequency of the functional truth-table testing is conducted at 1/8 the clock frequency specified on the describe screen.

3.13.4 Address Conversion

The 1732-9616 static RAM adaptor is shipped factory wired for a 2114 static RAM (1K × 4). For other address configurations, refer to Table 3-9 and connect the TB and WT jumpers as specified.

3.13.5 Testing Techniques

Basically a test program, such as that for the 2114 in the program library, conducts tests in two parts: parametric and functional. During parametric testing, the CMOS switches

are opened to isolate the adaptor electronics (counter, timing circuitry, and data latches) from the device pins. During parametric testing, all pins are exercised for their high and low states within the specified parametric start, stop truth table steps. During functional testing, all CMOS switches are closed to connect the adaptor electronics to the device. The device control lines, such as Chip Select, Write Enable, etc., are first exercised for a function verification. Then march tests are performed to verify the read/write ability of the RAM. This is usually done as follows:

- a. March through and write a 0 into each location as the address counter increments through all locations.
- b. March through, reading the 0's and then writing 1's into each location.
- c. March through, reading the 1's and writing 0's into each location.

Figure 3-28. Static RAM socket adaptor board and cover.

Programming – Section 4

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4.1 GENERAL

This section presents guidelines for programming the 1732 Digital IC Test System. It is assumed that the user has a clear understanding of how the system operates (refer to Section 3), and it is recommended that Section 6 be read prior to actually programming a device. Primary emphasis will be given to filling in program worksheets, both with regard to system requirements and with application to a number of representative device test programs. Program worksheets are supplied at the end of this section and in the Sample Programs Manual as follows:

- Describe screen worksheet
- Parameters screen worksheet
- Alternate parameters screen worksheet
- Truth-table worksheet
- Run-mode screen worksheet

Notice that each worksheet is an expansion of one of the video display screens described in Section 3, and thus reflects the input requirements for that screen. Together, these screens comprise the necessary framework and, with their inputs, the necessary specifications for completely structuring a device test program. The “screen-image” organization of the worksheets produces a program plan that is ready for direct keyboard entry.

Essentially, the programmer's first task is to learn how the device under test (DUT) operates, by carefully studying the manufacturer's data sheets. The programmer can then proceed to plan the test program by filling in the worksheets. Because the basic program structure is supplied by the menu-type format of the program function screens, no programming language is required. The necessary descriptive, parametric, and functional specifications can be derived from the manufacturer's data sheets.

In the process, however, the programmer will require a fundamental understanding of how the system performs functional and parametric tests and how the specifications that are entered into the screens control their execution. This information and related guidelines are presented in the following paragraphs, first by considering basic test

structure and program specifications in their most general application, and then by discussing a series of program examples for particular device families or types.

4.2 BASIC TEST STRUCTURE

Device tests are organized into groups (up to 6) and types (up to 3) which are separately specified and executed. Each test group can include one, two, or all three types of tests: continuity, functional, and parametric. The number of test groups is defined in the describe screen and the order of test group execution is determined by the consecutive group numbers in the parameters screen and groups screens. The selection and order of execution of types of tests for all groups are defined in the run-mode screen.

Although separately structured, both functional and parametric tests use the functional pin electronics and the truth table. Further discussion of type test structure follows.

4.2.1 Functional Pin Electronics

Figure 4-1

The voltage and current levels referenced in Figure 4-1 are defined in the parameters screens where the programmer should specify VIH, VIL, IOH, and IOL as functional test conditions and VOH and VOL as test limits (refer to para 4.3).

During functional testing, DUT input pins are forced to high (VIH) or low (VIL) voltage levels, as required by the truth table. DUT output pins are connected via the diode bridge to two current supplies. When the output logic level is either high or low, the current supplies sink or source a corresponding current load IOH (at high level) or IOL (at low level), while the functional error logic senses the output voltage level as high (1) or low (0) with respect to reference levels VOH and VOL. However, when the output is in a high-impedance (“off”) state, the diode bridge balances so that the DUT pin floats to a mid-range value approximately equal to (VOH + VOL)/2 (i.e., the DUT output { Vout } is less than VOH and greater than VOL). The functional error logic senses this output as neither high nor low, but as high-impedance or tristate (T). A more

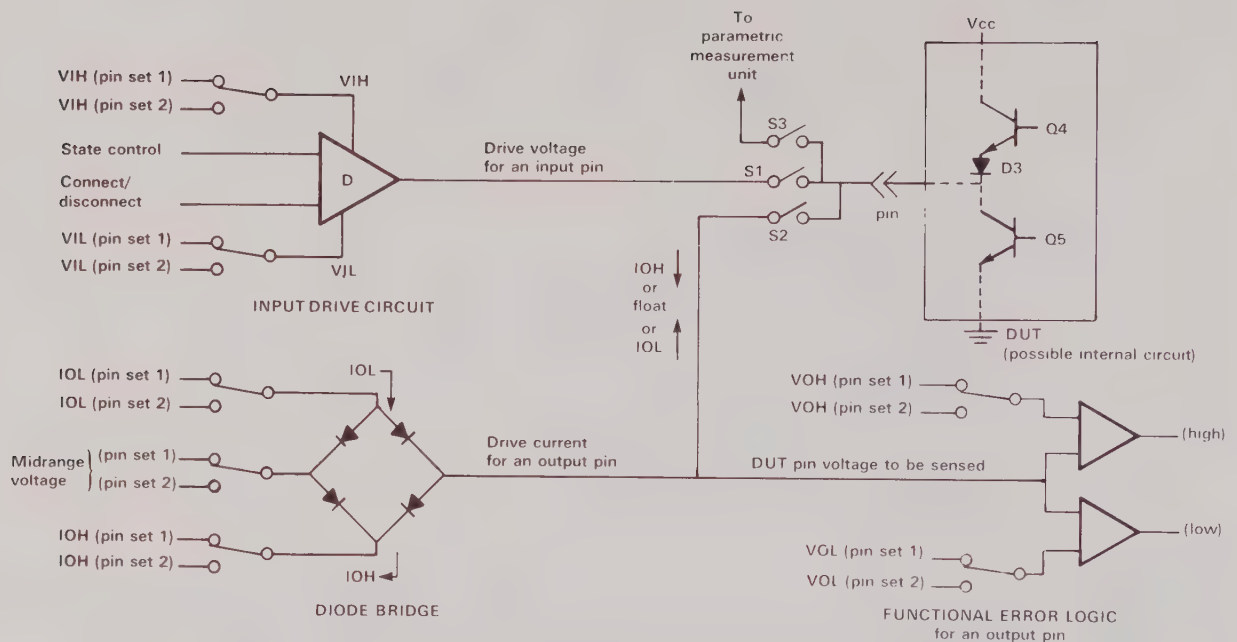


Figure 4-1. Functional-test pin electronics, simplified diagram. All switches are semiconductor types. S3 represents a pair of semiconductor switches; there is both a drive and a sense line connecting the pin to the parametric head. All pin set 1/pin set 2 switches are changed together and remain closed throughout testing of the pin. For functional testing, the appropriate switch S1 or S2 is closed; S3 remains open. For parametric testing, the appropriate switch S1 or S2 is closed while the DUT is brought to the desired logic state; S1 and S2 are opened and S3 is immediately closed.

detailed discussion can be found in Section 6, where the theory of the active load is described.

4.2.2 Functional Testing

The truth-table screen defines the order and patterns of stimulus and expected response that the functional electronics will generate. The voltage levels and current loading for these tests are specified in the parameters screen and groups screens. Functional testing applies to all DUT pins defined in the describe screen as I (input), O (output), B (bidirectional), or T (tristate). These pins will be tested either as inputs or as outputs, as follows.

Input (I) and output (O) pins retain their functions as defined in the describe screen. Bidirectional (B) and tristate (T) pins have their functions defined as input (code in reverse video) or output (code in normal video) in each step of the truth table. The default of bidirectional and tristate pins is always defined by the system as an output. Once the function is changed by the [I/O] key, the pin will remain in the newly designated function until the [I/O] key is used again to change it. Additionally, bidirectional and tristate pins coded X ("don't care") and tristate pins coded T (high-impedance) are all treated as outputs and the functional results are ignored.

Functional test steps are executed at the predetermined delay (Gate) from the positive-edge of the clock pulse at the sync-clock frequency by simultaneously applying the indicated conditions or measurements at all pins under test, as follows:

1. Apply a high-level (VIH) or low-level (VIL) voltage at each input pin.
2. Apply current load IOH (at high level) or IOL (at low level) at each output pin. The output voltage level with respect to mid-range $(VOL + VOH)/2$ determines

whether the current load is sink (IOH) or source (IOL) with respect to the DUT.

3. Compare the voltage level at each output pin with high-level (VOH), low-level (VOL), and high-impedance ($VOL < V_{out} < VOH$) reference voltages to sense a high (1), low (0), or high-impedance (T) logic state, respectively.

When a pin defined as an input is coded X in the truth table, the voltage driver is placed in the high-impedance state and the level at the pin is allowed to float (at step 1, above). When a pin defined as an output is coded X in the truth table, the pin definition in the describe screen dictates the loading and any result, whether high, low, or high-impedance, is ignored. During the power-supply test, however, at the specified power-supply test step, outputs coded X cause the active functional load to be disconnected. This unloads the output for static power-supply current measurement.

NOTE

The use of "X" entries on input pins, in conjunction with very small values of functional IOL/IOH, can cause high-frequency oscillations to draw excessive current, shutting down proper supplies. For this reason, insofar as possible, avoid putting "X" entries on input pins.

For every group, a functional test will cycle through the truth table once from the first to the last step designated for functional testing in the run-mode screen. (Default is step 0 to end.)

Pins defined in the describe screen as CI, G, or X are not tested functionally or parametrically. However, a pin defined as VI is tested parametrically, for power-supply current, but not functionally.

4.2.3 Parametric Testing

Parametric testing proceeds according to the order of the parameters specified for measurement in the parameters screen of each test group, beginning with the power-supply tests, then the inputs, outputs, and leakage current tests, and finally the IOS test. The test proceeds from the lowest numbered pin defined for a given function to the highest numbered pin for each parameter. Testing for each parameter continues until every appropriate pin has been tested once in the required logic state, as indicated by the truth table, or until the last test designated for parametric testing has been reached. (Refer to para 4.3.3, Alternate Parameters Screen Worksheet, Inclusive Test Steps.)

The system uses the functional electronics to cycle through the truth table. Inputs are forced and outputs loaded in the manner described for functional testing, except that functional error results are ignored. At the same time, the program checks the truth table at the test step being applied. When the desired logic state for a particular pin is found in the truth table, the pin is disconnected from the functional electronics and connected to the parametric measurement unit, which then forces the required parametric test condition at the pin and measures the parameter, as defined for the associated test group and pin set.

The values entered for the test limits and parametric conditions in each parameters group screen cause the parametric measurement unit to select one of 3 current-limiting resistors. If a voltage is being forced, the value entered in the parameters group screen for the parameter being tested causes the selection of one of 3 voltage ranges. These two selections are changed automatically by the system if the entries for the various parameters in a parameters group screen require different ranges of current or voltage.

To measure IIL (input current at low level), for example, the system checks the logic state of all input pins. This includes all pins defined as input (I) in the describe screen, as well as bidirectional (B) and tristate (T) when they are defined as inputs (reverse video) in particular steps of the truth table. The test cycle begins at step 0 of the truth table and proceeds to the first occurrence of a low logic state at the first input pin. The parametric unit then forces VIL, the low-level input voltage, at the pin and measures IIL. (Alternatively, if no low is found, the cycle continues through the last step designated for parametric testing in the alternate parameters screen; refer to para 4.3.3, Alternate Parameters Screen Worksheet.) To test the next input pin, the system restarts the functional cycle at step 0 and repeats the process, recycling for each input pin until all have been checked or tested once in the low logic state.

The remaining parameters of the group for which test limits and parametric conditions have been specified are measured in a similar manner.

It is important to realize that parametric testing is very dependent upon the truth table. The system forces the logic states it finds in the truth table and looks only for

those states listed in the truth table for the outputs. In essence, the system tests for the logic states it is told to test, whether or not the DUT produces those states for the inputs supplied. The programmer should structure test steps to include the logic states required for testing the indicated parameters. If a low is required but never programmed at a particular pin, for example, the system searches from the first step to the last step of the truth table (or to the last step designated for parametric testing in the alternate parameters screen) and, leaving that pin untested by default, proceeds to the next pin. If a pin is to be tested, it must have both a test condition and a test limit specified. For example, if IIL is specified but VIL is not, IIL will not be tested. The parametric results display will show a blank at a particular pin for any parameter that is left untested at that pin.

For a power-supply test, the programmer must specify the truth-table step that defines the desired state of the DUT pins (normally specified in the manufacturer's data sheet). As for other parametric tests, the system begins at step 0 and cycles to the specified step before connecting the parametric unit and measuring the current from the appropriate power supply. (The power supply is identified by describe screen and parameters screen entries.)

When selected in the run-mode screen, a continuity test is performed by the parametric unit once each time a program is executed prior to the testing of the first group. The continuity test automatically checks all power-supply, input, and output pins. Clock, ground, and "don't care" pins are not tested. A power-supply (positive or negative) pin is checked by sinking from or sourcing to it a current of approximately 100 μ A. The current direction is defined by the power supply being used. An input or output pin is checked by sinking from or sourcing to it a current of about 100 μ A to forward-bias its protection network. In each case, the magnitude of voltage measured determines whether there is continuity between the pin and the tester. (For details, refer to Measurement Theory, Section 6.)

4.2.4 Timing Sets

The test step repetition rate for functional testing is determined by the positive-edge sync clock frequency that the programmer selects in the describe screen (refer to para 4.3.1). This selection, in turn, defines the time frame for two separate timing sets, each generating a gate pulse and a strobe pulse. Basically, the gate determines when input conditions are gated to the DUT; the strobe, which must occur after the gate of the gate/strobe set, determines when DUT outputs are sensed by the system. Gate and strobe timing are independently programmable within certain limits which are defined in terms of the sync-clock time frame. Default timing for a 1-MHz clock rate is initially set as follows: gate = 5 ticks, strobe = 15 ticks or one tick less than the sync-clock period (whichever exceeds the gate by the smallest amount). If the selected sync-clock frequency is increased, the program automatically adjusts the default strobe so that it does not exceed its limit.

The gate/strobe settings are available to allow the system drive and sense timing to be adjusted around devices which have long propagation delays or output slew rates. Normally, the system runs with default gate and strobe settings which are identical for both timing sets and adequate for testing many devices. However, when

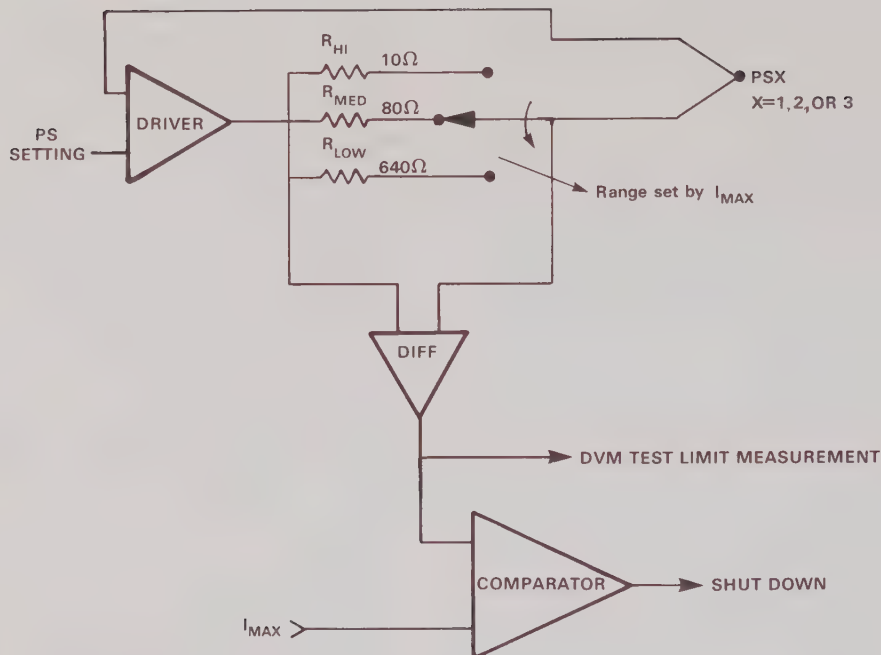


Figure 4-2. Power Supply Block Diagram.

DUT propagation delays are such that adjustments to the gate and strobe are critical, both timing sets can be programmed and selectively assigned to DUT pins in the gate/strobe screen.

For specifications and a graphical representation of gate and strobe timing, refer to Gate/Strobe Screen, in para 3.7.7. A detailed example of timing considerations for a particular CMOS device is given in para 4.9.4.

4.2.5 Pin Sets

The system provides two independently programmable sets of drive voltages, sense voltages, and sensor loads to set up each test group. Each DUT pin can be assigned to one of two respective "pin sets" by DUT pin selection in the describe screen (refer to para 4.3.1). The pin assignment remains fixed for all groups. However, the conditions programmed for a pin set in one group are independent of the conditions for the same pin set in another group. Parameters for each of the two pin sets are specified separately in the group screen (parameters screen worksheet, para 4.3.2) for each group of the test program.

4.2.6 Test Limit and I-max Selection

Figure 4-2

The system requires the user to select the appropriate power supplies for the DUT by means of jumper wires on the DUT socket adaptor board. Each supply has a different voltage range, allowing the selection of the ones most suitable for testing a particular device. Table 4-1 lists these ranges. In addition to specifying which supply (or supplies) will be used, two test values can be specified, one of which allows the system to limit current into the DUT. The first test value is the test limit (li); when this value is exceeded in a power-supply test, a test failure is sensed. If a value is not entered, the system will not perform a power-supply current-limit test. The second test value, I-max, must be

specified. It prevents excessive current flow by specifying an absolute shutdown current limit. Each power supply divides its output current into 3 ranges, as shown in Figure 4-2. This increases the resolution of low-current measurements beyond that which would be possible with a single current range. If this limit is exceeded at any time during system operation, it shuts down all three device power supplies.

Test limit (li) is selected to test for worst-case current conditions. In TTL devices, lccl and lcch are usually the heaviest current loads that the DUT places on the system, with the exception of IOS (see below). lccl is usually greater than lcch, so select the value of lccl for the test limit (li). In CMOS devices, Idd is usually the largest current load, while in ECL devices, lee is normally the largest. If the DUT draws more current than the specified value, it fails the test.

If I-max is the same as the test limit, i.e., if the test limit cannot be exceeded, the magnitude of the failure cannot be determined. At the same time, if the maximum current is not limited in some manner, a hard short can draw enough current to damage the DUT. In order to be able to determine the magnitude of the fault and yet still to protect the system from overload, I-max should be specified as follows.

Several factors need to be considered when selecting I-max, such as: DUT current supply load, the effects of output loading on the supply current, and dynamic loading of the supply current. For example, in a TTL device, lccl is usually greater than lcch, so it represents worst-case DUT current supply load. Output functional loading occurs when IOH is drawn from the power-supply rail through the DUT's output transistors. When more than one output is

Table 4-1
VOLTAGE RANGES

Device Power Supply	Range	Resolution	Accuracy (+/- % of setting)	Maximum Current
1	0 to +8 V	2 mV	(4 mV + 0.3%)	400 mA
2	0 to +19 V	5 mV	(10 mV + 0.3%)	160 mA
	+19 to +20 V	5 mV	(10 mV + 0.3%)	100 mA
3	0 to -7 V	2 mV	(4 mV + 0.3%)	160 mA
	-7 to -8 V	2 mV	(4 mV + 0.3%)	100 mA

high, IOH is drawn through each output. Thus, IOH (functional) times the number of outputs represents the worst-case output loading for a TTL device.

All these factors must be taken into account, yet they do not allow for any marginal devices. In order to provide this margin, the overall sum of these factors is increased by 25 percent. As an example, for a TTL device, the formula for I-max would be constructed as follows:

$$I\text{-max} = \{ I_{cc1} + [IOH(\text{func}) \times \# \text{ of outputs}] \} \times 1.25$$

This formula includes dynamic current loading in the 25 percent allowance for marginal devices. The I-max formula for CMOS devices calculates the dynamic current loading rather than lumping it in with the allowance for marginal devices (refer to para 4.9.3) as follows:

$$I\text{-max} = \{ [IOH(\text{func}) + [CL \times f(\text{sync}) \times V_{dd}] \times \# \text{ of outputs} + I_{dd}(\text{static}) + IOH(\text{para})] \} \times 1.25$$

The I-max formula for ECL devices is the simplest:

$$I\text{-max} = I_{ee} \times 1.25$$

4.2.7 High-Speed Controller Activity

When a test program is loaded into the system, the high-speed controller loads the truth table into the 4K × 4 memory which resides behind each pin on the driver/sensor boards. Once the test is started, the high-speed controller sends the address of each step of the truth table to the driver/sensor RAMs, causing the step to be executed. The RAMs place highs or lows on the drive lines, or highs, lows, or high-impedances on the sense lines, according to what is written in the enabled address. The high-speed controller performs this basic function in the functional, parametric, and power-supply tests.

Functional Testing.

The functional start step and stop step were defined in the run-mode screen. The start step tells the high-speed controller what address to generate to begin only the functional test. The high-speed controller then counts through the addresses until it reaches the stop step or an End command. The sync pin on the DUT board returns a clock pulse to the high-speed controller, causing it to generate the address for the next step of the truth table. Command lines modify the incrementing of the test pattern address. When the stop step or an End command is reached, the system stops functional testing and halts.

There are four command lines which will change the incrementation of the test step address. They are:

Jump ([J] [step number xxxx] [+/-] [rep number yyyy])

Subroutine ([S] [step number xxxx])

Wait ([W] [count number xxxx])

Return ([R])

Each command is described in detail in para 4.3.4.

Parametric Testing.

The PARAMETRIC STEP aaaa TO bbbb entries defined on the alternate parameters screen tell the high-speed controller what addresses to send to the driver/sensor RAMs to mark off the portion of the truth table within which parametric measurements are enabled. For parametric testing, the high-speed controller always starts at step 0000 and functionally executes the truth table at full speed, ignoring functional errors (if any), to step aaaa and beyond until the pin to be measured is in the appropriate logic state. Immediately, functional drives are frozen at that step. The pin being measured is now disconnected from the functional network and connected to the parametric measurement unit. After the test for that pin is completed, the high-speed controller resets its address register to 0000 and begins the next parametric test.

Power-Supply Testing.

If entries for TEST LIMIT (li) and SUPPLIES STEP have been entered in the parameters screen for the group under test, the high-speed controller begins executing the functional test from step 0000. It will stop at the step specified for power-supply testing and check to see whether the outputs have been coded "don't care" (X) for that step. If so, the outputs will be disconnected from the system; this allows for power-supply current testing with the outputs unloaded. If the outputs have not been coded X, the system will test the supply current with the outputs set as they are coded.

4.3 PREPARATION OF WORKSHEETS

While the following paragraphs put program data into a format that can be entered into either the worksheets or the system with equal ease, it is recommended that the worksheets be used. This will minimize the amount of time that the system will be dedicated to program development rather than on-line testing. Blank worksheets (one of each) are provided in this manual. These may be duplicated locally as necessary.

The program worksheets should be filled in in the following sequence: (1) describe screen, (2) parameters screens, (3) alternate parameters screens, (4) truth table, and (5) run-mode screen. It is important to realize, however, that these worksheets are interdependent and decisions on all program specifications do not necessarily fall in sequential order. Certain entries may be left blank on one worksheet until the requirements of a subsequent worksheet have been considered. It is suggested that the appropriate worksheet be removed from the manual and referred to while reading the paragraph on its preparation.

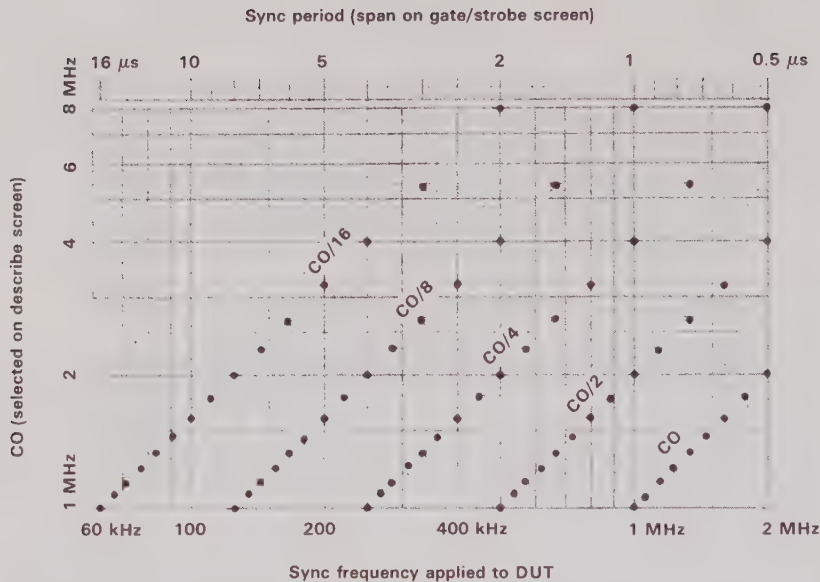


Figure 4-3. Sync frequency relationships. Using the C0 span of 1 to 8 Mhz, sync frequencies of 62.5 kHz to 2 MHz can be selected. Sync frequency is applied to the DUT; the truth-table steps are executed at this rate. The necessary divider selection (C0/2, C0/4, etc.) must be established by clock jumper on the socket adaptor. It is part of the program data and is indicated for reference on the describe screen.

4.3.1 Describe Screen Worksheet

Figure 4-3

The entries in the describe screen worksheet provide the initial description of the DUT, as "seen" by the test program.

Program Name and Comment.

Enter the PROGRAM NAME — generally, but not necessarily, the alphanumeric type designation of the DUT. The name, which can be up to 12 characters long, will be automatically stored as a header for the remaining program screens. The associated COMMENT of up to 15 characters is descriptive only and does not affect the test program.

Number of Pins and Number of Groups.

Enter the NUMBER OF PINS (up to 48), which can be taken directly from the manufacturer's data sheet.

Initially, the NUMBER OF TESTS GROUPS entry may be left at the software supplied default value of 1, although 6 is the system upper limit of the number of parameters screens available to the user for programming. This can be corrected to the number of groups actually required, after completion of the parameters screens worksheets. This value determines how many groups are available for programming.

Clocks.

Select a clock frequency of C0 and a sync clock frequency divider from the options listed on the worksheet. Timing data can be obtained from the voltage waveforms on the manufacturer's data sheets. If timing is not critical, the entries for clock and sync clock can be left to the default values of 4 MHz and C4, respectively, producing a 1-MHz clock frequency. Otherwise, the system provides fifteen clock frequencies (C0) ranging from 1 to 8 MHz, from which one can be specified. The sync clock, in

turn, must be implemented (by socket adaptor wiring of the clock to the sync pin) as a submultiple of the clock or as an external input.

Note that clock pins defined as inputs which receive the clock pulses must be wired to correspond to the selected code on the DUT socket adaptor board.

There is also the option of supplying an external sync clock. This is implemented by selecting EXT as the sync code and wiring the external clock directly to the socket adaptor DUT SYNC.

The system clock output is also available as a TTL-level 50% duty cycle clock to the DUT. If the DUT clock input is driven from the system clock and the system sync is driven from the same clock frequency, the following characteristics of clock operation should be noted for proper DUT timing. The positive-going edge of the clock pulse will be generated for both functional and parametric execution of the truth table, independent of the sync (C1 through CF) selected. The negative-going edge of the clock pulse is seen only during functional testing. Parametric tests halt the clock when it reaches the truth-table step where a test is to be performed. If syncs C2 through CF are selected, the clock will stop while in a logic-high state as the parametric test is performed. Sync C1 generates a negative-going edge for every positive-going sync pulse edge, regardless of whether a parametric or functional test is being performed.

NOTE

There are two ways to ensure having a negative-going edge where it is needed for parametric testing: use clock sync C1 or a repeat step. It may not be practical to use a repeat step with some LSI devices. If a step is to be repeated, proceed as follows. Enter

Table 4-2
1732 CLOCK FREQUENCY RELATIONSHIPS

To Obtain FREQUENCY AND PERIOD:			For a Sync Clock Selection of:				
			C1	C2	C4	C8	CF
			Select a Clock Frequency C0 (MHz)				
2.00	MHz	500 ns	2.00	4.00	8.00	---	---
1.78		562	---	---	---	---	---
1.60		625	1.60	3.20	---	---	---
1.45		688	1.45	---	---	---	---
1.33		750	1.33	2.66	5.33	---	---
1.23		813	1.23	---	---	---	---
1.14		875	1.14	2.29	---	---	---
1.07		938	1.07	---	---	---	---
1.00		1.00 μ s	1.00	2.00	4.00	8.00	---
889	kHz	1.12	---	1.78	---	---	---
800		1.25	---	1.60	3.20	---	---
727		1.38	---	1.45	---	---	---
667		1.50	---	1.33	2.66	5.33	---
615		1.63	---	1.23	---	---	---
571		1.75	---	1.14	2.29	---	---
533		1.88	---	1.07	---	---	---
500		2.00	---	1.00	2.00	4.00	8.00
444		2.25	---	---	1.78	---	---
400		2.50	---	---	1.60	3.20	---
364		2.75	---	---	1.45	---	---
333		3.00	---	---	1.33	2.66	5.33
308		3.25	---	---	1.23	---	---
286		3.50	---	---	1.14	2.29	---
267		3.75	---	---	1.07	---	---
250		4.00	---	---	1.00	2.00	4.00
222		4.50	---	---	---	1.78	---
200		5.00	---	---	---	1.60	3.20
182		5.5	---	---	---	1.45	---
167		6.0	---	---	---	1.33	2.66
154		6.5	---	---	---	1.23	---
143		7.0	---	---	---	1.14	2.29
133		7.5	---	---	---	1.07	---
125		8.0	---	---	---	1.00	2.00
111		9.0	---	---	---	---	1.78
100		10.0	---	---	---	---	1.60
91		11.0	---	---	---	---	1.45
83		12.0	---	---	---	---	1.33
77		13.0	---	---	---	---	1.23
71		14.0	---	---	---	---	1.14
67		15.0	---	---	---	---	1.07
63		16.0	---	---	---	---	1.00

“don't care” (X) for the pin of interest on the step of the truth table where the pin first appears in the desired state, and repeat the desired pattern in the next step. This will allow the sync to generate the negative-going edge, which is the transition necessary to perform the test.

The resulting sync clock frequency determines the test step repetition rate. The software will not allow an entry which exceeds the system limitation of 2 MHz set by the hardware. Additionally, the sync clock defines the time frame for the gate and strobe timing in both system timing sets (refer to Timing Sets, para 4.2.4). Whereas the default setting is generally adequate, gate and strobe timing

are critical for certain device types and, in such cases, should be considered in relationship with the sync clock entry. An example of gate and strobe timing for CMOS-B programming is given in para 4.9.4

Figure 4-3 and Table 4-2 present the clock frequency relationships provided by the system clocks. Table 4-2 is used to obtain a combination of clock frequency (C0) and sync clock that will result in a desired frequency. To produce a given frequency or period, read down the frequency or period column until the desired value is reached. Read across the line until a number (the clock frequency C0) is obtained in one or more columns (each column is a different sync clock divider).

As an example, assume a period of 2 μ s is desired. Read down the period column to 2 μ s, then read across to find a

clock frequency/sync clock divider combination. In this example, possible combinations are 1.0 MHz for C0 if C2 is used for the sync clock divider, 2.0 MHz for C0 if C4 is used for the sync, 4.0 MHz for C0 if C8 is used for the sync, and 8.0 MHz for C0 if CF is used for the sync clock divider. Note that the sync clock divider selected has to be hard-wired as a jumper on the DUT socket adaptor board, while the clock frequency is implemented by software. If it will be desirable to change the test frequency over a range of values, select a sync clock that will allow varying the frequency by varying only the clock frequency entry; this will reduce or eliminate the need to rewire the DUT socket adaptor board to accommodate a change in the sync clock divider.

Notice that clock frequencies higher than 2 MHz are available to allow flexibility in creating special interfaces for devices requiring complex timing or special device/tester synchronization. However, the software still restricts the clock frequency and sync relationship so that the selection must result in a sync clock frequency equal to or less than 2 MHz.

Pin Identification.

Enter the pin assignment for each DUT pin according to the manufacturer's data sheet, in the ID column, using the pin-ID code. Code definitions and notes are as follows:

1. I — input.
2. O — output.
3. B — bidirectional. Apply this definition to any pin that changes function from input to output, or vice versa, but does not enter the high-impedance (T) logic state during DUT operation. This allows the truth table to define the pin as either input or output ([SHIFT] [I/O] command), depending on device state, for each functional step.
4. T — tristate. Apply this definition to any pin that enters the high-impedance (T) logic state at any time during DUT operation. This also provides the same capabilities described for bidirectional pins.
5. X — "don't care." This electrically disconnects the DUT pin from the system pin electronics module during testing. The system sees the pin as a 200-pF load throughout the program.
6. V(1, 2, 3) — voltage source. From the Specifications in the front of this manual, select the device power supply that provides the voltage range required for the DUT. Enter V1, V2, or V3 to designate PS1, PS2, or PS3, respectively. Note that the code entered here must correspond to the voltage source specified for power-supply tests in the parameters screen worksheet to measure the current limit for the proper supply. Also, the assigned voltage-source pin must be wired for the designated device power supply on the socket adaptor board.
7. G — ground. Note that pins defined as G must be wired accordingly on the socket adaptor board. (As with pins coded X, pins coded G will be electrically disconnected from the pin electronics module.)
8. C(1, 2, 4, 8, F) — clock. Enter the code (C1 ... CF) for the selected submultiple of the clock frequency. See *Clocks* above. Note that pins defined as clock inputs must also be wired to correspond to this code on the socket adaptor board. (As with pins coded X, these pins will be electrically disconnected from the test pin electronics.)

Pin Set.

Assignment of pins to pin sets should be deferred until completion of the parameters screens. Then, if the use of a second pin set is required, enter a 2 in the S column to the right of the ID code to designate pins assigned to the second pin set. No more than two pin sets are allowed. Entering the default value of 1 for the remaining pins is optional. Pins defined as V, C, G, or X cannot be assigned to a pin set.

The S designation assigns each pin to either of two separate sets of test conditions, as will be defined in the parameters screen worksheet. There are two general reasons for separate pin sets:

1. Different functional requirements (VIL, VIH, IOL, IOH, VOL, and VOH) for the same parts (as in a level shifter, for example).
2. Multiple specifications for parameters to be measured. (refer to IIL and IIH specifications in the 74LS161A example program, para 4.8.4.)

Defining two pin sets allowed both conditions to be tested in the same test group. If separate conditions are required for more than two sets of pins, the additional conditions must be programmed in additional test groups. (Refer to Alternate Parameters Worksheet, para 4.3.3, and the tables there.)

4.3.2 Parameters Screen Worksheet

General.

This worksheet is organized into three sections, running from top to bottom. The first section defines the power-supply setup that will be used in that group's test. Values for voltage, current test limit (li), and shutdown current limit (I-max) can be specified for each of the three power supplies. The second and third sections are identical in structure. The second section defines the values used for pin set 1, while the third section defines the values used for pin set 2. Each of these sections is divided into 3 columns, with the exception of the parameters for measuring IOS. The first column is used to enter the values for the "Test Limits," which the system compares to the test results when determining whether the DUT passes or fails either the functional or parametric test. The second column is used to enter the values for the "Parametric Test Conditions," which are forced on each pin during the parametric test so that the parametric measurement unit can measure properly the values entered in the first column. The third column is used to enter the "Functional Test Conditions," which the system forces on the pins during the functional test. During parametric testing, these values are also forced on all pins except the one under test.

The entries in the parameters screen worksheet can be derived from the manufacturer's data sheets for the device to be tested (although the entries are not restricted to only that source of data). Voltage and current levels are defined in terms of pin function and logic state and are applied accordingly by the system when performing parametric and functional tests.

The entries on each worksheet define the parameters for a single test group. Only those parameters are measured for which test limits and corresponding parametric or functional test conditions have been specified. Test program structure defines up to two pin sets while allowing one set of test conditions per pin set

for any one test group. Additional sets of conditions for either pin set must be structured in additional groups (up to a total of 6).

While filling in the parameters screen worksheet, be sure the parameters that are specified do not exceed the system specifications at the front of this manual. Notice, for example, that the functional unit and parametric unit do not have the same capabilities. Functional unit current source and sink limits are 24 mA to a DUT low and 8 mA from a high, while parametric unit limits for source and sink are 320 mA and 80 mA, respectively. If voltage or current specifications are exceeded, the system will ignore the entry and treat it as if a blank has been entered.

As a general rule, plan the most significant tests in the first groups, leaving the less significant — say, a power-supply test with unique conditions — for last in group number order. This provides a comprehensive program in which the less significant groups can be selectively deactivated simply by specifying in the describe screen fewer than the total number of groups available in the parameters screens.

Power Supplies.

In section (A) of the worksheet, enter the number of the truth-table step at which the power supply will be tested. Normally, leave this entry blank until the truth table has been structured. The number should designate the step that satisfies the DUT logic state specified for the voltage level (Vi) and current limit (Ii) that are entered below. Typically, this logic state may be all outputs high, all outputs low, or a unique condition; the test step can be designated on the first occurrence of this state in a routine functional test pattern, or the state can be structured especially to test the power supply.

Enter the voltage level Vi and current test limit Ii for the power-supply test. Any current measured in excess of the limit will be flagged as a failure. Be sure that the voltage source (i = 1, 2, or 3) corresponds to the voltage source pin assignment entered on the describe screen worksheet. If Ii is left blank, the power-supply static current parametric test will not be performed.

Enter the shutdown current I-max. Any current measured in excess of this value will cause shutdown of all three power supplies. If this entry is left blank, the system will default to the test limit Ii, assuming a value was entered for Ii. The specific formula for determining I-max varies with each device family. These formulas are given in the sections describing how to program for each family. As a general rule, select a shutdown value that exceeds the worst-case current specification by 25 — 50%. This will permit datalogging of overcurrent values if the DUT fails the power-supply test.

Preliminary Definitions.

The voltage and current levels specified in this worksheet (see Test Limits and Conditions, below) are defined in terms of pin function and logic state. Pins defined as input (I) or output (O) in the describe screen are restricted to those respective functions. Pins defined as bidirectional (B) or tristate (T) in the describe screen can be assigned either input or output functions (by the [SHIFT] [I/O] command) in the truth table. Also, a tristate pin can be assigned to the high-impedance (off) condition by specifying a (T) in the truth table.

The actual levels used for low-level (0), high-level (1), and high-impedance (T) logic states will be determined by the voltage levels specified for functional test conditions VIL and VIH and parametric test limits VOL and VOH (Test Limits and Conditions, below). They will be implemented in functional testing as follows:

1. Low level. Equal to the functional condition VIL for input pins. Equal to or less than the test limit VOL for output pins.
2. High level. Equal to the functional condition VIH for input pins. Equal to or greater than the test limit VOH for output pins.
3. High impedance. Functionally detected at the pin as less than VOH and greater than VOL.

Test Limits and Conditions.

There are two sets of identically defined parameters available under pin set 1 and pin set 2, thus providing for a second pin set that can be separately specified, when required.

Generally, an entry under “Parametric Test Limits” specifies a maximum or minimum limit for the test of the indicated parametric test or functional comparison. An entry under “Test Conditions, Parametric” (after the symbol @) specifies the test condition applied by the system. Any parametric measurement that does not comply with the specified test limit is flagged as a failure. The following define test limits and conditions for parametric tests.

IIL @ VIL. Current IIL measured at an input pin with low-level voltage VIL applied at the pin. IIL is a maximum limit. A negative value of current for this or any other limit indicates that the current is sourced to the parametric measurement unit from the DUT. A positive value indicates that the current is sunk from the parametric measurement unit to the DUT.

IIH @ VIH. Current IIH measured at an input pin with high-level voltage VIH applied at the pin. IIH is a maximum limit.

VOL @ IOL. Voltage VOL measured at an output pin with current IOL sourced to the pin; functional input conditions are established so that a low level is expected at the pin. VOL is a maximum limit.

VOH @ IOH. Voltage VOH measured at an output pin with current IOH sunk from the pin; functional input conditions are established so that a high level is expected at the pin. VOH is a minimum limit.

IZL @ VZL. Leakage current IZL measured at a pin defined as tristate with low-level voltage VZL applied; functional input conditions are established so that a high-impedance state is expected at the pin. IZL is a maximum limit.

IZH @ VZH. Leakage current IZH measured at a tristate pin with high-level voltage VZH applied; functional input conditions are established so that a high-impedance state is expected at the pin. IZH is a maximum limit.

IOS @ VOS. Short-circuit current IOS at an output pin with the pin grounded (i.e., the applied voltage VOS at the pin set to a level specified by the manufacturer); functional input conditions are established so that a high level is expected at the pin. The two entries for IOS are minimum and maximum limits, as indicated. The

software requires that VOS actually be entered (even when the VOS level is 0.0) to ground the pin. When parametrically testing for IOS, the system software changes I-max to the maximum allowed for the selected power supply.

NOTE

The IOS measurement is a force-voltage/measure-current test that can be used for special measurements, e.g., expander current (IX) at an expandable gate, or for unbuffered outputs on the 74LS161.

Under "Test Conditions, Functional" enter the voltage or current values for the system to implement the logic states expected by the truth table. The following define functional test conditions.

VIL is the low-level voltage applied at the DUT input pin when the truth table defines the logic level as a low.

VIH is the high-level voltage applied at the DUT input pin when the truth table defines the logic level as a high.

IOL is the current sourced to the DUT output pin when the output is in a low state.

IOH is the current sunk from the DUT output pin when it is in a high level.

A system requirement for proper operation of the IOH and IOL current generators is that the mid-range voltage $(VOH + VOL)/2$ must be equal to or less than the functional test condition VIH and greater than VIL for the pin set that is being used. (Refer to the theory of the active load, 6.2.3.)

With functional conditions applied, functional testing consists of verifying expected logic states at the output pins. As previously indicated, parametric test limits VOL and VOH are the reference levels for output logic states. (Refer to the discussion of functional testing para 4.2.2, and the theory of the active load, para 6.2.3.)

Tristate Testing.

Functional and parametric testing of tristate pins in the VOL and VOH logic states is the same as for normal output pins. A high-impedance state is detected functionally when the voltage at a tristate pin falls between VOH and VOL for that pin set. (As shown in para 4.2.2, voltage at the pin floats to an approximate mid-range value of $(VOH + VOL)/2$.)

Essentially, parametric testing of the high-impedance state consists of testing how well the pullup and pulldown transistors (Q4 and Q5 of the DUT in Figure 4-1) are turned off. When specified as parametric conditions, VZH and VZL are applied at a pin in the high-impedance state to measure the leakage currents IZH and IZL, respectively, of Q5 and Q4.

General Requirements.

For testing a digital logic device, the functional electronics circuit is used to implement DUT logic states for both functional and parametric testing. As a consequence, functional test conditions VIL, VIH, IOL, and IOH, as well as parametric test limits VOL and VOH, are always required to set up the system for each group and *must* be specified on the parameters worksheet. This applies to *all*

groups of the test and to *both* pin sets if a second pin set is used.

To measure a particular parameter, the test limit and corresponding parametric test condition must be specified. For example, while VOL must be generally specified with functional condition IOL to perform a functional test for an output pin, VOL will not be measured by the parametric unit during a parametric test unless a value for IOL as a parametric test condition is also specified.

4.3.3 Alternate Parameters Screen Worksheet

General.

Use the alternate parameters screen worksheet to expand the program specifications of the parameters screen in three ways:

1. Specify inclusive test step numbers to localize group parametric testing to a particular section of the truth table.
2. Specify relay switching to make special-purpose connections on the socket adaptor board for both parametric and functional testing.
3. Specify an additional value for any parametric test limit (except the power-supply current test and IOS) to provide both maximum and minimum limits for the indicated test, thus bracketing parametric levels.

The software provides an alternate parameters screen for each group of a test program. Entries in this screen supplement entries in the parameters screen and should not be made unless the group has been initialized by entries in the parameters screen. If no entries are made in the alternate parameters screen, test parameters remain as specified in the group parameters screen.

NOTE

The range setting of the parametric measurement unit for a particular measurement is determined by the respective entry for the test limits and conditions in the parameters screen, not the entry in the alternate parameters screen.

Parametric Test Steps.

Enter the START and STOP step numbers that inclusively limit the section of the truth table where parametric tests are to be performed for this group. Although the system will functionally exercise the DUT by starting at the first step (0) and proceeding forward (refer to Parametric Testing, para 4.2.3), it will not search for the logic state required to test a particular parameter until the start step is reached, and it will not proceed beyond the stop step or the first End command it encounters. After the test, the DUT is restarted at step zero (0) for the next test cycle.

The ability to restrict parametric testing to designated steps in the truth table finds a number of applications. For example, some ICs have more than two specifications for a single parameter. To program parametric tests in such cases, use additional groups and different portions of the truth table so that different pins are tested for different specifications of the same parameters.

Tables 4-3 through 4-5 illustrate a portion of the programming for a fictitious device for which the manufacturer gives three different pairs of input current specifications.

Table 4-3
PIN SET ASSIGNMENT

Manufacturer's Specifications*			Describe Screen	
Pin #	IIL	IIH	ID	S (Pin Set)
1	H	H'	I	1
2	M	M'	I	2
3	L	L'	I	1

*H, M, and L are the highest, medium, and lowest specifications for IIL, respectively. H', M', and L' are the highest, medium, and lowest specifications for IIH, respectively.

Table 4-4
PARAMETERS AND ALTERNATE PARAMETERS SCREEN SPECIFICATIONS

	Group 1	Group 2
Parameters Screen:	Pin Set 1 IIL = H IIH = H'	IIL = L IIH = L'
	Pin Set 2 IIL = M IIH = M'	—
Alternate Parameters Screen:	Step 0 to Step 1	Step 2 to Step 3

Table 4-5
TRUTH TABLE

Pin No: ID:	1 I	2 I	3 I	4 0
Step 0	0	1	X	X
1	1	0	X	X
2	X	X	0	X
3	X	X	1	X

*Body of truth table contains logic states.

By assigning pin 1 to pin set 1 and pin 2 to pin set 2 in the describe screen, the high and medium specifications can be tested in group 1, using steps 0 and 1 of the truth table. Notice that this provides the required high (1) and low (0) logic states for pins 1 and 2 while pin 3 is "don't care" (X). The low specification at pin 3, which is also in pin set 1, can then be tested by using steps 2 and 3 of the truth table for group 2. This provides the required high and low logic states for pin 3 while pins 1 and 2 are "don't care".

Other applications include devices that require a preconditioning sequence in the truth table prior to testing for worst-case parametric specifications. The use of inclusive test steps facilitates such programming.

If inclusive steps are not specified for parametric testing, the default values are step 0 to end, i.e., from the first step to the first End command encountered in the truth table.

Relay Selection.

K1...K4 designate four relays which can be installed to make special-purpose connections on the socket adaptor board. By entries in the "Parametric" column, indicate those relays to be enabled during parametric testing for this group. In the same way, make entries in the next column for functional testing. Note that these relays and their associated circuitry must be installed on the socket adaptor board according to program specifications. (Refer to Socket Adaptor Preparation, para 3.9.)

Additional Parametric Test Limits.

Parameters entered in this screen are restricted to test limits IIL, IIH, VOL, VOH, IZL, and IZH in both pin sets. Any value entered for one of these limits is paired with the value entered in the parameters screen to provide a maximum and minimum test limit for the specified parametric test; refer to Table 4-6. The range settings for the entries in the alternate parameters screen are determined by the entries that were made for the associated parameters in the parameters screen.

If no value has been entered for a particular parameter in the parameters screen, then no entry should be made for that parameter in the alternate parameters screen, because the range setting that the system will use in such an instance cannot be determined in a consistent fashion.

Table 4-6
PARAMETRIC MAXIMUM AND MINIMUM TEST LIMITS

Parameter	Parameters Screen	Alternate Parameters Screen
IIL	Max	Min
IIH	Max	Min
VOL	Max	Min
VOH	Min	Max
IZL	Max	Min
IZH	Max	Min

4.3.4 Truth-Table Worksheet

General.

The truth table defines the patterns of input stimulus and expected response that are the basis for testing the DUT both functionally and parametrically. It should include all the functions that the DUT is designed to perform and will generally incorporate worst-case conditions, those most likely to cause failure. The fundamental test sequence is a step-by-step application of these patterns at the sync clock rate, forcing the indicated logic states at the DUT input pins. During functional testing, DUT outputs are compared with expected logic states listed in the table. During parametric testing, the same sequence is used, except that outputs are not verified, to generate the required logic states (either forced on inputs or expected at the outputs) for parametric measurements. (Refer to para 4.2 for a discussion of functional and parametric testing.)

The system supports either manual or automatic entry of data in the truth-table screen (refer to para 4.4). The manual method requires that the inputs and expected outputs be specified by keyboard entry of the appropriate pin states for every pin of each test step. Automatic data entry

is provided by pattern generation and learn mode operation. Up to 4091 steps can be entered in the truth table (0 to 4090).*

The procedure for manual (keyboard) entry of truth-table data and use of the edit mode is given in the truth-table screen description in para 3.7.6. The procedures for automatic pattern generation and learn mode operation are given in this section. Instructions that cover manual coding and preparation for automatic coding of test patterns are included with the following guidelines for preparing the truth-table worksheet.

In pattern generation, the system automatically generates one of three selectable test patterns for DUT input pins: binary, gray code, or pseudorandom gray code, while coding output pins as L (learn) in preparation for the learn mode.

In learn mode operation, the system requires specification of input logic states and permits "learning" of the output response from a DUT. In this case, input coding is specified either manually or by automatic pattern generation. With the manual method, the code L (learn) must be entered for the output pins to be learned; with pattern generation, output pins are automatically coded as L. Run the test program on a *known-good device*. The Ls at the outputs are automatically replaced by the logic state codes resulting from the test, thereby completing the truth table with expected outputs for all subsequent executions of the program.

Data Lines.

The logic state codes allowed for data line entries depend on the pin assignments made in the describe screen, as shown in Table 4-7, where 1, 0, T, and X are high, low, high-impedance, and "don't care" logic states, respectively. L indicates that the output will be "learned" (stored) when the program is initially executed. X indicates that the driver/sense electronics are disconnected from that pin.

The system's actions when it encounters a pin that is "don't care" in the truth table are determined by the definition of the pin in the describe screen and the function it is performing at that step of the truth table. A pin defined as a "don't care" in the describe screen is disconnected from the driver/sensor electronics and the parametric measurement unit. The system sees that pin as a load of approximately 200 pF.

If the pin was defined as a tristate in the describe screen, the active load is enabled, and the current driver at the output of the driver/sensor chip goes to the high-impedance condition disconnecting the pin.

Input pins and bidirectional pins acting as inputs for that step of the truth table are disconnected when the driver disconnect goes into the high-impedance condition and the active load is disabled.

Output pins and bidirectional pins acting as outputs for that step of the truth table are disconnected when the driver disconnect goes into the high-impedance condition. The pins aren't loaded by the active current load.

The codes G, V, C, and X are automatically generated for pins that are correspondingly defined in the describe screen. Pins thus defined are not tested functionally.

Remember that pins defined as bidirectional (B) and tristate (T) in the describe screen can function as either output or input pins and can change function from one test

Table 4-7
ALLOWED LOGIC STATE CODES

Describe Screen Pin Assignment	I	O	B	T	G	V	C	X
	1	1	1	1	G	V	C	X
	0	0	0	0				
	X	X	X	X				
		L	L	T				
				L				

step to another. Accordingly, when coding these pins on the worksheet, indicate (by some convention) which function each of these pins is performing. When these data are entered via the keyboard, input logic states must be displayed in reverse video on the truth-table screen. (Use the [SHIFT] [I/O] command to toggle the entry from normal to reverse video, or vice versa.)

Each data line constitutes a test step and should be consecutively numbered as the worksheet is organized. Later, when data lines are transferred from the worksheet to the truth-table screen, the software will automatically supply and display the required numbering (numbers 0 to 4095 are allowed).

Command Lines.

In addition to data lines, the truth table also contains the command lines of a special instruction set which implement such functions as waiting, looping, and subroutines. The following are rules for writing these commands and descriptions of the functions they initiate.

A command line cannot stand alone as a test step. It must be preceded by a consecutively numbered data line with which it will be associated. Thus, the first line of the truth table cannot be used to write a command line nor can commands be written on two consecutive lines at any location.

The end command (E) is the only command required by every program, regardless of how simple the truth table is; it must be used at least once and can be used to mark the end of the truth table. All other commands are optional.

Jump. The jump command has the form

[J] [step number xxxx] [+/-] [rep number yyyy]

where: [J] is the command letter for a jump

[step number xxxx] is a variable number from 1 to 4090

[+/-] is a keystroke to separate the step number and repetition number

[rep number yyyy] is a variable number from 1 to 4095

When it is encountered, this command causes the program to jump from the present step back to step xxxx and to execute the sequence from xxxx to the present step. This "loop" sequence is repeated yyyy times before the program executes the next test step after the step where it encountered the jump command. Note that the steps which comprise the loop have been performed once before the program reaches the J command line; the program then loops yyyy times, so that the steps listed for the jump command (from xxxx to the J command) are actually performed 1 + yyyy times.

*4000 steps is a recommended limit.

The placement of one jump command within the loop range (step xxxx to the present step) of another is not permitted. Note that xxxx must be located before the jump command line address; the jump command will *not* loop forward. Because of this, step xxxx cannot be zero (0) and must not have an associated command line. The loop count, yyyy, is stored in address xxxx-1. Therefore, step xxxx-1 cannot carry an associated command line (which, if present, would appear after the data line). Note that, for example, when a jump command is used to shift data serially into a DUT containing a register, the output states must specify X for all steps between step xxxx and the present step inclusive. Because the register's contents will change with every repetition of the jump, the register's output pattern for the steps in the jump loop and the truth table's contents for those steps will not match. Comparing the patterns would cause the system to sense an error, but using the "don't cares" in the truth table causes the system to ignore the output states.

A jump command can be placed within a subroutine (see below), provided the loop range does not include the first line of the subroutine.

Subroutine.

The subroutine command has the form

[S] [Step number xxxx]

where: [S] is the command letter for a subroutine

[step number xxxx] is a variable number from 1 to 4090

When the subroutine command is encountered, it causes the high-speed controller to generate the address xxxx and place the return address (which is the present address + 1) on the top of its 4-high address stack. This command causes the program to jump from the present step forward to step number xxxx and to execute the sequence (subroutine) from step xxxx to the first return command ([R]) it encounters.

NOTE

Never place subroutines at the beginning of a truth table. The high-speed controller would then encounter a return command without a known return vector in the address stack. This would cause the program to go off into an indeterminate state.

Step number xxxx should always be greater than the stop step number of the functional test range designated in the run-mode screen. Subroutines should be located after the E command line marking the end of the portion of the truth table containing the functional and parametric tests. If a subroutine is located before the E command and the functional stop step, it will be executed without an S command when the program reaches the step where the subroutine begins. This can be prevented by specifying all parametric and functional testing stop-steps at a step in the truth table before the first step of the subroutine itself.

One subroutine can call another; the 4-high address stack allows up to four subroutines to be nested in this manner.

Return.

The return command is as follows:

[R]

This command indicates the end of a subroutine and returns the program to the next data line after the com-

mand line that called the subroutine.

The Return ([R]) command causes the high-speed controller to read the address on the top of its 4-high address stack. This address is erased from the stack after it is placed on the lines to the driver/sensor RAMs, returning the program to the step immediately after the subroutine command. If a second return command is encountered, it causes the high-speed controller to read the new top address from the address stack.

When the program, without having executed an S command, reads a subroutine located before the E command and reaches the R command for that subroutine, the R command will be read. This causes the system to go to an indeterminate step number because a random number is stored in the 4-high address stack, which also happens when an S command is located at the start of the truth table. Note that, if the subroutine has another subroutine nested inside, i.e., it contains an S command, an address will have been stored in the high speed controller's address register. When the second return command is encountered, ending the nested subroutine, it causes the high-speed controller to read the new top address from the address stack.

Wait

The wait command has the form

[W] [count number xxxx]

where: [W] is the command letter for a wait

[count number xxxx] is a variable number from 1 to 4095

This command causes the program to wait xxxx cycles of the test repetition rate (sync clock frequency) before executing the next test step. The Wait ([W] [xxxx]) command will cause the high-speed controller not to increment the address for xxxx number of positive sync triggers. This effectively causes the execution xxxx times of the truth-table step to which the wait command is attached. The wait count, xxxx, is stored as part of the 12-bit code for the preceding address's truth-table step. (Values 1 to 4095 are allowed for xxxx.)

NOTE

Counts for the jump and wait commands are stored in the preceding address. The field for the 12-bit code can be used to store either commands or counts, but not both.

End.

The end command is as follows:

[E]

It is possible to use multiple End commands to block portions of the truth table from being executed. If End commands are used in this way, the truth table must be structured so that all parametric tests are performed before the first End command is encountered. Note that the same blocking effect can be achieved by specifying mutually exclusive start and stop steps for each parametric group and for the functional test. (Refer to para 3.7.6.)

Table 4-8 is a fragment of a truth table illustrating the five basic command lines. The program executes steps 0 to 3 and then skips to the subroutine beginning at step 26. It executes steps 26 to 28 and repeats steps 29 to 30 eight times, before executing step 31 to complete the sub-

Table 4-8
TRUTH TABLE EXAMPLE

Pin: Pin ID:	1	2	3	•	•	•	Comment
	1	1	1	•	•	•	
S 0000;	0	0	0				Functional test start (Run-mode screen)
T 0001;	0	0	0				
E 0002;	1	1	0				
P 0003;	1	1	1				
	S		26				Subroutine called
0004;	0	0	0				Subroutine returns here
	W		5				Wait 5 cycles
0005;	1	1	1				
•							
•							
•							
0024;	1	0	0				Functional test stop (Run-mode screen)
	E						End command
0025;	X	X	X				
0026;	0	0	0				Subroutine begins
0027;	0	0	1				
0028;	0	1	1				
0029;	1	1	1				Loop
0030;	0	0	0				
	J	29 -	8				Jump
0031;	1	1	1				
	R						Subroutine ends

routine. The program then returns to execute step 4, waits five test cycles, and continues from step 5 to step 24 to complete the functional test.

An additional command, the "Z" command, is provided uniquely for debugging applications and is discussed in para 4.7.2 (Debugging).

Learn-Mode Preparation.

If the program is initially run in the learn mode, manually coded truth-table worksheet entries should follow the rules for coding pin states as described for data line entries, except that the output pins to be learned must be coded as L. Additionally, if these output pins are not to be learned, they must be coded as X ("don't care"). When data are entered into the system, the truth-table screen will refuse an L entry for any pin that has been coded 1, 0, or T in a previous step. The L code is restricted to pins defined output (O), bidirectional (B), or tristate (T) in the describe screen. If automatic pattern generation is used to code truth-table screen entries, all test step coding will be generated by the software. The instruction code that initiates each of the three test patterns requires specifying the number of test steps to be generated. Accordingly, allow for this number of data lines when structuring the truth-table worksheet.

4.3.5 Run-mode Screen Worksheet

The entries in the run-mode worksheet primarily select the sequence of system modes of operation for executing the program. It is necessary to be familiar with the various Run modes and the Run-mode Screen discussed in para 3.6.1 of this manual, which covers the required specifications in detail, particularly as they apply to the operator. The following is a brief review of these specifications.

Test Sequence.

One, two, three, or all of the test types can be selected in any order, but if a continuity or Kelvin test is selected, it will be performed first regardless of the order of selection. The order of specification determines the order of execution of the functional and parametric tests. If continuity (C) is selected, it will be executed only once, before the first

group which is enabled, each time the program is executed. The selection and order of the functional (F) and parametric (P) tests, on the other hand, apply to all groups when the program is executed.

In general, select functional testing before parametric testing because it is generally faster than parametric testing, and because functional failures can cause parametric failures.

Bin Table.

As indicated in para 3.6.1, the types enabled as "pass required" in each bin of the bin table constitute the test requirements the DUT must pass to be assigned to a given bin. DUTs will be assigned by the system to the lowest-numbered bins whose requirements they meet. It is important to note, for example, that bin 1 selects the types of tests that will actually be executed for each group that is enabled in bin 1 when the program runs. This permits maintaining a comprehensive program in memory and, according to need, enabling or disabling selected types of tests by the entries in each bin prior to execution.

Functional Test.

Specify here the inclusive truth-table test steps that will be applied in any functional type test for all groups. (refer to Functional Testing, para 4.2.2.) Default values are step 0 to end.

Testing Modes.

The indicated testing modes are described in para 3.6. Of particular interest is their use as debugging aids during the development stages of programming. (Also refer to Debugging, para 4.7.)

4.3.6 Program Layout Chart

Making a program layout chart is suggested as the most effective means for organizing the test program. It permits planning the sequence of conditions and functions for the test program and then identifying by step

where each element of the sequence is to be accomplished as the truth table is filled in. The result is an effective check on the completeness of the program and a valuable tool for any debugging or modification that may be undertaken. When the test results are being evaluated, the program layout chart is particularly useful as a cross-reference between the programmed conditions and functions and the device failures (identified by step number or pin number in results screens). Refer to Figure 4-9 and the Sample Programs Manual for examples of program layout charts (also referred to as block flow diagrams).

Functional Test Requirements.

The most general requirement for programming the truth table is to exercise the device in all the functions it is designed to execute. Additionally, the conditions for these functions should normally be structured so as to include worst-case situations and yield a comprehensive evaluation of device performance. The following are intended as guidelines.

1. Check all input and output pins for proper logic operation.
2. Check that all internal nodes can be drive high or low and that each node is independent of adjacent nodes.
3. Worst-case data pattern transfer:
 - All 1's
 - All 0's
 - Alternate 1's and 0's
 - Alternate 0's and 1's
4. Stuck bit test:
 - All 1's on inputs and outputs and walk a 0 through
 - All 0's on inputs and outputs and walk a 1 through
5. Avoid race conditions. A race condition is defined as the inability to determine the output of a gate when the inputs to the gate are making simultaneous transitions. Any device could have race conditions established by the inputs.

Parametric Test Requirements.

The truth table should include all the pin states required to test the DUT completely, as specified in the parameters screen worksheets. Typically, a parametric measurement at a particular pin specifies a logic state for that pin only and is independent of the states at other DUT pins. In such cases, the test patterns programmed for functional testing can often satisfy the logic conditions for parametric testing, the parameters being measured on the first occurrence of their required logic states as parametric testing cycles through the truth table.

On the other hand, some parametric tests require control of logic states at more than one DUT pin at a time. Power-supply tests are generally of this type; input current tests on TTL multi-emitter gates and multiple (more than two) specifications for a single parameter are typical examples. In such cases, test steps are normally written specifically to provide logic conditions for parametric testing.

Generally, it is recommended that parametric test steps be located at the beginning of the truth table, i.e. after the parameters screen worksheets have been completed, so that test time can be minimized (because the DUT is exercised starting at truth-table step zero again for each parametric test. This is not always possible or desirable,

however, so keep in mind the flexibility that the software provides. For each test group, it is possible to specify by step number (on the parameters screen worksheet) where the power-supply test is performed and by inclusive step numbers (on the alternate parameters screen worksheet) where the other parametric tests of the group are located. Accordingly, with the aid of the program layout chart, the parametric pin state requirements for all test groups can be combined with the overall functional requirements of the truth table.

Finally, verify that the completed truth table satisfies the logic conditions for each parametric group as follows:

1. Check that the test step designated for the power-supply test provides the DUT pin states specified (generally by the manufacturer) for that test.
2. Check the logic requirements for each parameter specified under "test conditions, parametric" in the parameters screen worksheet. The indicated logic state should occur at least once at each appropriate pin (input, output, or tristate, as defined by the parameter) within the inclusive test steps designated in the alternate parameters screen.
3. Check that any special parametric condition specifying logic states at more than one pin (e.g., input current conditions for a multi-emitter gate, para 4.8.5, or multiple specifications of a single parameter, para 4.3.3) is properly structured within the inclusive test steps designated in the alternate parameters screen for the group where the test is to be performed.

4.4 AUTOMATIC PATTERN GENERATION

4.4.1 General

The 1732 provides three macro programs to generate automatically test patterns for the DUT input pins in a binary code, gray code, or pseudorandom gray code sequence. Normally, in each case, all outputs are automatically coded L in preparation for learn mode operation. The purpose of these macros is to aid the user in filling in the truth-table screen while reducing the programming time and chance of error normally associated with manual data entry. The macros are especially useful for programming devices that require long and comprehensive test sequences (e.g., counting, generation of memory addresses, etc).

When using automatic pattern generation, all test step coding is generated by the software. By this method, one of three input patterns can be selected: binary, gray code, or pseudorandom gray code. In each case, code variation is restricted to pins defined as I in the describe screen. Output pins will normally be coded L automatically. Pins defined as B and T will be treated only as outputs by the pattern generators. If they have been defined as inputs in the line preceding the pattern generation macro, they will be coded as X outputs in the pattern. The V, C, G, and X codes will be repeated in the normal manner.

The binary and gray code generators permit user selection of the input pins to be varied. Unselected input pins will repeat their last-defined codes (or zeroes (0) if no previous code is defined) throughout the pattern. The pseudorandom gray code generator does not allow pin selection; the test pattern is entered for all inputs.

When pattern generation is used in conjunction with manually coded output pins, those pins should normally

be entered as X or L. When the pattern generator is implemented, Ls are generated for all output pins that were coded X or L in preceding steps of the truth table, and Xs are generated for all output pins that were previously coded other than X or L.

The use of automatic pattern generation does not exclude manual data entry elsewhere in the truth table. Additionally, by means of the edit mode, the resulting patterns can be manually altered, as desired, prior to executing the program. Automatic and manual test patterns can be strung together to expand the truth table. One automatic pattern can be executed following another (e.g., a gray code following a binary code), provided that pins coded L have not been previously learned. Note that the patterns created by the pattern generator can be changed; alterations can be made via the edit mode prior to executing the program.

Common Features.

The three pattern generator macros have the following features in common: the number of test steps to be generated must be specified and all DUT pins are coded automatically, as follows.

- Codes in the pattern are varied only for pins defined as input (I) in the describe screen.
- Pins defined as output (O), bidirectional (B), or tristate (T) are coded learn (L) in the pattern if they have been coded L or X in previous steps of the truth table; they are coded X if they have been previously coded high (1), low (0), or high-impedance (T).
- Pins defined as bidirectional (B) or tristate (T) are treated as outputs unless they are defined as inputs in the line preceding the pattern generator macro command, in which case, they are coded as X outputs in the pattern.
- The codes for pins defined as ground (G), voltage source (V), clock (C), and "don't care" (X) are repeated in the usual manner. Use the [right arrow] key to move the cursor past such pins to complete the macro command.

A pattern generator macro can be initiated at any test step to generate any number of additional test steps or the remainder of the truth table. One restriction is that the truth-table step numbers cannot exceed (decimal) 4090. The second restriction is that the binary and gray code generators cannot be used to generate patterns for more than 12 inputs per device. A third restriction is that the pins to be learned must have been coded either X or L in the line just prior to the macro. If the pin has been coded with some other logic state, Xs will be inserted for that pin upon execution of the macro.

4.4.2 Binary Code Generator

Figure 4-4

The macro program for the binary code generator is initiated by a command having the general form

[B] [number of steps xxxx] [weighting w . .]

where: [B] is the key character indicating that the code will

be binary [number of steps xxxx] is a decimal number from 1 to 4094 specifying how many steps will be generated

[weighting w] is the hexadecimal weight given to an input pin (pin numbers were assigned in the describe screen).

Weight is defined as the number of times a pin will change state.

A pin with a weight of w will change state once every 2^w steps; thus a pin weighted 0 will change state every step, a pin weighted 3 would change once every 8 steps, and so forth. Hexadecimal weights 0 to B are available; hence, up to 12 input pins can be programmed. Input pins can be weighted according to program requirements, and not all inputs needed be weighted. An input pin is weighted by entering the desired hexadecimal value in the column under the assigned pin number. An input pin can be skipped by pressing the right-arrow key, moving the cursor past the pin's column. If no weight is entered for a particular pin, the last code entered for that pin is automatically repeated throughout the pattern. (Zeros (0) are repeated if no previous code has been entered.) No weight can be used more than once, however, and no weight can be skipped. If four input pins are to be varied, the weights must be 0, 1, 2, 3 – not 0, 1, 3, 4, for example.

Program Example.

Figure 4-4a shows the truth-table screen for a 74LS161A synchronous counter that is being programmed using the binary code generator. Steps 0 through 5 have been filled in manually. (The truth-table screen description, para 3.7.6, gives detailed procedures for manual data entry and use of the edit mode.) The command code which initiates the macro is shown below step 5. The keyboard sequence for this command is

[B] [ENTER] [6] [0] [ENTER] [5] [0] [1] [2] [3] [4] [ENTER]
where the alphanumeric entries are typical and the [ENTER] key is pressed where indicated.

For the illustration, the command is only partially complete, i.e., the last [ENTER] keystroke has not yet been executed to run the macro program. The command states that 60 steps of binary code will be generated and assigns weights 5, 0, 1, 2, 3, 4 to input pins 1 through 6, respectively.

Note that, if the programmer had decided not to weight pin 1, he could have used the [right arrow] key to skip the column under that pin. This would cause the high (1) last entered for pin 1 to be repeated throughout the pattern when the macro was executed. Any input pins can be skipped in a similar manner.

When the last [ENTER] keystroke of a macro command line is executed, a delimiter "\$" symbol is displayed to the far right and remains on the screen while the macro is running. The resulting test pattern is then displayed on the truth-table screen, with the first line of the pattern replacing the command line. The results can be viewed (up to 11 lines at a time) in the usual manner by using the observe [0] command in the edit mode, and any data or command lines that are appropriate can be added after the macro-generated pattern. (Remember that an E command is required, and it is recommended that it be placed at the end of the truth table.)

NOTE

If a large number of steps are specified, the time required for the system to generate the pattern can be significant. For example, a 4000-step pattern for a 16-pin device requires about 5 minutes.

Figure 4-4b shows the first 11 lines of the truth table, including the first five lines of the automatically generated

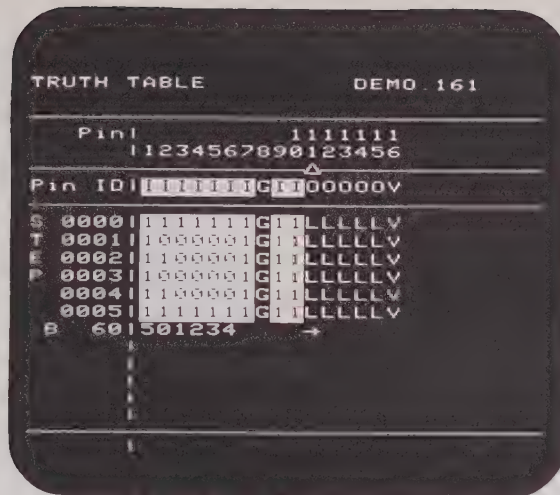


Figure 4-4a. Truth-table screen of example program "DEMO.161" showing the first 6 steps of manually-entered code followed by the macro command after step 5, which initiates the binary pattern generator. On execution, 60 steps of binary code will be automatically generated with pins 1 through 6 weighted as indicated.

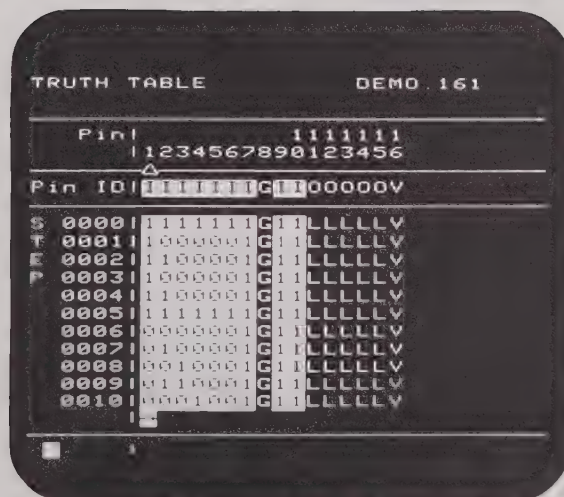


Figure 4-4b. Truth-table screen of example program "DEMO.161" showing steps 0 through 10 of code after generation of the binary pattern previously defined after step 5. Input pins 7, 9, and 10 are not part of that pattern and repeat their previously entered codes. All outputs are coded L for "learn", in all steps.

TRUTH TABLE										DEMO. 161									
Pin										1111111									
										1234567890123456									
										A									
Pin ID										1111111G1100000V									
S	0000	1	1	1	1	1	1	1	1	G	1	1	0	0	0	0	0	0	V
T	0001	1	0	0	0	0	0	0	1	G	1	1	0	0	0	0	0	0	V
E	0002	1	1	0	0	0	0	0	1	G	1	1	0	0	0	1	0	0	V
P	0003	1	0	0	0	0	0	0	1	G	1	1	0	0	0	1	0	0	V
	0004	1	1	0	0	0	0	0	1	G	1	1	0	0	1	0	0	0	V
	0005	1	1	1	1	1	1	1	1	G	1	1	0	0	1	0	0	0	V
	0006	0	0	0	0	0	0	0	1	G	1	1	0	0	0	0	0	0	V
	0007	0	1	0	0	0	0	0	1	G	1	1	0	0	0	0	0	0	V
	0008	0	0	1	0	0	0	0	1	G	1	1	0	0	0	0	0	0	V
	0009	0	1	1	0	0	0	0	1	G	1	1	0	0	0	0	0	0	V
	0010	0	0	0	1	0	0	0	1	G	1	1	0	0	0	0	0	0	V

Figure 4-4c. Truth-table screen (steps 0 through 10 of example program "DEMO.161" after learn mode execution.

TRUTH TABLE										DEMO. 161									
Pin										1111111									
										1234567890123456									
										A									
Pin ID										1111111G1100000V									
S	0035	0	1	0	1	1	1	1	1	G	1	1	0	0	0	0	0	0	V
T	0036	0	0	1	1	1	1	1	1	G	1	1	0	0	0	0	0	0	V
E	0037	0	1	1	1	1	1	1	1	G	1	1	0	0	0	0	0	0	V
P	0038	1	0	0	0	0	0	0	1	G	1	1	0	0	0	0	0	0	V
	0039	1	1	0	0	0	0	0	1	G	1	1	0	0	0	1	0	0	V
	0040	1	0	1	0	0	0	0	1	G	1	1	0	0	0	1	0	0	V
	0041	1	1	1	0	0	0	0	1	G	1	1	0	0	1	0	0	0	V
	0042	1	0	0	1	0	0	0	1	G	1	1	0	0	1	0	0	0	V
	0043	1	1	0	1	0	0	0	1	G	1	1	0	0	1	1	0	0	V
	0044	1	0	1	1	0	0	0	1	G	1	1	0	0	1	1	0	0	V
	0045	1	1	1	1	0	0	0	1	G	1	1	0	1	0	0	0	0	V

Figure 4-4d. Truth-table screen (steps 35 through 45) of example program "DEMO.161" after learn mode execution. All outputs were "0" in the intervening steps (11 through 34.)

code that results after execution of the macro command line illustrated in Figure 4-4a. Notice that unweighted input pins 7, 9, and 10 repeat their previously entered codes, while all output pins are coded L. (Figure 4-4d shows steps 35 to 45 of the same truth table after the outputs have been learned. Refer to Learn Mode Operation, para 4.6.3.)

Truth Table Recovery

The Binary macro can also be used to move the display pointer to recover a truth table deleted by the "New" command (see para 3.7.6). The recovery procedure is as follows:

- Exit the edit mode by pressing [SHIFT][B].
- Press [ENTER] and the number of truth table steps to recover.
- Press [ENTER][TRUTH TABLE]. The recovered truth table is then displayed.

4.4.3 Gray Code Generator

The macro program for the gray code generator is initiated by a command having the general form

[G] [number of steps xxxx] [weighting w . .]

where: [G] is the key character indicating that the code will be gray.

[number of steps xxxx] is a decimal number from 1 to 4091 specifying how many steps will be generated

[weighting w] is the hexadecimal weight given to an input pin (pin numbers were assigned in the describe screen).

The rules for weighting input pins are the same as described for the binary code generator (above) except that the weighting will produce a gray code sequence rather than a binary sequence. The keyboard command sequence for an example of this command generating 10 steps of code is:

[G] [ENTER] [1] [0] [ENTER] [0] [1] [2] . . . [ENTER]

4.4.4 Pseudorandom Gray Code Generator

The macro program for the pseudorandom gray code generator is initiated by a keyboard command sequence having the general form

[P] [number of steps xxxx]

where: [P] is the key character indicating that the code will be pseudorandom gray code.

[number of steps xxxx] is a decimal number from 1 to 4094 specifying how many steps will be generated.

For this macro, unlike the binary and gray code macros, selection and weighting of pins do not apply. Pseudorandom gray code is generated for *all* input pins; it is not limited to a maximum of 12 input pins as gray and binary code generation are. The keyboard command sequence for an example of this command generating 10 steps of code is:

[P] [ENTER] [1] [0] [ENTER]

4.5 PROGRAM AND SOCKET ADAPTOR COMPATIBILITY

Before trying a newly-coded program, make a final check that the following program specifications have actually been implemented on the socket adaptor for the device to be tested. (Also refer to Socket Adaptor Preparation, para 3.9)

4.5.1 Describe Screen Requirements

sync Clock.

The sync clock must be implemented by wiring DUT SYNC to C0, C0/2, C0/4, C0/8, or C0/16 on the socket adaptor board, or to an external clock, according to the respective program specification C1, C2, C4, C8, or CF, or EXT.

Voltage Source.

Each pin assigned as a voltage source V1, V2, or V3 must be wired to its respective device power supply PS1, PS2, or PS3 on the socket adaptor board.

Ground.

Each pin assigned as ground (G) must be wired to DUT GND on the socket adaptor board.

Clock.

Each pin assigned as a clock input C1, C2, C4, C8, or CF must be wired to its respective clock source C0, C0/2, C0/4, C0/8, or C0/16 on the socket adaptor board, or to an external source if the clock is externally supplied.

4.5.2 Alternate Parameters Screen Requirements

Relays.

Selection of any relays for parametric or functional tests in the alternate parameters screens will only supply software-generated relay-enable signals during the respective tests. The effect of these selections depends on how they are implemented in the socket adaptor hardware.

The enable signals for relays K1 through K4 are present at RY1 through RY4, respectively, on the socket adaptor board. Install and wire the relays and dependent circuitry according to program requirements.

4.6 LEARN MODE

4.6.1 General

Learn-mode operation of the system permits "learning" the output response to specified inputs by running the test program on a *known-good device*. When the program is initially executed, all truth-table learn (L) codes at output pins are replaced by codes corresponding to actual DUT responses, so that the resulting truth table defines expected outputs for all subsequent executions of the program.

Any program containing unknown (L) outputs in the truth table is automatically executed in the learn mode, i.e., execution is restricted to a functional test which will determine the unknown outputs. Any subsequent execution of the program is not so restricted. The procedures for programming and "learning" a known-good device parallel routine programming and operational procedures, differing only in the particulars that are discussed below.

4.6.2 Program Preparation

Prior to beginning learn-mode program preparation, make sure that there are no partially executed tests waiting to be continued. Press the [START/ABORT] button until either a general information screen or a PASS/FAIL/BIN screen is displayed.

When programming for a learn-mode test, follow the general guidelines in para 4.3 (Preparation of Program Worksheets). The basic differences are that some or all outputs are coded L in the truth table and testing is restricted to a single functional test. Thus, any additional functional tests and all parametric tests, as well as all specifications in the display- and output-mode screens, are ignored when the program is first executed.

The user has the option of either writing a program that will be complete after the initial learn-mode execution or writing a program in which using the learn-mode will generate only a portion of the final program.

To facilitate generation of new versions of the same program, a program coded for learn-mode execution can also be recorded for execution at a later time. An example is a ROM test program where several test patterns can be

recorded and then learned for new applications of the same base program.

Additionally, if the truth table represents a substantial amount of work, the program should be recorded prior to running it in the learn mode. Then if the program aborts, the work can be easily recovered. (Refer to NOTE in step c of Operating Procedure, para 4.6.3.)

The following are the minimum program requirements for learn mode operation.

Describe Screen. Complete all describe screen specifications. The only restriction is that the sync clock selection must be equal to or less than one-quarter of C0, i.e., only C4, C8, or CF are allowed for learn-mode operation. Additionally, if gate and strobe adjustments are required within the sync clock time frame, make these adjustments in the gate/strobe screen. (A different sync clock can be selected after outputs have been learned.)

Parameters Screen. Specify parametric test limits VOL, VOH and functional test conditions VIL, VIH, IOL, and IOH for the group to be selected in the run-mode screen.

Alternate Parameters Screen. Enable any relays that are required to implement the intended functional test for the group selected.

Truth-Table Screen. Enter the code L for the output pins to be learned. For detailed instructions, refer to Truth-Table Worksheet, Learn Mode Preparation, para 4.3.4.

Figure 4-4b shows the first 11 lines of an example program truth table that has been coded for the learn mode.

Run-Mode Screen. Enable the following selections prior to running the program in the learn mode:

1. Test Sequence. Include an "F" for functional test in the entered sequence.
2. Bin Table. Only one functional (type) test is executed. Therefore, make sure the intended functional test is the first functional test, according to group order, that is enabled in the bin table.
3. Functional Test Steps. Enter the correct functional test start and stop steps, if other than default values (0 to End).
4. Test Mode. Enable "All Groups".

The system will use the first group which has a functional cursor in the run-mode screen. Thus, to insure optimum dc functional levels for learning a device, the first test group that is selected for a functional test in the run-mode screen should have VIL, VIH, VOL, VOH, IOL, and IOH set to best-case values.

4.6.3 Operating Procedure

The following procedures assume a working familiarity with Basic Operating Procedure, para 3.2 of this manual. Further, it is assumed that the program in memory has been prepared for learn-mode operation (Program Preparation, above) and a known-good device and compatible socket adaptor are available.

Steps a through f (below) parallel steps g through j of Basic Operating Procedure, presenting the supplementary information that applies to learn-mode operation.

- a. Prior to loading the program, insure that there is no partially completed test waiting to be continued. Press the [START/ABORT] button until either the general information screen or a PASS/FAIL/BIN result is displayed.
- b. Install an appropriate socket adaptor, and a known-good device.
- c. Load the program into the system and call it up.
- d. Press START and observe that the message

TESTING

is shown in reverse video on the currently displayed screen during program execution. On completion of the test, the first 11 lines of the truth table are automatically displayed with the learned states substituted for the Ls.

NOTE

If, for any reason, the program aborts at this point (the general information screen is displayed), truth-table data are lost and must be entered again before repeating this step. (In this case, use the [N] command in the edit mode to clear the table.)

NOTE

When "learning" a device in learn mode, be patient. A long learn operation, such as the contents of a 2K ROM, can take as long as 5 minutes. Pressing the start/abort key before the operation is completed aborts the procedure. Pressing the start/abort key again will cause the display of a "pass" screen. The device has not been tested, however. The truth table still contains only "L" entries.

- e. Confirm that the learn (L) codes have been replaced by logic state codes. (Enter the edit mode and use the [O] command to view additional lines of the truth table.)

Figure 4-4c shows the first 11 lines of the example program truth table after learn mode execution. Figure 4-4d shows lines 35 through 45 of the same truth table.

After the initial execution (step c, above), all subsequent executions of the program proceed in the normal mode of operation.

- f. Press START again and observe that this time the test is followed by a results screen display. Confirm that the known-good device passes the functional test.

4.7 DEBUGGING

4.7.1 General

Basically, the procedures for debugging programs on the system consist of selectively using the normal system operating modes. Clearly, a number of devices of the same type should be tested to determine that the cause of failure is in the program, program/socket adaptor interface, or socket adaptor, and not in a particular device; an oscilloscope and the Z command could also be used to check that the DUT is functioning. Thereafter, it should be possible to select the appropriate combinations of run and display modes to isolate the problem. Detailed descriptions of system run and display modes are given in Section 3 of this manual.

Additionally, the truth-table instruction set includes a "Z" command which serves uniquely as a debugging tool and is discussed separately (see below).

The following are intended as general guidelines for debugging.

- a. Verify that the socket adaptor is compatible with program specifications (review para 4.5).

- b. Select the run mode. Recommended run modes are either:

- "All Groups First Failure"
- "Stop After Each Group"

- c. In the run-mode screen, enable continuity testing on-ly and execute the program. If continuity fails:

- Check that the socket adaptor is firmly locked into the

pin electronics unit.

- Inspect the socket adaptor for correct assembly and solder connections, particularly if it is a new assembly. If the socket adaptor is suspected, the use of an ohmmeter will aid in the isolation of any open or short.

NOTE

The continuity test cannot be run if there is an intervening circuit in the socket adaptor between the system and the DUT. For example, continuity tests cannot be performed when using the Dynamic RAM Adaptor. In such situations, perform the checks listed above after the checks listed for the functional test.

d. Enable functional testing in the run-mode screen and execute the program. If a functional test fails:

- From the result summary display, note the step number at which the DUT failed and pin numbers of the failed pins.
- If a step number is displayed but no pins are flagged, reduce the strobe setting by one unit.
- Check that the corresponding step in the truth table is correctly coded in terms of the device's response.
- Check that the functional test conditions are correctly entered in the parameters screen of the failed group.

e. Enable parametric testing in the run-mode screen and execute the program. If a parametric test fails:

- Note the pin numbers and functional definitions of the failed pins and display the measurement results for those pins on the results screen.
- Check that the parametric test limits and conditions for pins of the same functional definition are correctly entered in the parameters screen of the failed group.

4.7.2 Using the Z Command

Instructions for entering the "Z" or "zone" command are given in Section 3 (Truth-Table Screen, para 3.7.6). The Z command is the only command in the truth-table instruction set which is intended uniquely for debugging. When the character Z is inserted after any data line not already associated with a command line in the truth table, the system executes the test steps from step 0 up to the Z command and then recycles to step 0 so that the same test pattern repeats continuously when the program runs.

With the Z command in effect and using the system sync clock or the external sync source, if one is used, (test step repetition rate) as the sync for an oscilloscope in a test setup, the DUT pins can be probed to observe the actual pin states at any test steps in the pattern. A more detailed example of how to use the Z command is given below.

The Z command is extremely useful in detecting race conditions. Race conditions will generally be responsible for functional failures with no apparent cause. Sometimes, however, race conditions will be transparent to the system, causing no failures. As an example, consider the 7400 quad 2-input nand gate which is programmed in the Sample Programs Manual. The Boolean expression for each gate is $AB = C^*$ (an asterisk indicates the active-low state), where A and B are the inputs and C^* the resulting output. If the states are $A = 0$, $B = 1$, and $C^* = 1$ in one test step, and the inputs are changed to $A = 1$ and $B = 0$ in the next step, the resulting output is still $C^* = 1$. During

the transition, however, it is conceivable that both $A = 1$ and $B = 1$ for a short period of time, producing a transient low ($C^* = 0$) at the output.

In this case, the low will not be sensed because of the static nature of the device and the rate at which its outputs change with respect to system timing. The minimum interval between gating inputs to a DUT (gate pulse) and sensing outputs (strobe pulse) is 62.5 ns for the system, whereas the propagation delay for the 7400 is 30 — 40 ns. Thus the device reaches a stable state before the outputs are sensed. (For a discussion of system and device timing relationships, refer to para 4.9.4).

On the other hand, a similar race condition can cause problems when testing high-speed MSI devices or devices that are dynamic in nature. Consider a 74122 one shot (The TTL Data Book, Texas Instruments Inc., 1976, page 6-76). Pins 1 through 5 are trigger inputs and the Boolean expression for triggering the device is $A^*B^*CDE = Q$. Let's assume the following sequence: $A^* = 1$, $B^* = 0$, and $C = D = E = 1$ in one step; $A^* = 0$ and $B^* = 1$ in the next step while C, D, and E remain high (1). During the double transition of A^* low to high and B^* high to low, the states of these inputs are undeterminable and the device could be triggered. Note that both A^* and B^* low (i.e., B^* low before A^* high) would have this effect. If the device is triggered, the resulting change of state at the output will last several microseconds and cause unexpected functional failures.

Using the Z command and a dual-trace oscilloscope will allow each pin's logic state to be checked against the truth table worksheet. This will reveal the race condition as an unplanned logic transition. The Z command loops from zero to the first Z regardless of errors.

4.7.3 Debugging the Functional Test

The functional test should be checked in the following manner to assure proper operation. The first step in performing any debug operation is to load the program to be debugged into the system. If the program was entered directly from the keyboard, it is recommended that the program be copied onto a tape cartridge before beginning the debug procedure.

a. Call up the run-mode screen. Select the continuity and functional test sequences, and either "All Groups First Failure" or "Stop After Each Group".

b. After placing a known-good device into the socket adaptor and making sure that the socket adaptor is firmly seated on the pin electronics module, press the [START/ABORT] button.

c. If the device passes the test, insert another device in the socket adaptor and run the test again. If a failure occurs on either test attempt, note the group, step number, and pin(s) which failed.

d. Check the entries in the program worksheets against the values displayed for each screen on the monitor. If the worksheets do not agree with the displays, enter the correct values from the worksheets and run the test again. If the worksheets agree with the displays, check to see if the following conditions have been observed:

- $VIL(\text{func})$ must be less than $VIH(\text{func})$.
- VOL must be less than VOH .
- $(VOL + VOH)/2$ must be less than or equal to VIH and greater than or equal to VIL for that pin set.
- $VIL(\text{func})$, $VIH(\text{func})$, $IOL(\text{func})$, $IOH(\text{func})$, VOL , and VOH must have entries for each pin set used, even if

the pins tested in that pin set do not use them. For example, if the only pin listed in pin set 2 is an input pin, it won't be tested for IOL(func), IOH(func), VOL, or VOH, but those test conditions must be entered in that pin set of the parameters screen or the test may fail.

e. Check the propagation delay of the DUT and verify that the gate/strobe settings are within the DUT's tolerances. Remember that the gate and strobe settings have a tolerance of ± 62.5 ns each. (Refer to para 4.9.4, Sync Clock Timing.) Check that each pin is assigned to the proper gate/strobe set.

f. If all the required conditions for the values have been observed, the proper values have been entered, and the device is believed to be a known-good device, the socket adaptor may be assumed to be faulty.

g. Check the socket adaptor against the information (schematic, tape library adaptor drawings, etc) used in wiring the adaptor; if it does not match the circuit described on the schematic, repair the socket adaptor so that it is in accordance with the schematic. If the adaptor agrees with the schematic, use an ohmmeter to check for opens or shorts in the socket adaptor. For complex socket adaptors containing electronic circuitry (such as the Dynamic RAM Adaptor), use of an oscilloscope to check the functioning of the socket adaptor electronics will be required.

h. If the socket adaptor is found to be wired correctly and working properly, the program may be suspected as the cause of the failure. Two checks should be made prior to any further testing:

- Verify that the frequency of operation of the system sync is within the allowable frequency range for the DUT.
- Check for possible race conditions.

i. Insert a Z command at the step of the truth table which is failing (or the first step without an associated command line following the failing step). Using a dual-trace oscilloscope, synchronize the scope to trigger on either the system sync or some input pin where the required sync level is received prior to the step in the truth table with the Z command. On the system, select the truth-table screen and display the portion of the truth table containing the failing step. Press the [START/ABORT] switch to begin cycling the test. The system will execute the truth table through the step with the Z command, then jump back to step 0. It will continue to do this until the [START/ABORT] switch is pressed again to abort the test. Using one of two traces on the oscilloscope, look at a known-good pin (either input or output) which can be identified on the scope at the step in the truth table which fails. Use the second trace to display the suspected faulty pin.

j. If the DUT appears to be working properly according to the truth table, move the scope probe to the system sync line. Reference that display to the gate/strobe settings to determine the actual position of the gate as it applies to the suspected pin state. The strobe signal can't be accurately viewed with an oscilloscope at the DUT, but the position of the strobe can be determined by adding the amount of delay specified in the gate/strobe settings to the position of the gate signal.

k. Verify the input voltage levels and power-supply voltage levels with the oscilloscope or a digital voltmeter.

l. Stop the program, remove the DUT, and then restart the test. Using an ammeter, connect the common lead (usually the black lead) to the ground pin of the DUT socket adaptor. Place the other lead (normally red) to the suspected pin of the socket adaptor. The ammeter should read the functional value of IOH within system accuracy. Leaving the red lead on the suspect pin, move the common lead to the power-supply pin of the DUT socket adaptor. The ammeter should display the functional value of IOL.

m. At this point, if the failure still cannot be isolated, run the system OVP.

4.8 PROGRAMMING FOR TTL DEVICES

4.8.1 General

Most TTL devices will have a minimum of two test groups based on the power-supply setting: one at a maximum value (V_{cc} max), and the other at a minimum value (V_{cc} min), as specified by the manufacturer's data sheet.* In general, a device is tested functionally in each of the two groups while parametric testing is structured as follows:

- At V_{cc} max, measure IIL, IIH, IOS, and power supply current I_i .
- At V_{cc} min, measure VOL and VOH.

Further testing can be incorporated in these two basic groups or in additional groups, as required.

I_{max} can be determined for TTL devices as follows:

$$I_{max} = \{ I_{cc} + [IOH(\text{functional}) \times \# \text{ of outputs}] \} \times 1.25$$

4.8.2 Program Example, 7400

Pertinent worksheets, a block flow diagram, and excerpts from the manufacturer's data sheets for a 7400 quad 2-input positive nand gate are shown in the Sample Programs Manual and are referenced in the following discussion.

Describe Screen. The default values of 4 MHz and C4 are selected for the clock and sync clock, respectively, to generate a 1-MHz test repetition rate. The device power supply PS1 (0 — +8 V) provides the required commercial voltage range (4.75 — 5.25 V) at pin 14 (V1).

Parameters Group 1. This group is used for V_{cc} min ($V1 = 4.75$ V) test conditions. No power-supply test is executed in this group since no value is entered for the current test limit; only a shutdown value (50 mA) is specified. Parametric test conditions IOL and IOH are entered so the required parameters VOL and VOH will be measured parametrically.

Notice that parametric test limits VOL and VOH and functional test conditions VIL, VIH, IOL, and IOH are entered for all groups, according to system requirements (Parameters Screen Worksheet, General Requirements, para 4.3.2).

Parameters Group 2. This group is for V_{cc} max ($V1 = 5.25$ V). (The group numbers for the V_{cc} max and V_{cc} min group tests could be reversed; the order of execution for these groups is arbitrary.) The power-supply current test limit I1 is the maximum supply current (I_{cc1}) specified by the manufacturer for all outputs low. This condition is produced in step 4 of the truth table by setting all inputs high. In order to unload the outputs, they are coded X for the step where the power-supply test is executed, which keeps the system from adding to the measured current.

*TTL Data Book, Texas Instruments, Inc., 1976.

The value for I-max is calculated from the formula:*

$$I\text{-max} = \{ I_{CC} + [I_{OH}(\text{functional}) \times \# \text{ of outputs}] \} \times 1.25$$

In this example, I-max = 22 mA + [400 μ A $\times$ 4] $\times$ 1.25
 = 22 mA + 1.6 mA $\times$ 1.25
 = 23.6 mA $\times$ 1.25
 = 29.5 mA

Parameters Group 3. This group is added to test the power-supply current limit with all outputs high (Icch). It is measured in step 5 of the truth table, where this condition is produced by setting all inputs low. The test is executed with outputs unloaded, i.e., with X entered as the outputs' logic code.

Run-mode Screen. Both the parametric and functional types of tests are enabled for groups 1 and 2 in the bin table. Only the parametric type test is enabled for group 3. Since the only parametric test that has an entry is the current limit test, the power supply test will be executed and no other tests will be performed in this group.

4.8.3 Multi-emitter Inputs

Because of the nature of multi-emitter input gates, some consideration must be given to the structure of the truth table for devices which contain them. For an accurate parametric measurement of IIL and IIH at a multi-emitter input gate, for example, at least one input should be forward-biased with a low (0) while all other inputs of the gate are high (1). Truth-table steps are generally structured

to walk a 0 through the inputs of each gate for this purpose. Since the system begins all parametric testing by cycling from step 0 of the truth table to the step where parametric testing is to take place, this is accomplished for the 7400 in steps 0 and 1. It is better illustrated by the example for a 3-input nand gate in the Sample Programs Manual.

If all the inputs of a multi-emitter gate were in the high logic state during a parametric test for IIH, IIH would be drawn from all the inputs rather than just the input under test. By setting at least one of the other inputs low, a leakage path is provided and the current supplied through the other inputs is drained off without affecting the measurement.

4.8.4 Program Example, 74LS161A Figures 4-5 thru 4-9 Parametric Requirements.

The manufacturer's data sheets for a 74LS161A synchronous 4-bit counter are shown in Figure 4-5. A study of these data sheets reveals three characteristics to be considered in addition to the general parametric requirements for programming TTL devices.

1. Additional Input Current Limits. Test limits IIL and IIH have multiple input specifications, depending on input pin function.
2. An Additional Output Voltage Limit. Test limit VOL has a second specification for a second test condition IOL.

*Early versions of the Sample Programs Manual used a different formula for calculating I-max which provided a larger tolerance than necessary for marginal devices.

TYPES SN54LS160A THRU SN54LS163A, SN74LS160A THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)									
PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 μ A	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I _{OL} = 8 mA					0.35	0.5	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
	Data or enable P			0.2			0.2		
	Load, clock, or enable T			0.1			0.1		
	Clear ('LS160A, 'LS161A) Clear ('LS162A, 'LS163A)			0.2			0.2		
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V		20			20		μ A
	Data or enable P			40			40		
	Load, clock, or enable T			20			20		
	Clear ('LS160A, 'LS161A) Clear ('LS162A, 'LS163A)			40			40		
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
	Data or enable P			-0.8			-0.8		
	Load, clock, or enable T			-0.4			-0.4		
	Clear ('LS160A, 'LS161A) Clear ('LS162A, 'LS163A)			-0.8			-0.8		
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CCH}	Supply current, all outputs high	V _{CC} = MAX, See Note 3	18	31		18	31		mA
I _{CCL}	Supply current, all outputs low	V _{CC} = MAX, See Note 4	19	32		19	32		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡At typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Figure 4-5. Excerpt from the TTL Data Book, Texas Instruments, Inc., 1976, page 7-199.

1732 DESCRIBE SCREEN WORKSHEET

A. Program Name: 74LS161A

Type of Device (if different from program name) or other comment: _____

B. Number of pins per device: 16
Number of Test Groups per Test Program: 6

C. Clocks
C0: 4.00 MHz (One of these fifteen choices) | 8.00 2.29 1.33
| 5.33 2.00 1.23
| 4.00 1.78 1.14
Sync: C1 = C0/1 C8 = C0/8 | 3.20 1.60 1.07
 C2 = C0/2 C4 = C0/4 | 2.66 1.45 1.00
X C4 = C0/4 External

D. Pin Assignments

	ID	S	ID	S	ID	S
1.	<u>I1</u>		17.		33.	
2.	<u>I2</u>		18.		34.	
3.	<u>I1</u>		19.		35.	
4.	<u>I1</u>		20.		36.	
5.	<u>I1</u>		21.		37.	
6.	<u>I1</u>		22.		38.	
7.	<u>I1</u>		23.		39.	
8.	<u>G</u>		24.		40.	
9.	<u>I2</u>		25.		41.	
10.	<u>I2</u>		26.		42.	
11.	<u>O1</u>		27.		43.	
12.	<u>O1</u>		28.		44.	
13.	<u>O1</u>		29.		45.	
14.	<u>O1</u>		30.		46.	
15.	<u>O1</u>		31.		47.	
16.	<u>V1</u>		32.		48.	

Definitions (for ID)

I (1,2) = Input
O (1,2) = Output
B = Bidirectional
T = Tristate
X = Don't Care
V (1,2,3) = Power
G = Ground

S = Pin Set
(Default is 1)

Figure 4-6a. Describe screen worksheet for 74LS161A program.

1732 RUN-MODE SCREEN WORKSHEET

74LS161A

A. Test Sequence: CFP (for example: CFP, CPF, F, or CP)

B.

	Bin 1	Bin 2	Bin 3	Bin 4	Bin 5
	F	P	F	P	F
G 1	<u>✓</u>	<u>✓</u>			
R 2	<u>✓</u>	<u>✓</u>			
O 3	<u>✓</u>	<u>✓</u>			
U 4	<u>✓</u>				
P 5	<u>✓</u>				
S 6	<u>✓</u>				

Test Procedure

C. Functional Test: Step 0 to step E

D. ✓ All Groups First Failure
 All Groups (use if binning is needed)
 Stop After Each Group
 Test Continuously to Failure
 Test Continuously

E. Single Step

F. Keyboard IS NOT Locked. (Password = up to 6 characters)

Figure 4-6b. Run-mode screen worksheet for 74LS161A program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 6 groups Program Name 74LS161APower Supplies (1) 2, 3)(A) Power Supplies tested at step 65(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+5.25</u> V	I1 = <u>32.0</u> mA	<u>100</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = <u>400</u> mA <u>uA</u>	@ VIL = <u>0.4</u> V	<u>0.8</u> V
IIH = <u>20</u> mA <u>uA</u>	@ VIH = <u>2.7</u> V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA <u>uA</u>
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA <u>uA</u>
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = <u>20</u> mA <u>uA</u> (min)	<u>100</u> mA <u>uA</u> (max)	@ VOS = <u>0.0</u> V

Figure 4-6c. Parameters screen worksheet, group 1, for 74LS161A program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = <u>800.0</u> mA <u>uA</u>	@ VIL = <u>0.4</u> V	<u>0.8</u> V
IIH = <u>40.0</u> mA <u>uA</u>	@ VIH = <u>2.7</u> V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA <u>uA</u>
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA <u>uA</u>
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA (min)	_____ mA/uA (max)	@ VOS = _____ V

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 6 groups Program Name 74LS161APower Supplies (1) 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+4.75</u> V	I1 = _____ mA	<u>100</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = <u>4.00</u> mA <u>uA</u>	<u>4.00</u> mA <u>uA</u>
VOH = <u>2.7</u> V	@ IOH = <u>400</u> mA <u>uA</u>	<u>400</u> mA <u>uA</u>
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA (min)	_____ mA/uA (max)	@ VOS = _____ V

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.00</u> mA <u>uA</u>
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA <u>uA</u>
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA (min)	_____ mA/uA (max)	@ VOS = _____ V

Figure 4-6d. Parameters screen worksheet, group 2, 74LS161A program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 6 groups Program Name 74LS161APower Supplies ① 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+4.75</u> V	I1 = _____ mA	<u>100</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.5</u> V	@ IOL = <u>5.00</u> mA/uA	<u>8.00</u> mA/uA
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

Figure 4-6e. Parameters screen worksheet, group 3, for 74LS161A program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.00</u> V
VOL = <u>0.5</u> V	@ IOL = _____ mA/uA	<u>8.00</u> mA/uA
VOH = <u>2.70</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 4 of 6 groups Program Name 74LS161APower Supplies ① 2, 3)(A) Power Supplies tested at step 66(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+5.25</u> V	I1 = <u>32.0</u> mA	<u>100</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA/uA
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA/uA
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

Figure 4-7a. Parameters screen worksheet, group 4, for 74LS161A program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 5 of 6 groups Program Name 74LS161A

Power Supplies ① 2, 3)

(A) Power Supplies tested at step 67

(B) Power Supply

Shutdown Current

I-max

(for this group)

Voltage	Test Limit	
V1 = <u>+5.25</u> V	I1 = <u>31.0</u> mA	<u>100</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = _____ V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA/uA
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

Figure 4-7b. Parameters screen worksheet, group 5, for 74LS161A program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.00</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA/uA
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>4.00</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 6 of 6 groups Program Name 74LS161A

Power Supplies ① 2, 3)

(A) Power Supplies tested at step 68

(B) Power Supply

Shutdown Current

I-max

(for this group)

Voltage	Test Limit	
V1 = <u>+5.25</u> V	I1 = <u>31.0</u> mA	<u>100</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = _____ V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Figure 4-7c. Parameters screen worksheet, group 6, for 74LS161A program.

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA/uA
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>4.0</u> mA/uA
VOH = <u>2.7</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

TRUTH TABLE

74LS161A

```

-----
Pin:      1111111
:1234567890123456
-----*-----
Pin ID:IIIIIIIGII00000V
-----
S 0000:aaaaaaGaiXXXXXV
T 0001:iiiiiiiGioXXXXXV
E 0002:iaiiiiiiGioXXXXXV
P 0003:iaiiiiioGaiXXXXXV
   0004:iiiiiiiGai11111V
   0005:aiiiiiiiGai00000V
   0006:iaaaaaaiGii00000V
   0007:iaaiiiiGii00010V
   0008:iaaiiiiGii00010V
   0009:iaaiiiiGii00100V
   0010:iaaiiiiGii00100V
S 0011:iaaiiiiGii00110V
T 0012:iaaiiiiGii00110V
E 0013:iaaiiiiGii01000V
P 0014:iaaiiiiGii01000V
   0015:iaaiiiiGii01010V
   0016:iaaiiiiGii01010V
   0017:iaaiiiiGii01100V
   0018:iaaiiiiGii01100V
   0019:iaaiiiiGii01110V
   0020:iaaiiiiGii01110V
   0021:iaaiiiiGii10000V
S 0022:iaaiiiiGii10000V
T 0023:iaaiiiiGii10010V
E 0024:iaaiiiiGii10010V
P 0025:iaaiiiiGii10100V
   0026:iaaiiiiGii10100V
   0027:iaaiiiiGii10110V
   0028:iaaiiiiGii10110V
   0029:iaaiiiiGii11000V
   0030:iaaiiiiGii11000V
   0031:iaaiiiiGii11010V
   0032:iaaiiiiGii11010V
S 0033:iaaiiiiGii11100V
T 0034:iaaiiiiGii11100V
E 0035:iaaiiiiGii11111V
P 0036:iaaiiiiGii11111V
   0037:iaaiiiiGii10000V
   0038:iaaiiiiGii10000V
   0039:iaaiiiiGai10000V

```

TRUTH TABLE

74LS161A

```

-----
Pin:      1111111
:1234567890123456
-----*-----
Pin ID:IIIIIIIGII00000V
-----
   0040:iaaiiiiGai00000V
   0041:iaaiiiiGai00000V
   0042:iaaiiiiGai00010V
   0043:iaaiiiiGai00010V
S 0044:iaaiiiiGai00100V
T 0045:iaaiiiiGai00100V
E 0046:iaaiiiiGai01000V
P 0047:iaaiiiiGai01000V
   0048:iaaiiiiGai01000V
   0049:iaaiiiiGai01000V
   0050:iaaiiiiGai01100V
   0051:iaaiiiiGai01100V
   0052:iaaiiiiGai01100V
   0053:iaaiiiiGai01100V
   0054:iaaiiiiGai01100V
S 0055:iaaiiiiGai01100V
T 0056:iaaiiiiGai01100V
E 0057:iaaiiiiGai01100V
P 0058:iaaiiiiGai01111V
   0059:iaaiiiiGai01111V
   0060:iaaiiiiGai01110V
   0061:iaaiiiiGai01110V
   0062:iaaiiiiGai00000V
   0063:iaaiiiiGai00000V
   0064:iaaiiiiGai00000V
   0065:iaaiiiiGaiXXXXXV
S 0066:aaaaaaGaiXXXXXV
T 0067:iiiiiiiGaiXXXXXV
E 0068:iiiiiiiGaiXXXXXV
P      :E
   0069:
      :
      :
      :
      :
      :
      :

```

Figure 4-8. Truth table for 74LS161A program. This printout shows the character i and o where the display screen would show 1 and 0 in reverse video.

3. Unique Power-Supply Test Conditions. Supply current limits I_{ccL} and I_{ccH} each have two pin state conditions specified, requiring a total of four power-supply tests.

Special Considerations

Some 74LS161A manufacturers buffer the inputs rather than the outputs. This can cause a problem when attempting a force-current/sense-voltage test. The sample and hold network of the test is at 0 V prior to the sample and hold time. Connecting this to an unbuffered output causes the output to drop beneath the threshold. This level is sensed at the input flip/flop and can cause a change of state. A device with buffered inputs will likely pass the functional test and fail the V_{OH} test with a reading of about 1.25 V. This type of device can be tested with a force-V/sense-I test.

Worksheet Organization.

Figures 4-6 through 4-9 are the program worksheets, program layout chart, and truth table referenced in the following discussion.

Describe Screen. Input current specifications IIL and IIH can be resolved into two sets corresponding to two sets of input pins. Accordingly, the describe screen defines input pins 2, 9, and 10 (clock, load, and enable T) as pin set 2, leaving the remaining input pins 1, 3 — 6, and 7 (clear, data, and enable P), as well as all output pins, in pin set 1.

Parameters Group 1. IIL and IIH are measured for both pin sets at V_{cc} max. IOS is also measured (output pins only, therefore pin set 1 only).

The first of the four power-supply tests, all at V_{cc} max with outputs open, is specified — this one with clock high and all other inputs low at step 65 of the truth table.

Notice that test limits VOL and V_{OH} and functional test conditions VIL, VIH, IOL, and IOH are specified for both pin sets in all groups of this program, according to system general requirements (para 4.3).

Parameters Group 2. VOL and V_{OH} are measured at V_{cc} min.

Parameters Group 3. VOL is measured at V_{cc} min for a second IOL condition. Notice that this value for IOL is also entered as a functional condition for this group.

Parameters Group 4. The power supply is tested for all inputs low at step 66 of the truth table.

Parameters Group 5. The power supply is tested for all inputs high at step 67 of the truth table.

Parameters Group 6. The power supply is tested for load low and all other inputs high at step 68 of the truth table.

Program Layout Chart. The organization of the truth table is laid out to ensure that all the required tests are performed. Step numbers are entered after the truth table has been completed.

Truth Table. The truth table is structured to perform a complete check of all input and output pins of the 74LS161A functionally and parametrically. The following summarizes all conditions and functions according to step number sequence.

Parametric tests (steps 0 — 5). All parametric tests (IIL, IIH, VOL, V_{OH}, and IOS) except the power-supply tests are performed in the first five steps of the truth table.

Clear (steps 3 — 5). In order to verify that the clear works, the truth table forces all outputs into a high state and tries to hold it. A clear signal (active low) is sent and the truth table looks or senses for all outputs low.

Count (steps 6 — 38). A low at the load input enables the counter and a clear signal presets all outputs to 0. Thereafter the load input is held high so that data inputs, which are arbitrary during the count sequence, are not transmitted. Data inputs are loaded one step before the enabling clock pulse because the D flip-flops require stable data at their inputs. After toggling the clock input, the truth table attempts to sense a binary count on the output. The truth table requires two steps to complete a full binary count because the counter only toggles on a rising clock edge.

Data (A — D) (steps 39 — 59). After the count sequence, all outputs are reset to 0. The load signal is then enabled to allow the transfer of data from the data (A — D) inputs to the outputs upon the rising edge of the clock signal. The

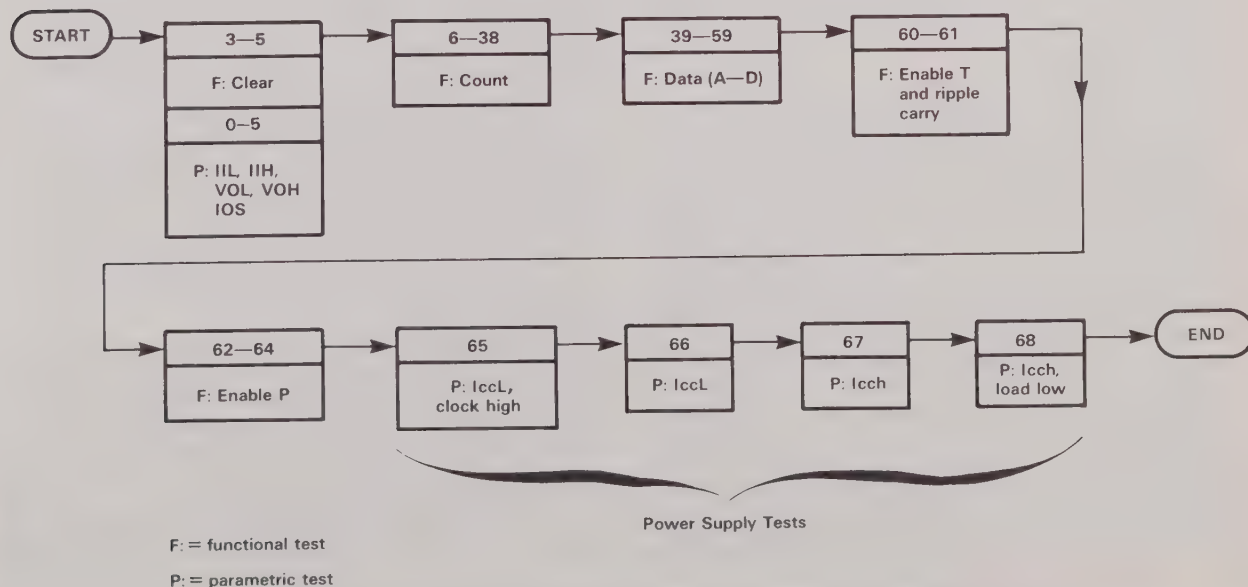


Figure 4-9. Program layout chart for 74LS161A program. This diagram shows organization of the truth table in step number sequence.

truth table walks a high through a field of low inputs and then a low through a field of high inputs and senses for the proper response at the outputs.

Enable T and ripple carry test (steps 60 — 61). The ripple carry bit and all other outputs are preset high at step 59. Enable T is toggled low and enable P is brought high while load is disabled (1) at the same time. In order to try to change all outputs to 0 (i.e., do one more binary count), the clock is toggled from low to high but, because enable T is disabled (0), the outputs are sensed for all 1's.

Enable P test (steps 62 — 64). All outputs are reset to 0 while the enable P and enable T inputs are charged to 0 and 1, respectively. In order to try to change the outputs, the clock is switched high but because enable P is disabled (0), all outputs are sensed for no change (all 0's).

Power-supply tests (steps 65 — 68). See the discussion of parameters groups (above).

Run-Mode Screen. Both functional and parametric testing are enabled for the first three groups of the program. Groups 1 and 2 test the device at Vcc max and Vcc min, respectively, according to general TTL test requirements. The device is tested again at Vcc min in group 3 because of the second set of conditions for VOL, which is tested parametrically and functionally.

The last three groups are enabled for parametric testing only; these are the remaining power-supply tests. (The first was performed in group 1.) Any or all of these groups may be considered optional and can be disabled in the run-mode screen at the discretion of the user.

4.8.5 Open Collector Outputs **Figures 4-10 and 4-11**

Figures 4-10 and 4-11 show the manufacturer's data sheet and sample program worksheets for a 7405 hex inverter with open collector outputs. As an alternative to using pullup resistors, the diode bridge can be set up to act as an active pullup. Structuring the program to use this technique avoids the problems pullup resistors would cause during the parametric test and eliminates the requirements for a special DUT socket adaptor dedicated to just this device. The outputs are sensed as limited tristate outputs: an output is in a low state (0) when the output transistor is on and in a high-impedance state (T) when it is off. A high state (1) is never seen; the high-impedance state is used in its place.

At this point, it is useful to take note of two facts: first, a good device will produce a given output from a given set of inputs; and, second, the 1732 will test for whatever logic state it finds coded for a given pin at a given step of the truth table. This means that the DUT in this program example could have a low input at a given pin, which will produce a high at a given output. If the system finds a logic code T in a step of the truth table for that output pin, it will treat whatever logic level it finds at that step as a T (high-impedance). The system will then measure that level against the test conditions IZL or IZH, whichever is specified in the parameters screen for the group being tested.

The requirement for proper functioning of the active load is that the mid-range voltage $(VOH + VOL)/2$ must be equal to or less than functional test condition VIH for the pin set that is used. This requirement is not satisfied by the specifications for the 7405 (VIH is 2 V and the mid-range voltage is 2.95 V). The general solution for open collector

devices is to use the same nominal value for test limit VOH and functional condition VIH and to define two pin sets: one for input pins, the other for output pins. Thus, the specified value for VIH is used as the nominal value for VOH in the input pin set and the specified value for VOH is used as the nominal value for VIH in the output pin set. This ensures that device test conditions will be correct for the functioning of the active load in both pin sets.

The device will then be tested functionally for either lows (0) or high-impedance states (T) at the outputs. A high-impedance state is tested parametrically by forcing the voltage VZH (VOH from the data sheet) at the pin and measuring the leakage current IZH (IOH from the data sheet).

Worksheet Organization.

The following is a discussion of pertinent worksheet entries for the 7405 program.

Describe Screen. All input (I) pins are assigned to pin set 1; all output pins are defined as tristate (T) and assigned to pin set 2.

Parameters Group 1. The system's general requirements (test limits VOL, VOH, and functional conditions VIL, VIH, IOL, and IOH) are supplied in both pin sets of group 1, as in all other groups of this program.

This group is the Vcc min test and pin set 1, which is restricted to input pins, is exercised functionally only. The specified value for functional condition VIH is also entered as VOH for system setup requirements, although no outputs are actually tested in this pin set.

Pin set 2, which is restricted to output pins, is tested both functionally and parametrically. Because input pins are not tested in this group but are only forced, the specified value for VOH is also entered as functional condition VIH to satisfy the system requirement for the functioning of the active load.

As is the general case for the Vcc min group, VOL is measured parametrically; VOH cannot be measured, however, because an output is defined as going into a high-impedance state rather than a high-level voltage state. For this reason, IOH is not entered as a parametric condition. Instead, high-impedance outputs are tested parametrically by entering IOH (from the data sheet) as the leakage current limit IZH with VOH (from the data sheet) entered as the applied voltage condition VZH.

Parameters Group 2. This group is tested at Vcc max. In addition to the same entries determined for system requirements in group 1, specifications for VIL and VIH as parametric conditions are entered for testing IIL and IIH. The Icc1 power-supply current test is also performed in this group.

Parameters Group 3. This group is programmed for the IccH power-supply test and completes the group specifications for the 7405.

Truth Table. The truth table is filled out with all logic highs shown as high-impedances (T). On step 0, all inputs are low, and all outputs except one are high (T) in order to perform the power-supply tests in groups 2 and 3. In step 1, half the outputs are driven low while the other half are driven high. The remaining steps are used to walk a low (0) through a field of highs (T).

Run-mode Screen. In this screen, the tests for groups 1, 2, and 3 are selected. Both functional and parametric tests

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54H SERIES 74H		
		'01, '03, '05, '12, '22			'H01, 'H05, 'H22		
		MIN	NOM	MAX	MIN	NOM	MAX
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5
High-level output voltage, V_{OH}	74 Family	4.75	5	5.25	4.75	5	5.25
Low-level output current, I_{OL}	54 Family			16			20
	74 Family			16			20
Operating free-air temperature, T_A	54 Family	55	125	55	55	125	55
	74 Family	0	70	0	0	70	0

V_{zh2} , V_{ih2f}

V_{oh1} & V_{oh2}

I_{ol2fp}

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74			SERIES 54H SERIES 74H		
			'01, '03, '05, '12, '22			'H01, 'H05, 'H22		
			MIN	TYP‡	MAX	MIN	TYP‡	MAX
V_{IH} High-level input voltage	1, 2		2			2		
V_{IL} Low-level input voltage	1, 2							
		54 Family		0.8			0.8	
		74 Family		0.8			0.8	
V_{IK} Input clamp voltage	3	$V_{CC} - MIN$, $I_I = 5$		1.5			1.5	
I_{OH} High-level output current	1	$V_{CC} - MIN$, $V_{IL} - V_{ILmax}$, $V_{OH} = 5.5$ V		250			250	
V_{OL} Low-level output voltage	2	$V_{CC} - MIN$, $I_{OL} - MAX$	54 Family	0.2	0.4		0.2	0.4
		$V_{IH} = 2$ V	74 Family	0.2	0.4		0.2	0.4
		$I_{OL} = 4$ mA	Series 74LS					
I_{I1} Input current at maximum input voltage	4	$V_{CC} - MAX$		$V_I = 5.5$ V	1			
				$V_I = 7$ V				
I_{IH} High-level input current	4	$V_{CC} - MAX$		$V_{IH} = 2.4$ V	40		50	
				$V_{IH} = 2.7$ V				
I_{IL} Low-level input current	5	$V_{CC} - MAX$		$V_{IL} = 0.3$ V	1.6		2	
				$V_{IL} = 0.4$ V				
I_{CC} Supply current	7	$V_{CC} - MAX$		$V_{IL} = 0.5$ V				

V_{il1f} & V_{il2f}

I_{zh2}

V_{ol1} & V_{ol2}

I_{ih1p}

I_{il1p}

V_{ih1f}

V_{ih1p}

V_{il1p}

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ$ C.

§ $I_I = -12$ mA for SN54/SN74, -8 mA for SN54H/SN74H, and -18 mA for SN54LS/SN74LS and SN54S/SN74S.

TYPE	I_{CCH} (mA)¶		I_{CCL} (mA)		I_{CC} (mA) Average per Gate (50% duty cycle)
	TYP	MAX	TYP	MAX	
'01	4	8	12	22	2
'03	4	8	12	22	2
'05	6	12	18	33	2
'12	3	6	9	16.5	2
'22	2	4	6	11	2

¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ$ C.

f = functional test value 1 = pin set 1

p = parametric test value 2 = pin set 2

Figure 4-10. Excerpts from the TTL Data Book, Texas Instruments Inc., 1976, pages 6-4 and 6-5.

1732 DESCRIBE SCREEN WORKSHEET

A. Program Name: 7405

Type of Device (if different from program name) or other comment: _____

B. Number of pins per device: 14
Number of Test Groups per Test Program: 3

C. Clocks
C0: 4.00 MHz (One of these fifteen choices) | 8.00 2.29 1.33
| 5.33 2.00 1.23
| 4.00 1.78 1.14
Sync: C1 = C0/1 C8 = C0/8 | 3.20 1.60 1.07
 C2 = C0/2 CF = C0/16 | 2.66 1.45 1.00
 C4 = C0/4 External

D. Pin Assignments

	ID	S	ID	S	ID	S
Definitions (for ID)	1.	<u>I</u>	17.	<u> </u>	33.	<u> </u>
I (1,2) = Input	2.	<u>T</u>	18.	<u> </u>	34.	<u> </u>
O (1,2) = Output	3.	<u>I</u>	19.	<u> </u>	35.	<u> </u>
B = Bidirectional	4.	<u>T</u>	20.	<u> </u>	36.	<u> </u>
T = Tristate	5.	<u>I</u>	21.	<u> </u>	37.	<u> </u>
X = Don't Care	6.	<u>T</u>	22.	<u> </u>	38.	<u> </u>
V (1,2,3) = Power	7.	<u>G</u>	23.	<u> </u>	39.	<u> </u>
G = Ground	8.	<u>T</u>	24.	<u> </u>	40.	<u> </u>
	9.	<u>I</u>	25.	<u> </u>	41.	<u> </u>
	10.	<u>T</u>	26.	<u> </u>	42.	<u> </u>
	11.	<u>I</u>	27.	<u> </u>	43.	<u> </u>
	12.	<u>T</u>	28.	<u> </u>	44.	<u> </u>
S = Pin Set	13.	<u>I</u>	29.	<u> </u>	45.	<u> </u>
(Default is 1)	14.	<u>V</u>	30.	<u> </u>	46.	<u> </u>
	15.	<u> </u>	31.	<u> </u>	47.	<u> </u>
	16.	<u> </u>	32.	<u> </u>	48.	<u> </u>

Figure 4-11a. Describe screen worksheet for 7405 program.

1732 RUN-MODE SCREEN WORKSHEET

A. Test Sequence: CFP (for example: CFP, CPF, F, or CP)

B.

	Bin 1	Bin 2	Bin 3	Bin 4	Bin 5
	F	P	F	P	F
G 1	<u>*</u>	<u>*</u>	<u> </u>	<u> </u>	<u> </u>
R 2	<u>*</u>	<u>*</u>	<u> </u>	<u> </u>	<u> </u>
O 3	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
U 4	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
P 5	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
S 6	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>

Test Procedure

C. Functional Test: Step 0000 to step END

D. All Groups First Failure
* All Groups (use if binning is needed)
 Stop After Each Group
 Test Continuously to Failure
 Test Continuously

E. Single Step

F. Keyboard IS NOT Locked. (Password = up to 6 characters)

Figure 4-11b. Run-mode screen worksheet for 7405 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 3 groups Program Name 7405

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = <u>+4.75</u> V	I1 = _____ mA	<u>45.0</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>16.0</u> mA uA
VOH = <u>2.0</u> V	@ IOH = _____ mA/uA	<u>250</u> mA uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

Figure 4-11c. Parameters screen worksheet, group 1, for 7405 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>3.50</u> V
VOL = <u>0.4</u> V	@ IOL = <u>16.0</u> mA uA	<u>16.0</u> mA uA
VOH = <u>3.50</u> V	@ IOH = _____ mA/uA	<u>250</u> mA uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = <u>250</u> mA uA	@ VZH = <u>3.50</u> V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 3 groups Program Name 7405

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step 0 (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = <u>+5.25</u> V	I1 = <u>33.0</u> mA	<u>45.0</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Figure 4-11d. Parameters screen worksheet, group 2, for 7405 program.

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = <u>1.60</u> mA uA	@ VIL = <u>0.4</u> V	<u>0.8</u> V
IIH = <u>40.0</u> mA uA	@ VIH = <u>2.40</u> V	<u>2.0</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>16.0</u> mA uA
VOH = <u>2.0</u> V	@ IOH = _____ mA/uA	<u>250</u> mA uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>3.50</u> V
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>16.0</u> mA uA
VOH = <u>3.50</u> V	@ IOH = _____ mA/uA	<u>250</u> mA uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 3 groups Program Name 7405

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step 0

Voltage Test Limit
V1 = +5.25 V I1 = 12 mA
V2 = + V I2 = _____ mA
V3 = - V I3 = _____ mA

(B) Power Supply
Shutdown Current
I-max
(for this group)
15.0 mA
_____ mA
_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V	
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.0</u> V	
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>16.0</u> mA/uA	(mA/uA)
VOH = <u>2.0</u> V	@ IOH = _____ mA/uA	<u>250</u> mA/uA	(mA/uA)
IZL = _____ mA/uA	@ VZL = _____ V		
IZH = _____ mA/uA	@ VZH = _____ V		
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V	

Figure 4-11e. Parameters screen worksheet, group 3, for 7405 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.8</u> V	
IIH = _____ mA/uA	@ VIH = _____ V	<u>5.50</u> V	
VOL = <u>0.4</u> V	@ IOL = _____ mA/uA	<u>16.0</u> mA/uA	(mA/uA)
VOH = <u>5.50</u> V	@ IOH = _____ mA/uA	<u>250</u> mA/uA	(mA/uA)
IZL = _____ mA/uA	@ VZL = _____ V		
IZH = _____ mA/uA	@ VZH = _____ V		
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V	

1732 TRUTH-TABLE WORKSHEET

SHEET 1 of 1

Device Number if different from program name, PROGRAM NAME: 7405

Pin Number:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	STEP
ID:	<u>I</u>	<u>T</u>	<u>I</u>	<u>T</u>	<u>I</u>	<u>T</u>	<u>G</u>	<u>T</u>	<u>I</u>	<u>T</u>	<u>I</u>	<u>T</u>	<u>I</u>	<u>V</u>			
0	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>G</u>	<u>0</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>V</u>			0
1	<u>i</u>	<u>0</u>	<u>i</u>	<u>0</u>	<u>i</u>	<u>0</u>	<u>G</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>V</u>			1
2	<u>i</u>	<u>0</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>G</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>V</u>			2
3	<u>0</u>	<u>T</u>	<u>i</u>	<u>0</u>	<u>0</u>	<u>T</u>	<u>G</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>V</u>			3
4	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>i</u>	<u>0</u>	<u>G</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>V</u>			4
5	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>G</u>	<u>0</u>	<u>i</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>V</u>			5
6	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>G</u>	<u>T</u>	<u>0</u>	<u>0</u>	<u>i</u>	<u>T</u>	<u>0</u>	<u>V</u>			6
7	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>G</u>	<u>T</u>	<u>0</u>	<u>T</u>	<u>0</u>	<u>0</u>	<u>i</u>	<u>V</u>			7
8	<u>E</u>																8
9																	9
0																	0
1																	1
2																	2
3																	3
4																	4
5																	5
6																	6
7																	7
8																	8
9																	9
0																	0

Figure 4-11f. Truth table screen worksheet for 7405 program. This worksheet shows the characters i and o where the display screen would show 1 and 0 in reverse video.

are performed in groups 1 and 2. Only a parametric test is performed in group 3. The default values (0 to End) for the functional test start and stop steps are entered.

4.9 PROGRAMMING FOR CMOS-B DEVICES

Programming CMOS-B devices on the system requires particular attention to the following: (1) devices requiring clocked inputs, (2) power-supply tests, (3) I-max selection, (4) timing computations for device propagation delays, and (5) application of industry-standardized specifications to parametric testing. CMOS-B devices usually require all 6 groups in their test. The absolute minimum for a valid test is 3 groups.

4.9.1 CMOS-B Clocks

When devices that require a clocked input are being programmed, the input can be defined as a clock (C) in the describe screen and the corresponding pin wired to the system clock. For CMOS devices, however, the need arises to clock an input at +15 Vdc. The general solution, in this case, is to define the clock pin as an input (I) and have the truth table drive the pin according to the functional conditions specified in the parameters screens (e.g., $V_{IL} = 0$ V, $V_{IH} = 5, 10, \text{ or } 15$ V). The second pin set can be used if a clock requires different voltage levels than other inputs. This scheme for clocking doubles the length of the truth table but does not effectively increase overall test times.

4.9.2 Power-Supply Tests

When powering up for a given group, the system monitors the shutdown status for the selected power supply. There is a 1.0- μ F capacitor on the backplane for each of the power supplies. The power-supply shutdown circuitry is disabled for a period of time after the start of the test to allow this capacitor to change. Small values of I-max, on the order of 800 μ A or less, can take up to 250 ms to reach the programmed level, although the usual delay required is only about 1 ms.

The low level of measured currents during power-supply current-limit tests places some restrictions on the conditions that can be programmed at test steps designated for testing power supplies. Leakage of driver/sensor pins at DUT outputs can contribute to the measured value of power-supply current Idd when a power-supply test is executed. To minimize leakage, steps designated for testing a power supply should have all outputs coded X and, when possible, inputs also should be coded in such a way that a low level (0) is produced at the outputs. This turns off the upper output FET of the DUT, so that any leakage of the system driver/sensor pin is via the lower output FET to ground, thereby permitting a static Idd measurement.

For CMOS devices, such as flip-flops, which have complementary outputs, the outputs necessarily include both highs and lows, and any current drawn from Vdd at the highs could still contribute to the power-supply current measurement. This can be avoided by specifying "don't cares" (X) in the step of the truth table for the power-supply test.

4.9.3 I-max Computation

Several things must be considered when preparing a test program for a CMOS device. Foremost among these is the voltage range of the power supply. CMOS devices generally require Vdd between 5 Vdc and 15 Vdc; only PS2

can provide this range. Vdd is tested at these limits because they provide a better indication of the DUT's performance than a single test with a Vdd of 10 Vdc would.

Second, the parametric value of IOH is drawn from Vdd via the upper FET. For this reason, IOH(para) and IOH(func) must be considered when calculating I-max.

A third consideration is that dynamic Idd is normally greater than static Idd. Dynamic power dissipation is due to two causes. Ninety percent is the result of charging and discharging the load capacitance. The remaining 10 percent is due to the momentary current flow when the output P-MOS and N-MOS transistors pass current from Vdd to Vss. The dynamic power drawn from the supply is found using the following formula:

$$\text{Power (dyn)} = C1 \times Vdd(\text{squared}) \times f(\text{sync}) \times \# \text{ of outputs}$$

Dynamic Idd current can thus be derived by using the following formula:

$$Idd(\text{dyn}) = C1 \times Vdd \times f(\text{sync}) \times \# \text{ of outputs}$$

where: C1 is the maximum system pin loading capacitance of 200 pF and f(sync) is the sync frequency determined by the computations in para 4.9.4, Sync Clock Timing.

The remaining two factors to consider are Idd(static) and worst-case IOH. Idd(static) is found in the manufacturer's data sheets. Worst-case IOH is found by multiplying IOH(func) by the number of outputs.

Combining all this, the formula for determining I-max is arrived at:

$$I\text{-max} = [\{ IOH(\text{func}) + [C1 \times f(\text{sync}) \times Vdd] \} \times \# \text{ of outputs} + Idd(\text{static}) + IOH(\text{para})] \times 1.25$$

This formula is used to determine I-max for CMOS devices *except* when power-supply Idd measurements are to be made.

NOTE

Because of the current limit in the low R-sense range, I-max should not exceed 2.5 mA (see DUT Power Supply table in system specifications). If I-max does exceed 2.5 mA, then the medium R-sense range will be selected by the system, with an attendant loss of resolution.

4.9.4 Sync Clock Timing Computation

Figures 4-12 and 4-13

Typical switching characteristics for a CMOS-B device are shown in Figure 4-12. When considered with respect to system timing requirements, DUT transition and propagation delay times are such that selection of a sync clock frequency can be critical for worst-case conditions. The following is a discussion of the timing events that should be evaluated.

CMOS devices have delays dependent on circuit capacitance. Use $C1 = 240$ pF (C_{max} for the 1732 system) in the timing computations.

Gate time (tg). To allow for system setup, the gate pulse must occur at a minimum of five units (1 unit = 62.5 ns) or 312.5 ns after the start (t0) of the sync clock period.

Driver/sensor delay (td). In response to the gate pulse, the delay of the driver/sensor chip is approximately 40 to 60 ns.

DUT input slew (tr). When comparing the DUT input slew rate requirement to the 1732 functional driver slew rate at a Vdd of 5 V, the 1732 driver/sensor slew rate is

50 V/ μ s. As shown in Figure 4-12, the slowest device response time is at a 5-V V_{DD}. The worst-case slew of the 1732 from 0 to 5 V on the device input is:

$$tr = (VIH - VIL) \times (20ns/V) = 100 \text{ ns}$$

DUT propagation delay (tp). Propagation delay is a function of load capacitance (CL). The typical delay can be calculated from the manufacturer's data sheet. The data sheet suggests a linear relationship between delay and load capacitance, so the maximum time for a capacitance of 240 pF is 4.8 times that of the specified t_{max} for a 50-pF load.

$$tp = tp_{max} \times 4.8 = 180 \text{ ns} \times 4.8 = 864 \text{ ns}$$

DUT output slew (tlh or thl). With V_{DD} at 5 V, determine which transition (high-low or low-high) is slower (generally low-high). As in tp, multiply tl_{hmax} (from the data sheet) by 4.8.

$$tlh = tl_{hmax} \times 4.8 = 360 \text{ ns} \times 4.8 = 1728 \text{ ns}$$

Strobe time (ts). At the maximum allowable setting, the strobe pulse occurs 1 unit (62.5 ns) prior to the end of the sync clock period. However, 100 ns is required for proper error sense latching. The strobe must be placed 2 units (125 ns) before the next sync clock.

$$ts = 125 \text{ ns}$$

Figure 4-13 is a timing diagram for a typical CMOS-B device. To summarize, the gate pulse occurs 5 units (tg) after the start (t0) of the sync clock period and, allowing an additional unit (td) for driver/sensor delay, the DUT will begin to see a change at its inputs at about 375 ns into the period. Assuming 90% of the driver/sensor slew time (tr) as threshold, the input begins to propagate at about 465 ns and, adding propagation time (tp), the DUT output start to change at about 1329 ns. The DUT output can be sensed by the system comparators when it is less than VOL or greater than VOH. Using the worst case (tlh) for output slew and adding 125 ns for output sensing, the sum of the worst-case timing events is 3182 ns. This is the minimum sync clock period and defines the highest frequency at which the device can be tested with confidence.

Gate and Strobe Setting.

Based on a 3182-ns period, the nearest programmable frequency from Table 4-2 (1732 Clock Frequency Relationships) is 1.23 MHz divided by 4 (C4) for the sync clock. This will give a total of 52 period units in the gate/strobe screen (para 3.7.7). Accordingly, set the gate and strobe at their respective limits of 5 and 50 units to test the device.

Table 4-9
CMOS-B WORST-CASE TIMING EXAMPLE

Event	Duration (ns)
tg	312.5
td	62.5
tr	90
tp	864
tlh	1728
ts	125
total	3182*

*The numbers given for tp and tlh are a little worse than worst-case. The Motorola timing diagram shows propagation time as reaching the **middle** (i.e., 50% point) of the tlh time, so instead of 1728 ns at tlh, the value could be one-half of 1728, or 864. The total of 3182 is therefore pessimistic, but certainly safe.

4.9.5 Functional and Parametric Test Considerations

Figures 4-14 through 4-16

Figure 4-14 shows the EIA/JEDEC specifications that have been standardized for the CMOS industry. In applying these data to parametric testing, note the following:

1. Test the device for the commercial temperature range (-40° to +85° C), taking data from the "+25° C" column in the table.
2. Test the device at a V_{DD} of 5 and 15 Vdc.
3. Test input currents IIL and IIH at V_{DD} = 15 Vdc.
4. IOL(func) and IOH(func) are usually set to 1.0 μ A.

Figures 4-15 and 4-16 show the parameters worksheet entries that are derived from the standardized specifications. In the first two groups, the device is tested both parametrically and functionally at the two V_{DD} voltage levels. In the third and fourth groups, the power-supply tests at the two V_{DD} levels are performed. In the last two groups, the device is tested functionally only for threshold operation at the two V_{DD} levels. Notice that I_{max} is set to 2.49 mA in both group 3 and group 4, i.e., to the upper limit of the measurement range with the greatest resolution for I_{DD}. (Refer to para 4.2 and Specifications.

*Formulas are from **Motorola CMOS Data Book**, Motorola, 1978

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns	t _{TLH}	5.0 10 15	— — —	180 90 65	380 180 130	ns
Output Fall Time t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 30 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 22 ns t _{PLH} , t _{PHL} = (0.50 ns/pF) C _L + 15 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	90 50 40	180 100 80	ns

Figure 4-12. Excerpt from Motorola CMOS Data Book, Motorola Inc., 1978, page 7-15, showing switching characteristics for a typical CMOS-B device.

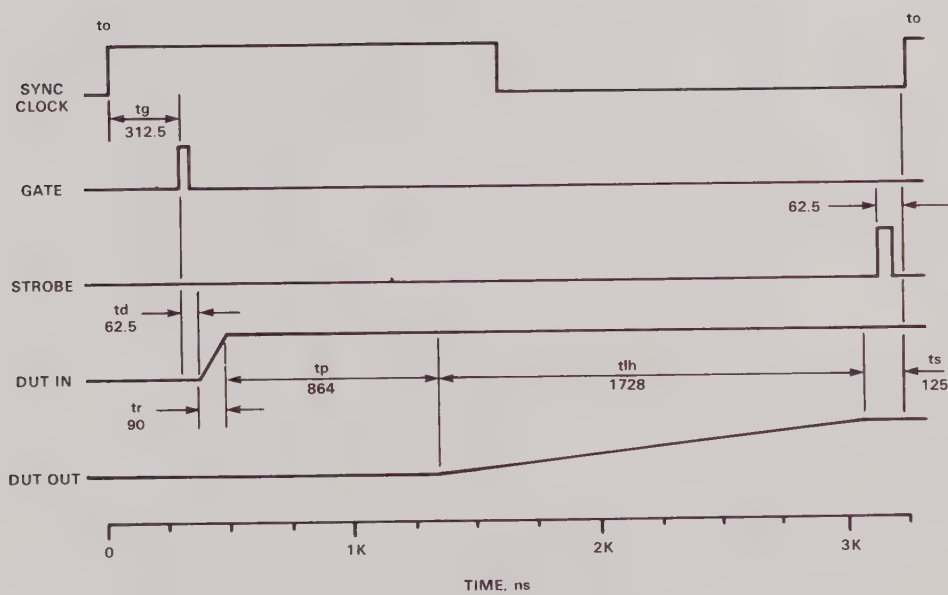


Figure 4-13. Timing diagram for a typical CMOS-B device.

TABLE 1 — EIA/JEDEC FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V _{DD} (Vdc)	CONDITIONS	LIMITS + 25°C						UNITS
					T _{LOW} *				T _{HIGH} *		
					Min	Max	Min	Max	Min	Max	
I _{DD}	Quiescent Device Current	Mil	5	V _{IN} = V _{SS} or V _{DD}		0.25		0.25		7.5	μA _{dc}
			10			0.5		1.5			
			15			1.0		3.0			
	GATES	Comm	5	All valid input combinations		1.0		1.0		7.5	μA _{dc}
			10			2.0		2.0			
			15			4.0		4.0			
	BUFFERS, FLIP-FLOPS	Mil	5	V _{IN} = V _{SS} or V _{DD}		1.0		1.0		3.0	μA _{dc}
			10			2.0		6.0			
			15			4.0		12.0			
	MSI	Comm	5	All valid input combinations		4		4.0		3.0	μA _{dc}
			10			8		8.0			
			15			16		16.0			
		Mil	5	V _{IN} = V _{SS} or V _{DD}		5		5		150	μA _{dc}
			10			10		10			
			15			20		600			
		Comm	5	All valid input combinations		20		20		150	μA _{dc}
			10			40		300			
			15			80		600			
V _{OL}	Low-Level Output Voltage	All	5	V _{IN} = V _{SS} or V _{DD}	0.05	0.05		0.05	0.05	0.05	V _{dc}
			10	I _{OL} < 1μA	0.05	0.05		0.05	0.05	0.05	
V _{OH}	High-Level Output Voltage	All	5	V _{IN} = V _{SS} or V _{DD}	4.95	9.95		4.95	9.95		V _{dc}
			10	I _{OL} < 1μA	9.95	14.95		14.95			
V _{IL}	Input Low Voltage #	All	5	V _O = 0.5V or 4.5V		1.5		1.5		1.5	V _{dc}
	B Types		10	V _O = 1.0V or 9.0V		3.0		3.0		3.0	
			15	V _O = 1.5V or 13.5V		4.0		4.0		4.0	
				I _{OL} < 1μA							
V _{IL}	Input Low Voltage #	All	5	V _O = 0.5V or 4.5V		1.0		1.0		1.0	V _{dc}
	UB Types		10	V _O = 1.0V or 9.0V		2.0		2.0		2.0	
			15	V _O = 1.5V or 13.5V		2.5		2.5		2.5	
				I _{OL} < 1μA							
V _{IH}	Input High Voltage #	All	5	V _O = 0.5V or 4.5V	3.5	7.0		3.5	7.0		V _{dc}
	B Types		10	V _O = 1.0V or 9.0V	7.0	11.0		7.0	11.0		
			15	V _O = 1.5V or 13.5V	11.0						
				I _{OL} < 1μA							
V _{IH}	Input High Voltage #	All	5	V _O = 0.5V or 4.5V	4.0	8.0		4.0	8.0		V _{dc}
	UB Types		10	V _O = 1.0V or 9.0V	8.0	12.5		8.0	12.5		
			15	V _O = 1.5V or 13.5V	12.5			12.5			
				I _{OL} < 1μA							
I _{OL}	Output Low (Sink) Current		5	V _O = 0.4V, V _{IN} = 0 or 5V	0.64			0.51	0.36		mA _{dc}
		Mil	10	V _O = 0.5V, V _{IN} = 0 or 10V	1.6			1.3	0.9		
			15	V _O = 1.5V, V _{IN} = 0 or 15V	4.2			3.4	2.4		
				V _O = 0.4V, V _{IN} = 0 or 5V	0.52			0.44	0.36		
		Com	10	V _O = 0.5V, V _{IN} = 0 or 10V	1.3			1.1	0.9		mA _{dc}
			15	V _O = 1.5V, V _{IN} = 0 or 15V	3.8			3.0	2.4		

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	VDD (Vdc)	CONDITIONS	LIMITS						UNITS
					T _{LOW} *		+25°C		T _{HIGH} *		
					Min	Max	Min	Max	Min	Max	
I _{OH}	Output High (Source) Current	Mil	5	V _O = 4.6V, V _{IN} = 0 or 5V	-0.25		-0.2		-0.14		mA _{DC}
			10	V _O = 9.5V, V _{IN} = 0 or 10V	-0.62		-0.5		-0.35		
			15	V _O = 13.5V, V _{IN} = 0 or 15V	-1.8		-1.5		-1.1		
		Com	5	V _O = 4.6V, V _{IN} = 0 or 5V	-0.2		-0.16		-0.12		mA _{DC}
			10	V _O = 9.5V, V _{IN} = 0 or 10V	-0.5		-0.4		-0.3		
			15	V _O = 13.5V, V _{IN} = 0 or 15V	-1.4		-1.2		-1.0		
I _{IN}	Input Current	Mil	15	V _{IN} = 0 or 15V		±0.1	±0.1	±1.0	μA _{DC}		
		Comm	15	V _{IN} = 0 or 15V		±0.3	±0.3	±1.0	μA _{DC}		
I _{oz}	3-State Output Leakage Current	Mil	15	V _{IN} = 0 or 15V		±0.4	±0.4	±12	μA _{DC}		
		Comm	15	V _{IN} = 0 or 15V		±1.6	±1.6	±12	μA _{DC}		
C _{IN}	Input Capacitance per unit load	All		Any Input			7.5			pF	

*T_{LOW} = -55°C for Military temperature range device, -40°C for Commercial temperature range device.T_{HIGH} = +125°C for Military temperature range device, +85°C for Commercial temperature range device.

#Applies for Worst Case input combinations.

Figure 4-14. Standardized EIA/JEDEC specifications for CMOS devices. (Excerpts from Motorola CMOS Data Book, Motorola Inc., 1978, pages 4-4 and 4-5.)

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) CMOS-BGroup 1 of 6 groups Program Name ANY CMOS-BPower Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max

Voltage	Test Limit	(for this group)
V1 = + V	I1 = mA	
V2 = <u>+5.00</u> V	I2 = mA	SEE PARA 4.9.3
V3 = - V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	.000 mV
IIH = mA/uA	@ VIH = V	5.0 V
VOL = <u>0.10</u> V	@ IOL = <u>440</u> mA/uA	1.0 mA/uA
VOH = <u>4.60</u> V	@ IOH = <u>160</u> mA/uA	1.0 mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

Figure 4-15a. Parameters screen worksheet, group 1, for a typical CMOS-B device.

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) CMOS-BGroup 2 of 6 groups Program Name ANY CMOS-BPower Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max

Voltage	Test Limit	(for this group)
V1 = + V	I1 = mA	
V2 = <u>+15.0</u> V	I2 = mA	SEE PARA 4.9.3
V3 = - V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = <u>0.3</u> mA/uA	@ VIL = .000 mV	.000 mV
IIH = <u>0.3</u> mA/uA	@ VIH = 15.0 V	15.0 V
VOL = <u>1.5</u> V	@ IOL = <u>3.00</u> mA/uA	1.00 mA/uA
VOH = <u>13.5</u> V	@ IOH = <u>1.20</u> mA/uA	1.00 mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

Figure 4-15b. Parameters screen worksheet, group 2, for a typical CMOS-B device.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) CMOS-BGroup 3 of 6 groups Program Name ANY CMOS-B
(POWER SUPPLY TEST)Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = <u>+5.00</u> V	I2 = <u>SEE DEVICE</u> mA	<u>2.49</u> mA
V3 = _____ V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>.000</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>15.0</u> V
VOL = <u>1.5</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA
VOH = <u>13.5</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

Figure 4-15c. Parameters screen worksheet, group 3, for a typical CMOS-B device.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	_____ V
VOL = _____ V	@ IOL = _____ mA/uA	_____ mA/uA
VOH = _____ V	@ IOH = _____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) CMOS-BGroup 4 of 6 groups Program Name ANY CMOS-BPower Supplies (1, 2, 3)

(POWER SUPPLY TEST)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = <u>+5.00</u> V	I2 = <u>SEE DEVICE</u> mA	<u>2.49</u> mA
V3 = _____ V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Figure 4-15d. Parameters screen worksheet, group 4, for a typical CMOS-B device.

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>.000</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>5.0</u> V
VOL = <u>0.400</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA
VOH = <u>4.60</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	_____ V
VOL = _____ V	@ IOL = _____ mA/uA	_____ mA/uA
VOH = _____ V	@ IOH = _____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) CMOS-BGroup 5 of 6 groups Program Name ANY CMOS-BPower Supplies (1, 2, 3) (THRESHOLD TEST)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>+5.00</u> V	I2 = mA <u>SEE PARA 4.9.3</u>	
V3 = V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>1.50</u> V
IIH = mA/uA	@ VIH = V	<u>3.50</u> V
VOL = <u>0.50</u> V	@ IOL = mA/uA	<u>1.0</u> mA/uA
VOH = <u>4.50</u> V	@ IOH = mA/uA	<u>1.0</u> mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	mA/uA(max) @ VOS = V	

Figure 4-16a. Parameters screen worksheet, group 5, for a typical CMOS-B device.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	mA/uA(max) @ VOS = V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) CMOS-BGroup 6 of 6 groups Program Name ANY CMOS-BPower Supplies (1, 2, 3) (THRESHOLD TEST)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>+15.00</u> V	I2 = mA <u>SEE PARA 4.9.3</u>	
V3 = V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>4.00</u> V
IIH = mA/uA	@ VIH = V	<u>11.00</u> V
VOL = <u>1.50</u> V	@ IOL = mA/uA	<u>1.0</u> mA/uA
VOH = <u>13.5</u> V	@ IOH = mA/uA	<u>1.0</u> mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	mA/uA(max) @ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	mA/uA(max) @ VOS = V	

Figure 4-16b. Parameters screen worksheet, group 6, for a typical CMOS-B device.

4.9.6 Program Example, CD4027B Figures 4-17 and 4-18

The CD4027B is a CMOS dual J-K Master-Slave flip-flop. Figure 4-17 shows the data sheets for this device. Each flip-flop has individual J, K, Set, Reset, and Clock inputs. It has buffered Q and Q* outputs. Changes in the flip-flops' output states are synchronous with the negative-going transition of the clock pulse. Set and reset functions are asynchronous and are initiated whenever a high level signal is present on either of the set and reset inputs.

Worksheet Organization.

Most of the values for the worksheets are derived from the standardized JEDEC specifications sheet, as illustrated in Figures 4-15 and 4-16. Values which are not derived from the JEDEC specifications will be described as each worksheet is discussed.

Describe Screen. Voltages for this device are referenced to Vss, so pin 8 will be coded G. The clocks do not require any special voltages, so all pins are entered in pin set 1. The clock frequency is selected by determining the worst-case timing (refer to para 4.9.4). The formulas found in para 4.9.4 produce a worst-case time of 2010 ns. Referring to Table 4-2, the nearest programmable frequency is 444 kHz. As this allows very little margin for delay, drop to the next lower frequency, 400 kHz. This is indicated by entering 1.60 for C0 and C4 for SYNC.

Gate/Strobe Setting. Based on a period of 2500 ns, there will be 40 period units. The gate should be set 312.5 ns after the start of the clock pulse, at 5 units, and the strobe should be set at 39 units in order to gate and strobe the device properly.

Parameters Group 1. Vdd for this group is 5 volts. I-max is calculated using the formula found in para 4.9.3 and the values for IOH(para) and IDD(static) listed in Figure 4-14.

$$\begin{aligned} I\text{-max} &= \left(\left\{ 1 \mu\text{A} + 240 \text{ pF} \times 400 \text{ kHz} \times 5 \text{ V} \right\} \times 4 \right) + \\ &\quad 160 \mu\text{A} + 4 \mu\text{A} \times 1.25 \\ &= \left(\left\{ 401 \mu\text{A} \times 4 \right\} + 164 \mu\text{A} \right) \times 1.25 \\ &= 2.5 \text{ mA (rounded up)} \end{aligned}$$

Parameters Group 2. Vdd for this group is 15 volts. I-max is calculated in the same way as in group 1, using the values for IOH(para) and Idd(static) listed in figure 4-17b for the new Vdd.

$$\begin{aligned} I\text{-max} &= \left(\left\{ 1 \mu\text{A} + 240 \text{ pF} \times 400 \text{ kHz} \times 15 \text{ V} \right\} \times 4 \right) + \\ &\quad 1.2 \text{ mA} + 16 \mu\text{A} \times 1.25 \\ &= \left(\left\{ 1.201 \text{ mA} \times 4 \right\} + 1.216 \text{ mA} \right) \times 1.25 \\ &= 8.0 \text{ mA (rounded up)} \end{aligned}$$

Parameters Group 3. The power-supply test is performed at 15 volts in this group. The value of Idd(max) is entered from the DUT data sheets. I-max is limited to 2.49 mA because of the PS2 current limit in the low R-sense range. Note that the functional value of IOH and IOL are set at 0.0 μA . This is because the DUT is a flip-flop and has complementary outputs, which means that one output will always be high.

Parameters Group 4. The power-supply test is performed at 5 volts in this group.

Parameters Group 5. This group tests the threshold levels at 5 V. I-max is the same as in group 1.

Parameters Group 6. This group tests the threshold levels at 15 V. I-max is the same as in group 2.

Truth Table. The truth table is set up so that the outputs of the two J-K flip-flops are always complements of each other. This will provide a quick check that the two flip-flops are operating independently of each other. In step 0, all inputs except one are placed low in each half of the DUT; in step 1, the logic states of all the inputs are reversed. Because of this, parametric checking can be accomplished on the first two steps of the truth table. The power-supply tests will be performed next, in step 2. The rest of the truth table completes exercising all the possible combinations of the DUT's inputs.

Run-mode screen. As noted in para 4.9.5, groups 1 and 2 are tested both functionally and parametrically, groups 3 and 4 are tested only parametrically, and groups 5 and 6 are tested only functionally. The functional test step default values are entered.

4.9.7 Tristate CMOS-B Devices

There are two differences between CMOS-B devices and tristate CMOS-B devices which must be taken into account when testing them on the system. First, using a functional IOL or IOH of 1 μA in the high-impedance state requires approximately 400 μs to charge or discharge the system capacitance to the high-impedance level. This can be shown as follows.

The time it takes to charge the system capacitance can be found using the equation:

$$dt = \frac{C \times dV}{i} \quad \begin{array}{l} C = 240 \text{ pf} + \text{PIN } C \\ dV = 15 - 13.5 \\ i = 1 \mu \text{ Ioh} \end{array}$$

The 1732 and the DUT socket adaptor have a maximum capacitance of 205 pF. The worst-case condition of dV would be for a VOH of 15 V and a VOL of 13.5 V. Thus, using an IOH of 1.0 μA as derived from the JEDEC specifications,

$$dV = 15 - 13.5 = 1.5 \text{ V}$$

and

$$dt = \frac{245 \text{ pF} \times 1.5 \text{ V}}{1.0 \mu\text{A}} = 367.5 \mu\text{s}$$

This would require a gate/strobe setting which can't be entered into the system. The only variable that can be changed is IOH. Using the value of IOL(para) and IOH(para) for the functional values of IOL and IOH produces a gate/strobe setting that can be entered into the system.

Second, the outputs of a tristate CMOS-B device won't source or sink current when it is operating in the high-impedance state. Only a small leakage current will be present at the outputs; thus, IZL and IZH must be tested.



MOTOROLA

MC14027B

DUAL J-K FLIP-FLOP

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- Toggle Rate = 3.0 MHz typical @ 5 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design –
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Pin	I	10	mA
Operating Temperature Range – AL Device	T_A	-55 to +125	°C
CL/CP Device		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

C†	INPUTS				OUTPUTS*		
	J	K	S	R	$Q_n^{\ddagger}$	Q_{n+1}	$\bar{Q}_{n+1}$
	1	X	0	0	0	1	0
	X	0	0	0	1	1	0
	0	X	0	0	0	0	1
	X	1	0	0	1	0	1
	X	X	0	0	X	Q_n	$\bar{Q}_n$
	X	X	1	0	X	1	0
	X	X	0	1	X	0	1
	X	X	1	1	X	1	1

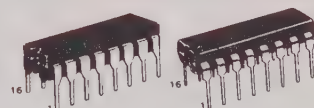
X = Don't Care
† = Level Change
‡ = Present State
* = Next State

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM

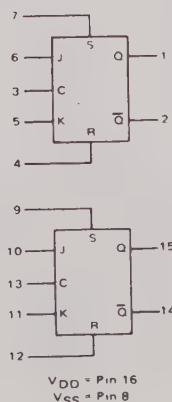


Figure 4-17a. Excerpt from Motorola CMOS Data Book, Motorola, 1978, page 7-80

MC14027B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage [#]	V _{IL}	(V _O = 4.5 or 0.5 Vdc)	5.0	—	1.5	—	2.25	1.5	—	Vdc
		(V _O = 9.0 or 1.0 Vdc)	10	—	3.0	—	4.50	3.0	—	
		(V _O = 13.5 or 1.5 Vdc)	15	—	4.0	—	6.75	4.0	—	
	V _{IH}	(V _O = 0.5 or 4.5 Vdc)	5.0	3.5	—	3.5	2.75	—	3.5	Vdc
		(V _O = 1.0 or 9.0 Vdc)	10	7.0	—	7.0	5.50	—	7.0	
		(V _O = 1.5 or 13.5 Vdc)	15	11.0	—	11.0	8.25	—	11.0	
Output Drive Current (AL Device)	I _{OH}	(V _{OH} = 2.5 Vdc) Source	5.0	-1.2	—	-1.0	-1.7	—	-0.7	mA _{dc}
		(V _{OH} = 4.6 Vdc)	5.0	-0.25	—	-0.2	-0.36	—	-0.14	
		(V _{OH} = 9.5 Vdc)	10	-0.62	—	-0.5	-0.9	—	-0.35	
		(V _{OH} = 13.5 Vdc)	15	-1.8	—	-1.5	-3.5	—	-1.1	
		(V _{OL} = 0.4 Vdc) Sink	5.0	0.64	—	0.51	0.88	—	0.36	
	I _{OL}	(V _{OL} = 0.5 Vdc)	10	1.6	—	1.3	2.25	—	0.9	mA _{dc}
		(V _{OL} = 1.5 Vdc)	15	4.2	—	3.4	8.8	—	2.4	
Output Drive Current (CL/CP Device)		I _{OH}	(V _{OH} = 2.5 Vdc) Source	5.0	-1.0	—	-0.8	-1.7	—	
	(V _{OH} = 4.6 Vdc)		5.0	-0.2	—	-0.16	-0.36	—	-0.12	
	(V _{OH} = 9.5 Vdc)		10	-0.5	—	-0.4	-0.9	—	-0.3	
	(V _{OH} = 13.5 Vdc)		15	-1.4	—	-1.2	-3.5	—	-1.0	
	(V _{OL} = 0.4 Vdc) Sink		5.0	0.52	—	0.44	0.88	—	0.36	
	I _{OL}	(V _{OL} = 0.5 Vdc)	10	1.3	—	1.1	2.25	—	0.9	mA _{dc}
		(V _{OL} = 1.5 Vdc)	15	3.6	—	3.0	8.8	—	2.4	
Input Current (AL Device)		I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	
Input Current (CL/CP Device)	I _{in}	15	—	± 0.3	—	± 0.00001	± 0.3	—	± 1.0	μA _{dc}
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μA _{dc}
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Quiescent Current (CL/CP Device) (Per Package)	I _{DD}	5.0	—	4.0	—	0.002	4.0	—	30	μA _{dc}
		10	—	8.0	—	0.004	8.0	—	60	
		15	—	16	—	0.006	16	—	120	
Total Supply Current***† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (0.80 μA/kHz) f + I _{DD} I _T = (1.60 μA/kHz) f + I _{DD} I _T = (2.40 μA/kHz) f + I _{DD}						μA _{dc}	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

I_T(C_L) = I_T(50 pF) + 2 × 10⁻³ (C_L - 50) V_{DD}f

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

Figure 4-17b. Excerpt from Motorola CMOS Data Book, Motorola, 1978, page 7-81

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.86 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Set to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — —	175 75 50 175 75 50 350 200 150	350 150 100 350 150 100 450 200 150	ns ns ns
Setup Times	t_{su}	5.0 10 15	140 50 35	70 25 17	— — —	ns
Minimum Hold Times	t_h	5.0 10 15	140 50 35	70 25 17	— — —	ns
Clock Pulse Width	t_{WH}, t_{WL}	5.0 10 15	330 110 75	165 55 38	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.0 9.0 13	1.5 4.5 6.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Set and Reset Pulse Width	t_{WH}	5.0 10 15	250 100 70	125 50 35	— — —	ns

* The formula given is for the typical characteristics only.

Figure 4-17c. Excerpt from Motorola CMOS Data Book, Motorola, 1978, page 7-82

MC14027B

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS
(J, K, Clock, and Output)

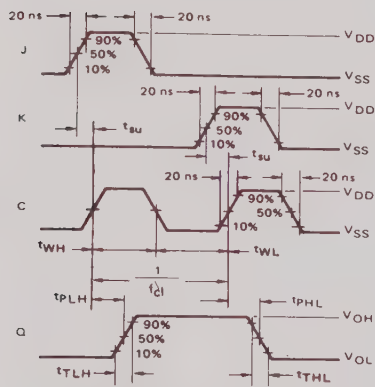
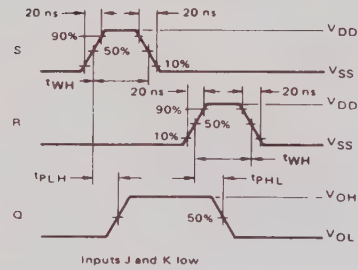
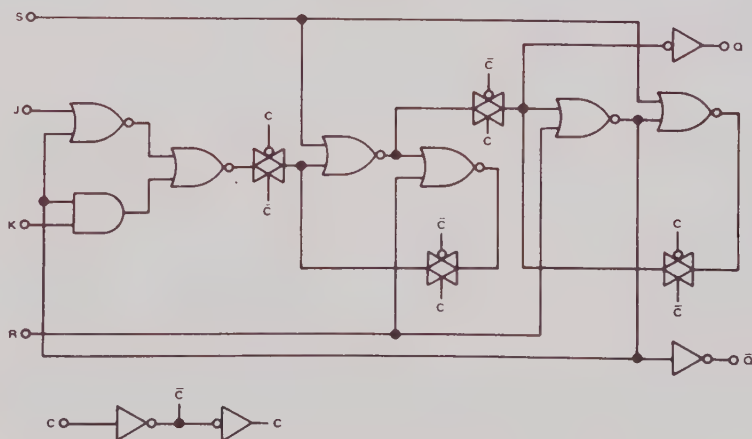


FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)



LOGIC DIAGRAM
(1/2 of Device Shown)



1732 DESCRIBE SCREEN WORKSHEET

A. Program Name: CD 4027-B

Type of Device (if different from program name) or other comment: _____

B. Number of pins per device: 16
 Number of Test Groups per Test Program: 6

C. Clocks
 C0: 1.60 MHz (One of these fifteen choices) | 8.00 2.29 1.33
 | 5.33 2.00 1.23
 | 4.00 1.78 1.14
 | 3.20 1.60 1.07
 | 2.66 1.45 1.00

Sync: C1 = C0/1 C8 = C0/8
 C2 = C0/2 CF = C0/16
X C4 = C0/4 External

D. Pin Assignments

	ID	S	ID	S	ID	S
1.	<u>0</u>		17.		33.	
2.	<u>0</u>		18.		34.	
3.	<u>1</u>		19.		35.	
4.	<u>1</u>		20.		36.	
5.	<u>1</u>		21.		37.	
6.	<u>1</u>		22.		38.	
7.	<u>1</u>		23.		39.	
8.	<u>G</u>		24.		40.	
9.	<u>1</u>		25.		41.	
10.	<u>1</u>		26.		42.	
11.	<u>1</u>		27.		43.	
12.	<u>1</u>		28.		44.	
13.	<u>1</u>		29.		45.	
14.	<u>0</u>		30.		46.	
15.	<u>0</u>		31.		47.	
16.	<u>V2</u>		32.		48.	

Definitions (for ID)

I (1,2) = Input
 O (1,2) = Output
 B = Bidirectional
 T = Tristate
 X = Don't Care
 V (1,2,3) = Power
 G = Ground

S = Pin Set
 (Default is 1)

Figure 4-18a. Describe screen worksheet for CD4027B program.

1732 RUN-MODE SCREEN WORKSHEET

A. Test Sequence: CFP (for example: CFP, CPF, F, or CP)

B.

	Bin 1	Bin 2	Bin 3	Bin 4	Bin 5	
	F	P	F	P	F	P
G 1	<u>X</u>	<u>X</u>				
R 2	<u>X</u>	<u>X</u>				
O 3		<u>X</u>				
U 4		<u>X</u>				
P 5	<u>X</u>					
S 6	<u>X</u>					

Test Procedure

C. Functional Test: Step 0 to step E

D. All Groups First Failure
 All Groups (use if binning is needed)
X Stop After Each Group
 Test Continuously to Failure
 Test Continuously

E. Single Step

F. Keyboard IS NOT Locked. (Password = up to 6 characters)

Figure 4-18b. Run-mode screen worksheet for CD4027B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 6 groups Program Name CD 4027-B

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>5</u> V	I2 = mA	<u>2.5</u> mA
V3 = V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = mA/uA	@ VIL = V	<u>0</u> V	
IIH = mA/uA	@ VIH = V	<u>5</u> V	
VOL = <u>0.4</u> V	@ IOL = <u>440</u> mA/uA	<u>1.0</u> mA/uA	
VOH = <u>4.6</u> V	@ IOH = <u>160</u> mA/uA	<u>1.0</u> mA/uA	
IZL = mA/uA	@ VZL = V		
IZH = mA/uA	@ VZH = V		
IOS = mA/uA(min)	@ VOS = V		

Figure 4-18c. Parameters screen worksheet, group 1, for CD4027B program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = mA/uA	@ VIL = V		
IIH = mA/uA	@ VIH = V		
VOL = V	@ IOL = mA/uA		
VOH = V	@ IOH = mA/uA		
IZL = mA/uA	@ VZL = V		
IZH = mA/uA	@ VZH = V		
IOS = mA/uA(min)	@ VOS = V		

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 6 groups Program Name CD 4027-B

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>15</u> V	I2 = mA	<u>8.0</u> mA
V3 = V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = <u>0.3</u> mA/uA	@ VIL = <u>0</u> V	<u>0</u> V	
IIH = <u>0.3</u> mA/uA	@ VIH = <u>15</u> V	<u>15</u> V	
VOL = <u>1.5</u> V	@ IOL = <u>3.0</u> mA/uA	<u>1.0</u> mA/uA	
VOH = <u>13.5</u> V	@ IOH = <u>1.2</u> mA/uA	<u>1.0</u> mA/uA	
IZL = mA/uA	@ VZL = V		
IZH = mA/uA	@ VZH = V		
IOS = mA/uA(min)	@ VOS = V		

(D) ----- Pin Set 2 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = mA/uA	@ VIL = V		
IIH = mA/uA	@ VIH = V		
VOL = V	@ IOL = mA/uA		
VOH = V	@ IOH = mA/uA		
IZL = mA/uA	@ VZL = V		
IZH = mA/uA	@ VZH = V		
IOS = mA/uA(min)	@ VOS = V		

Figure 4-18d. Parameters screen worksheet, group 2, for CD4027B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 6 groups Program Name CD 4027-B

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step 14

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>+1.5</u> V	I2 = <u>16.4</u> mA	<u>2.49</u> mA
V3 = - V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>0</u> V
IIH = mA/uA	@ VIH = V	<u>15</u> V
VOL = <u>1.5</u> V	@ IOL = mA/uA	<u>20</u> mA (<u>uA</u>)
VOH = <u>13.5</u> V	@ IOH = mA/uA	<u>20</u> mA (<u>uA</u>)
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

Figure 4-18e. Parameters screen worksheet, group 3, for CD4027B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 4 of 6 groups Program Name CD 4027 B

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step 14

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>+1.5</u> V	I2 = <u>4.04</u> mA	<u>2.49</u> mA
V3 = - V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>0</u> V
IIH = mA/uA	@ VIH = V	<u>5</u> V
VOL = <u>0.4</u> V	@ IOL = mA/uA	<u>20</u> mA (<u>uA</u>)
VOH = <u>4.6</u> V	@ IOH = mA/uA	<u>20</u> mA (<u>uA</u>)
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

Figure 4-18f. Parameters screen worksheet, group 4, for CD4027B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 5 of 6 groups Program Name CD 4027-BPower Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	mA
V2 = <u>+5</u> V	I2 = mA	<u>2.5</u> mA
V3 = - V	I3 = mA	mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>1.5</u> V
IIH = mA/uA	@ VIH = V	<u>3.5</u> V
VOL = <u>0.5</u> V	@ IOL = mA/uA	<u>1.0</u> mA <u>uA</u>
VOH = <u>4.5</u> V	@ IOH = mA/uA	<u>1.0</u> mA <u>uA</u>
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min) _____ mA/uA(max)	@ VOS = V	

Figure 4-18g. Parameters screen worksheet, group 5, for CD4027B program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min) _____ mA/uA(max)	@ VOS = V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 6 of 6 groups Program Name CD 4027-BPower Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	mA
V2 = <u>+15</u> V	I2 = mA	<u>8.0</u> mA
V3 = - V	I3 = mA	mA

Figure 4-18h. Parameters screen worksheet, group 6, for CD4027B program.

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>4.0</u> V
IIH = mA/uA	@ VIH = V	<u>11.0</u> V
VOL = <u>1.5</u> V	@ IOL = mA/uA	<u>1.0</u> mA <u>uA</u>
VOH = <u>13.5</u> V	@ IOH = mA/uA	<u>1.0</u> mA <u>uA</u>
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min) _____ mA/uA(max)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min) _____ mA/uA(max)	@ VOS = V	

1732 TRUTH-TABLE WORKSHEET

SHEET 1 of 1

Device Number if different from program name. PROGRAM NAME: **CD 4027-B**

Pin Number:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	STEP
ID:	0	0	1	1	1	1	1	G	1	1	1	1	1	0	0	V	0
0	0	1	0	1	0	0	0	G	1	0	0	0	0	0	1	V	0
1	1	0	1	0	1	1	1	G	0	1	1	1	1	1	0	V	1
2	0	1	0	1	1	1	0	G	1	1	1	0	0	0	1	V	2
3	1	1	1	1	1	1	1	G	1	1	1	1	1	1	1	V	3
4	0	1	0	1	1	1	0	G	1	1	1	0	0	0	1	V	4
5	1	0	1	0	1	1	0	G	0	1	1	0	1	1	0	V	5
6	1	0	0	0	1	1	0	G	0	1	0	0	0	1	0	V	6
7	0	1	1	0	1	1	0	G	0	1	0	0	1	0	1	V	7
8	0	1	0	0	0	0	0	G	0	1	0	0	0	0	1	V	8
9	0	1	1	0	0	0	0	G	0	1	0	0	1	0	1	V	9
10	1	0	0	0	0	0	1	G	0	1	1	0	0	0	1	V	10
1	1	0	1	0	0	0	0	G	0	1	1	0	1	1	0	V	1
2	1	0	0	0	0	0	0	G	0	0	1	0	0	1	0	V	2
3	1	0	1	0	0	0	0	G	0	0	1	0	1	1	0	V	3
4	X	X	0	1	1	1	0	G	1	1	1	0	0	X	X	V	4
5	E																5
6																	6
7																	7
8																	8
9																	9
0																	0

Figure 4-18I. Truth-table screen worksheet for CD4027B program. This worksheet shows the characters 1 and 0 where the display screen would show 1 and 0 in reverse video.

4.9.8 Program Example, MC4043B Figures 4-19 and 4-20

The MC4043B is a quad NOR R-S Latch with tristate outputs. The data sheets (Figure 4-19 a and b) show that all 4 R-S latches have a common enable line.

Worksheet Organization.

Most of the values for the worksheets are derived from the standardized JEDEC specifications sheet. Those values which are not derived from the JEDEC specifications will be described as each worksheet is discussed.

Describe Screen. Voltages for this device are referenced to Vss, so pin 8 will be coded G. The formulas are used to determine the clock frequency. The worst-case timing is 1395 ns, and the nearest programmable frequency is 727 kHz. This doesn't allow much delay for marginal devices, so the next lower frequency, 667 kHz, is entered instead.

Gate/Strobe Setting. Based on a period of 1500 ns, there will be 24 period units. The gate should be set 312.5 ns after the start of the clock pulse, at 5 units, and the strobe should be set at 23 units in order to gate and strobe the device properly.

Parameters Group 1. Vdd for this group is 5 volts. I-max is calculated using the formula found in para 4.9.3 and the values for IOH(para) and Idd(static) listed in Figure 4-19b.

$$\begin{aligned} I\text{-max} &= \left(\left\{ 1 \mu\text{A} + 200 \text{ pF} \times 667 \text{ kHz} \times 5 \text{ V} \right\} \times 4 \right) + \\ &\quad 160 \mu\text{A} + 20 \mu\text{A} \times 1.25 \\ &= \left(\left\{ 668 \mu\text{A} \times 4 \right\} + 180 \mu\text{A} \right) \times 1.25 \\ &= 3.5 \text{ mA (rounded up)} \end{aligned}$$

Since this is a tristate device, the standard parametric values for IOL and IOH are entered in both the parametric and functional test condition columns.

Parameters Group 2. Vdd for this group is 15 volts. I-max is calculated in the same way as in group 1, using the values for IOH(para) and Idd(static) listed in Figure 4-19b for the new Vdd.

$$\begin{aligned} I\text{-max} &= \left(\left\{ 1 \mu\text{A} + 200 \text{ pF} \times 667 \text{ kHz} \times 15 \text{ V} \right\} \times 4 \right) + \\ &\quad 1.2 \text{ mA} + 80 \mu\text{A} \times 1.25 \\ &= \left(\left\{ 2.001 \text{ mA} \times 4 \right\} + 1.280 \text{ mA} \right) \times 1.25 \\ &= 11.6 \text{ mA (rounded up)} \end{aligned}$$

The standard parametric IOL and IOH values are entered in both the parametric and functional test condition columns in this group also. The high-impedance leakage current is tested in this group, so the standard value is entered and tested at 0 and 15 volts.

Parameters Group 3. The power-supply test is performed at 15 volts in this group. The value of Idd(max) is entered from the DUT data sheets. I-max is limited to 2.49 mA because of the PS2 current limit in the low R-sense range. Note that the functional values of IOH and IOL are set at 0.0 μA .

Parameters Group 4. The power-supply test is performed at 5 volts in this group.

Parameters Group 5. This group tests the threshold levels at 5 volts. I-max is the same as in group 1. Because this is a tristate device, enter the parametric values for IOL and IOH in the functional test condition column.

Parameters Group 6. This group tests the threshold levels at 15 volts. I-max is the same as in group 2. The parametric values for IOL and IOH are entered in the functional test condition column for this group also.

Truth Table. The truth table steps through all the possible input combinations with the enable input high, and then tests for an output with the enable input low and all other inputs high. The power supply is tested on step 9.

Run-mode screen. As noted in para 4.9.5, groups 1 and 2 are tested both functionally and parametrically, groups 3 and 4 are tested only parametrically, and groups 5 and 6 are tested only functionally. The functional test step default values are entered.



MOTOROLA

CMOS MSI QUAD R-S LATCHES

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

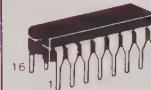
- Quiescent Current = 4.0 nA/pkg typical @ 10 Vdc
- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load, or Two HTL Loads Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

MC14043B

QUAD "NOR" R-S LATCH

MC14044B

QUAD "NAND" R-S LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package
	A	Extended Operating Temperature Range
	C	Limited Operating Temperature Range

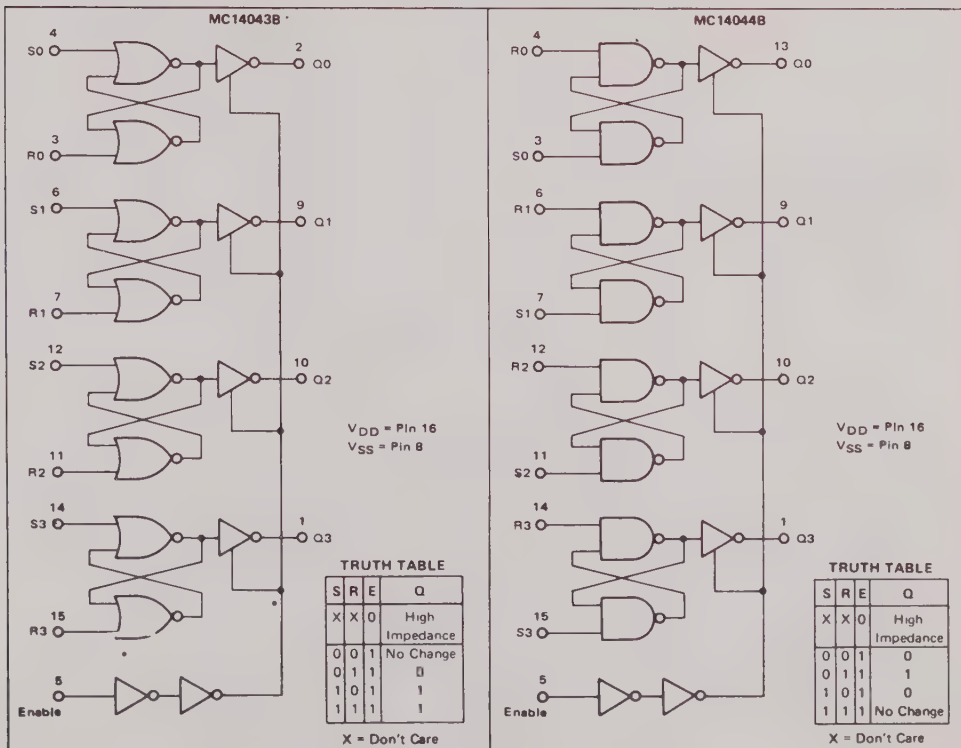


Figure 4-19a. Excerpt from Motorola CMOS Data Book, Motorola, 1978, page 120.

MC14043B • MC14044B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level V _{OL}	5.0		0.05		0	0.05		0.05	Vdc
		10		0.05		0	0.05		0.05	
		15		0.05		0	0.05		0.05	
	"1" Level V _{OH}	5.0	4.95		4.95	5.0		4.95		Vdc
		10	9.95		9.95	10		9.95		
		15	14.95		14.95	15		14.95		
Input Voltage* (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0		1.5	—	2.25	1.5		1.5	Vdc
		10	—	3.0	—	4.50	3.0		3.0	
		15	—	4.0	—	6.75	4.0		4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75		3.5	—	Vdc
		10	7.0	—	7.0	5.50		7.0	—	
		15	11.0	—	11.0	8.25		11.0	—	
Output Drive Current (AL Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	2.4	-4.2		1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88		-0.36	—	
		10	-1.6	—	-1.3	-2.25		-0.9	—	
		15	-4.2	—	-3.4	8.8		-2.4	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88		0.36	—	mAdc
		10	1.6	—	1.3	2.25		0.9	—	
		15	4.2	—	3.4	8.8		2.4	—	
Output Drive Current (CL/CP Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-2.5	—	-2.1	4.2		-1.7	—	mAdc
		5.0	-0.52	—	-0.44	-0.88		-0.36	—	
		10	-1.3	—	-1.1	-2.25		-0.9	—	
		15	-3.6	—	-3.0	-8.8		-2.4	—	
	Sink I _{OL}	5.0	0.52	—	0.44	0.88		0.36	—	mAdc
		10	1.3	—	1.1	2.25		0.9	—	
		15	3.6	—	3.0	8.8		2.4	—	
Input Current (AL Device)	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Current (CL/CP Device)	I _{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Quiescent Current (CL/CP Device) (Per Package)	I _{DD}	5.0	—	4.0	—	0.002	4.0	—	30	μAdc
		10	—	8.0	—	0.004	8.0	—	60	
		15	—	16	—	0.006	16	—	120	
Total Supply Current*** (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all outputs switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD} I _T = (1.15 μA/kHz) f + I _{DD} I _T = (1.73 μA/kHz) f + I _{DD}							μAdc
		10								
		15								
Three-State Output Leakage Current (AL Device)	I _{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μAdc
Three-State Output Leakage Current (CL/CP Device)	I _{TL}	15	—	±1.0	—	±0.0001	±1.0	—	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device

T_{high} = +125°C for AL Device, +85°C for CL/CP Device

#Noise immunity specified for worst-case input combination

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF

I_T(C_L) = I_T(50 pF) + 4 × 10⁻³ (C_L - 50) V_{DD}f

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency

**The formulas given are for the typical characteristics only at 25°C

Figure 4-19b. Excerpt from Motorola CMOS Data Book, Motorola, 1978, page 121.

MC14043B • MC14044B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Pin	I	10	mA _{dc}
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15	— — —	175 75 60	350 175 120	ns
Set Pulse Width	t_{WH}	5.0 10 15	200 100 70	80 40 30	— — —	ns
Reset Pulse Width	t_{WH}	5.0 10 15	200 100 70	80 40 30	— — —	ns
Three-State Enable/Disable Delay t_{PLZ} t_{PHZ}	t_{PLZ} t_{PHZ}	5.0 10 15	— — —	150 80 55	300 160 110	ns

* The formulas given are for the typical characteristics only.

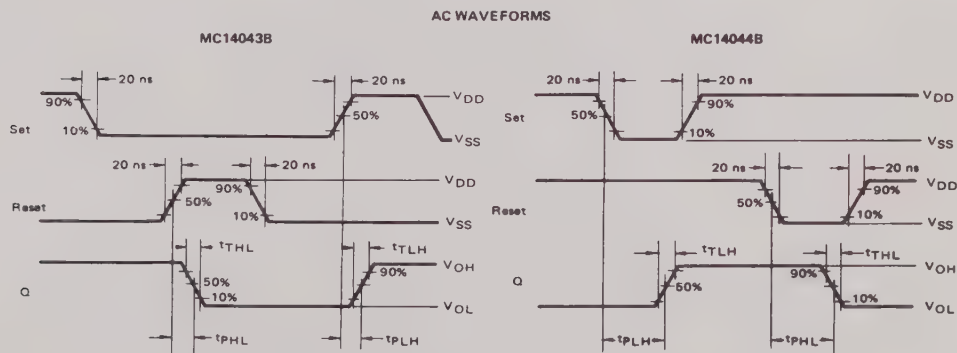


Figure 4-19c. Excerpt from Motorola CMOS Data Book, Motorola, 1978, page 122.

THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, and Switch Conditions for 3-State Tests.

TEST	S	R	MC14043B		MC14044B		
			S1	S2	Q	S1	S2
t _{PLZ}	V _{DD}	V _{SS}	Open	Closed	A	Closed	Open
t _{PLZ}	V _{SS}	V _{DD}	Closed	Open	B	Open	Closed
t _{PHZ}	V _{DD}	V _{SS}	Open	Closed	A	Closed	Open
t _{PHZ}	V _{SS}	V _{DD}	Closed	Open	B	Open	Closed

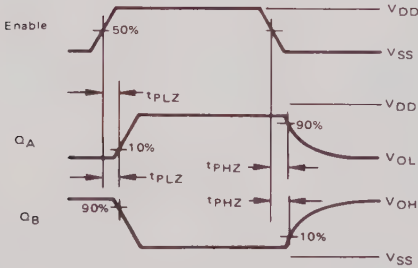
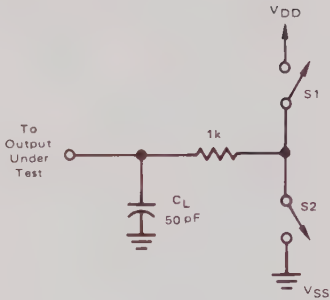


Figure 4-19d. Excerpt from Motorola CMOS Data Book, Motorola, 1978, page 123.

1732 DESCRIBE SCREEN WORKSHEET

A. Program Name: MC4043B

Type of Device (if different from program name) or other comment: _____

B. Number of pins per device: 16
 Number of Test Groups per Test Program: 6

C. Clocks
 C0: 2.66 MHz (One of these fifteen choices) | 8.00 2.29 1.33
 | 5.33 2.00 1.23
 | 4.00 1.78 1.14
 | 3.20 1.60 1.07
 | 2.66 1.45 1.00

Sync: ☐ C1 = C0/1 ☐ C8 = C0/8
☐ C2 = C0/2 ☐ CF = C0/16
☒ C4 = C0/4 ☐ External

D. Pin Assignments

	ID	S	ID	S	ID	S
1.	<u>I</u>		17.		33.	
2.	<u>I</u>		18.		34.	
3.	<u>I</u>		19.		35.	
4.	<u>I</u>		20.		36.	
5.	<u>I</u>		21.		37.	
6.	<u>I</u>		22.		38.	
7.	<u>I</u>		23.		39.	
8.	<u>G</u>		24.		40.	
9.	<u>I</u>		25.		41.	
10.	<u>I</u>		26.		42.	
11.	<u>I</u>		27.		43.	
12.	<u>I</u>		28.		44.	
13.	<u>X</u>		29.		45.	
14.	<u>I</u>		30.		46.	
15.	<u>I</u>		31.		47.	
16.	<u>V2</u>		32.		48.	

Definitions (for ID)

I (1,2) = Input
 O (1,2) = Output
 B = Bidirectional
 T = Tristate
 X = Don't Care
 V (1,2,3) = Power
 G = Ground

S = Pin Set
 (Default is 1)

Figure 4-20a. Describe screen worksheet for MC4043B program.

1732 RUN-MODE SCREEN WORKSHEET

A. Test Sequence: CFP (for example: CFP, CPF, F, or CP)

B.

	Bin 1	Bin 2	Bin 3	Bin 4	Bin 5	
	F	P	F	P	F	P
G 1	<u>X</u>	<u>X</u>				
R 2	<u>X</u>	<u>X</u>				
O 3		<u>X</u>				
U 4		<u>X</u>				
P 5	<u>X</u>					
S 6	<u>X</u>					

Test Procedure

C. Functional Test: Step 0 to step E

D. ☐ All Groups First Failure
☐ All Groups (use if binning is needed)
☒ Stop After Each Group
☐ Test Continuously to Failure
☐ Test Continuously

E. ☐ Single Step

F. Keyboard IS NOT Locked. (Password = up to 6 characters)

Figure 4-20b. Run-mode screen worksheet for MC4043B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 6 groups Program Name MC 4043 BPower Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>5</u> V	I2 = mA	<u>3.5</u> mA
V3 = - V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions Parametric	Functional
IIL = mA/uA	@ VIL = V	0 V
IIH = mA/uA	@ VIH = V	5 V
VOL = <u>0.4</u> V	@ IOL = <u>440</u> mA/uA	<u>440</u> mA/uA
VOH = <u>4.60</u> V	@ IOH = <u>160</u> mA/uA	<u>160</u> mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

Figure 4-20c. Parameters screen worksheet,
group 1, for MC4043B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 6 groups Program Name MC 4043 BPower Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>15</u> V	I2 = mA	<u>11.6</u> mA
V3 = - V	I3 = mA	

Figure 4-20d. Parameters screen worksheet,
group 2, for MC4043B program.

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions Parametric	Functional
IIL = <u>0.3</u> mA/uA	@ VIL = 0 V	0 V
IIH = <u>0.3</u> mA/uA	@ VIH = <u>15</u> V	<u>15</u> V
VOL = <u>1.5</u> V	@ IOL = <u>3.00</u> mA/uA	<u>3.00</u> mA/uA
VOH = <u>13.5</u> V	@ IOH = <u>1.2</u> mA/uA	<u>1.2</u> mA/uA
IZL = <u>16</u> mA/uA	@ VZL = 0 V	
IZH = <u>16</u> mA/uA	@ VZH = <u>15</u> V	
IOS = mA/uA(min)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 6 groups Program Name MC 4043 BPower Supplies (1, 2, 3)(A) Power Supplies tested at step 9(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>+1.5</u> V	I2 = <u>16.0 uA</u>	<u>2.49</u> mA
V3 = - V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>0</u> V
IIH = mA/uA	@ VIH = V	<u>1.5</u> V
VOL = <u>1.5</u> V	@ IOL = mA/uA	<u>20</u> mA <u>uA</u>
VOH = <u>13.5</u> V	@ IOH = mA/uA	<u>20</u> mA <u>uA</u>
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

Figure 4-20e. Parameters screen worksheet, group 3, for MC4043B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 4 of 6 groups Program Name MC 4043 BPower Supplies (1, 2, 3)(A) Power Supplies tested at step 9(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + V	I1 = mA	
V2 = <u>+5</u> V	I2 = <u>4 uA</u>	<u>2.49</u> mA
V3 = - V	I3 = mA	

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	<u>0</u> V
IIH = mA/uA	@ VIH = V	<u>5</u> V
VOL = <u>0.4</u> V	@ IOL = mA/uA	<u>20</u> mA <u>uA</u>
VOH = <u>4.60</u> V	@ IOH = mA/uA	<u>20</u> mA <u>uA</u>
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = mA/uA	@ VIL = V	V
IIH = mA/uA	@ VIH = V	V
VOL = V	@ IOL = mA/uA	mA/uA
VOH = V	@ IOH = mA/uA	mA/uA
IZL = mA/uA	@ VZL = V	
IZH = mA/uA	@ VZH = V	
IOS = mA/uA(min)	@ VOS = V	

Figure 4-20f. Parameters screen worksheet, group 4, for MC4043B program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 5 of 6 groups Program Name MC 4043 B

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = <u>+5</u> V	I2 = _____ mA	<u>3.5</u> mA
V3 = _____ V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>1.5</u> V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	<u>3.5</u> V	_____ V
VOL = <u>0.5</u> V	@ IOL = _____ mA/uA	<u>440</u> mA/uA	_____ mA/uA
VOH = <u>4.50</u> V	@ IOH = _____ mA/uA	<u>160</u> mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	_____ V	_____ V
IZH = _____ mA/uA	@ VZH = _____ V	_____ V	_____ V
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V	_____ V

Figure 4-20g. Parameters screen worksheet, group 5, for MC4043B program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	_____ V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	_____ V	_____ V
VOL = _____ V	@ IOL = _____ mA/uA	_____ mA/uA	_____ mA/uA
VOH = _____ V	@ IOH = _____ mA/uA	_____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	_____ V	_____ V
IZH = _____ mA/uA	@ VZH = _____ V	_____ V	_____ V
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V	_____ V

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 6 of 6 groups Program Name MC 4043 BPower Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = <u>+15</u> V	I2 = _____ mA	<u>11.6</u> mA
V3 = _____ V	I3 = _____ mA	_____ mA

Figure 4-20h. Parameters screen worksheet, group 6, for MC4043B program.

(C) ----- Pin Set 1 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>4.0</u> V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	<u>11.0</u> V	_____ V
VOL = <u>1.5</u> V	@ IOL = _____ mA/uA	<u>3.00</u> mA/uA	_____ mA/uA
VOH = <u>13.5</u> V	@ IOH = _____ mA/uA	<u>1.20</u> mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	_____ V	_____ V
IZH = _____ mA/uA	@ VZH = _____ V	_____ V	_____ V
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V	_____ V

(D) ----- Pin Set 2 -----

Parametric Test Limits	Parametric	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	_____ V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	_____ V	_____ V
VOL = _____ V	@ IOL = _____ mA/uA	_____ mA/uA	_____ mA/uA
VOH = _____ V	@ IOH = _____ mA/uA	_____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	_____ V	_____ V
IZH = _____ mA/uA	@ VZH = _____ V	_____ V	_____ V
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V	_____ V

Device Number if different from program name. PROGRAM NAME: *MC4043B*

Pin Number:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	STEP
ID:	<i>T</i>	<i>T</i>	<i>I</i>	<i>I</i>	<i>I</i>	<i>I</i>	<i>I</i>	<i>G</i>	<i>T</i>	<i>T</i>	<i>I</i>	<i>I</i>	<i>X</i>	<i>I</i>	<i>I</i>	<i>V</i>	
0	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>G</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>X</i>	<i>i</i>	<i>i</i>	<i>V</i>	0
1	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>G</i>	<i>0</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>X</i>	<i>i</i>	<i>i</i>	<i>V</i>	1
2	<i>i</i>	<i>0</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>i</i>	<i>0</i>	<i>G</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>X</i>	<i>i</i>	<i>i</i>	<i>V</i>	2
3	<i>i</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>G</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>0</i>	<i>X</i>	<i>i</i>	<i>i</i>	<i>V</i>	3
4	<i>0</i>	<i>i</i>	<i>0</i>	<i>0</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>G</i>	<i>i</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>X</i>	<i>0</i>	<i>i</i>	<i>V</i>	4
5	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>G</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>X</i>	<i>i</i>	<i>0</i>	<i>V</i>	5
6	<i>i</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>i</i>	<i>0</i>	<i>0</i>	<i>G</i>	<i>i</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>X</i>	<i>0</i>	<i>0</i>	<i>V</i>	6
7	<i>0</i>	<i>0</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>G</i>	<i>0</i>	<i>0</i>	<i>i</i>	<i>0</i>	<i>X</i>	<i>0</i>	<i>i</i>	<i>V</i>	7
8	<i>T</i>	<i>T</i>	<i>i</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>i</i>	<i>G</i>	<i>T</i>	<i>T</i>	<i>i</i>	<i>i</i>	<i>X</i>	<i>i</i>	<i>i</i>	<i>V</i>	8
9	<i>X</i>	<i>X</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>0</i>	<i>i</i>	<i>G</i>	<i>X</i>	<i>X</i>	<i>i</i>	<i>0</i>	<i>X</i>	<i>0</i>	<i>i</i>	<i>V</i>	9
0																	0
1																	1
2																	2
3																	3
4																	4
5																	5
6																	6
7																	7
8																	8
9																	9
0																	0

Figure 4-20i. Truth table screen worksheet for MC4043B program. This worksheet shows the characters *i* and *o* where the display screen would show 1 and 0 in reverse video.

Table 4-10
COMPARISON OF DEVICE FAMILY PARAMETERS

Parameter	ECL*		TTL		CMOS	
	Min	Max	Min	Max	Min	Max
VIL	-1.53 V	---	---	0.8 V	---	1.5 ... 4.0 V
VIH	---	-1.05 V	2.0 V	---	3.5 ... 11.0 V	---
VOL	-1.85 V	-1.65 V	---	0.4 V	---	0.05 V
VOH	-0.96 V	-0.81 V	2.4 V	---	4.95 ... 14.95 V	---
Supply Voltage:						
Vee	-5.2 V	-5.2 V	---	---	---	---
Vcc	---	---	4.75 V	5.25 V	---	---
Vdd	---	---	---	---	5.0 V	15.0 V

*In the 1732, minimum refers to the least positive value of a parameter, while maximum refers to the most positive value of a parameter.

4.10 PROGRAMMING FOR ECL DEVICES

4.10.1 General

At present, the ECL devices listed in the program library are all MECL 10,000 devices produced by Motorola.

Therefore, this discussion will use the specifications from the **MECL Data Book** by Motorola. Note that these specifications are quite different from those used in TTL and CMOS, as shown Table 4-10.

4.10.2 I-max Selection

The formula for I-max for ECL devices is given below:
 $I_{\text{max}} = 1.25 \times I_{\text{EE}}$

4.10.3 Functional Test Structure

The 1732 was designed to source current for IOL and sink it for IOH; ECL devices source current for both IOL and IOH. ECL clock frequencies exceed those available on the system, so ECL devices cannot be exercised at their full speed. Finally, ECL devices require pulldown resistors to compensate for the emitter follower configuration of their circuitry, but this can be compensated for a manner similar to that used for TTL devices with open collectors (refer to para 4.8.5). In order to understand the technique used in the functional testing of ECL, the theory of the active load in the 1732 should be reviewed. (Refer to para 6.2.3.)

Functional Testing of ECL Devices.

The functional testing of ECL devices presents a problem in that the output of an ECL device will source current into a load for both VOL and VOH. IOH is normally drawn from the DUT by the action of the active load as shown in Figure 4-21. IOL is normally sourced to the DUT by the active load, but must be drawn from the output of an ECL device to insure proper operation of the DUT. To force the diode bridge to sink current from a DUT, Vmid must be lower than the device's VOL by the voltage drop across a diode junction. On the other hand, Vmid must exceed the device's VIL by at least 250 mV in order to enable IOH to sink the current. Thus, for the active load to sink current from a low output, VOL must be somewhat greater than Vmid and VIL must be less than Vmid. If all the current is to be drawn through CR4, then VOL minus 0.7 V must exceed Vmid and Vmid plus 0.25 V must exceed VIL. The following values can be obtained from the Motorola **MECL Data Book** (all referenced values are at 25 degrees C):

$$\begin{aligned}V_{OL}(\text{min}) &= -1.65 \text{ V} \\V_{OH}(\text{min}) &= -0.96 \text{ V} \\V_{IL} &= -1.475 \text{ V} \\V_{\text{mid}} &= (V_{OH} + V_{OL})/2 \\V_{\text{mid}} &= (-0.96 \text{ V} + -1.65 \text{ V})/2 = -1.31 \text{ V}\end{aligned}$$

To force the active load to sink current for a low output of an ECL device, the value of Vout can be determined as follows:

$$\begin{aligned}V_{\text{out}} &= V_{\text{mid}} + 0.7 \text{ V} \\V_{\text{out}} &= -1.31 \text{ V} + 0.7 \text{ V} = -0.61 \text{ V}\end{aligned}$$

Active load current sinking is enabled when Vmid minus 250 mV is equal to or more positive than VIL.

$$\begin{aligned}V_{IL} &= V_{\text{mid}} - 0.25 \text{ V} \\V_{IL} &= -1.31 - 0.25 \text{ V} = -1.56 \text{ V}\end{aligned}$$

With normal values of input and output voltages for non-ECL devices, the current sink can be enabled, but the DUT output has an insufficient VOL to operate the diode bridge. VOL is not controlled by the tester directly, and any change in the expected Vout would pass a bad DUT (it has the effect of raising the minimum value of VOL). Therefore, in order to keep the socket adaptor simple and pass only good devices, the active load is used as an active pulldown for functional testing. This technique is similar to the technique used in testing open collector TTL devices (refer to para 4.8.5).

By using pin set 1 for inputs and pin set 2 for outputs, the VIH and VIL of pin set 2 can be set to any desired value

Figure 4-21

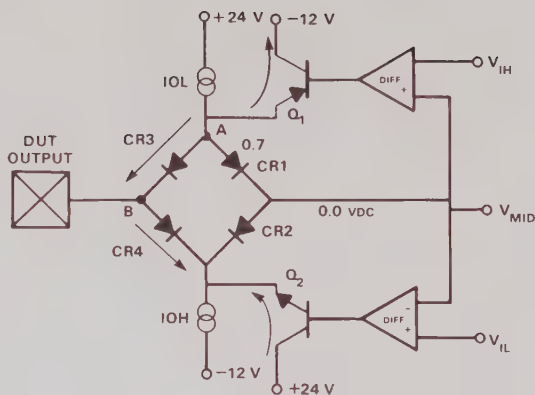


Figure 4-21. Simplified diagram of the functional active load.

without affecting the operation of the device. Pin set 2 is used to force the active load to act as an active pulldown. Note that the intent is to have IOH act as the current sink for both output states of the DUT. To calculate the values necessary to make the active load work in this manner, the capabilities and level interactions of the system must be known. System capabilities are listed below.

$$\begin{aligned}V_{in}(\text{min}) &= -2.5 \text{ V functional (driver)} \\V_{out}(\text{min}) &= -2.5 \text{ V functional (sensor)} \\IOH(\text{max}) &= 0.8 \text{ mA functional}\end{aligned}$$

System level interaction is discussed in the theory of the active load (refer to para 6.2.3). For IOH to be enabled in a given pin set and the active load to act as a current sink, two conditions must be met. First, Vmid plus 0.25 V must equal or exceed VIL for that pin set. Second, the output of the device (Vout) must be greater than or equal to Vmid plus 0.7 V. To simplify ECL testing (and for reasons which will become apparent later), the output logic states of ECL devices are limited to a high (logic 1) and a high-impedance (logic T) state.

ECL devices source current for both high and low output states; the system sources current for a low output and sinks it for a high. VOL and VOH are used to determine Vmid for that pin set. IOH is designated as the value which results when Vout is greater than Vmid. This means that there is no way to source current to the ECL DUT when the output is in the low state (logic 0). By limiting the output code entries in the truth table to 1 and T and setting Vmid more negative than an output logic 0, the system will never see a logic 0 at the output of the DUT. This means that the DUT output will never have to sink IOL. Modification of the values entered in pin set 2 will permit this form of operation of the DUT. Since pin set 1 is used to test the inputs only and pin set 2 is used to test the outputs only, VIL and VIH in pin set 2 can be set to whatever values are necessary to make the system work.

The only remaining problem is how to enable IOH and IOL while keeping Vmid at a value which will ensure proper operation of the diode bridge when testing ECL devices. The screen entries which will enable the current loads are VIL, VIH, VOL, and VOH. Since the functional test states are highs and high-impedance (1s and Ts), the only value used in the functional test that relates to the ECL Vout and is specified by the manufacturer's data sheets in the

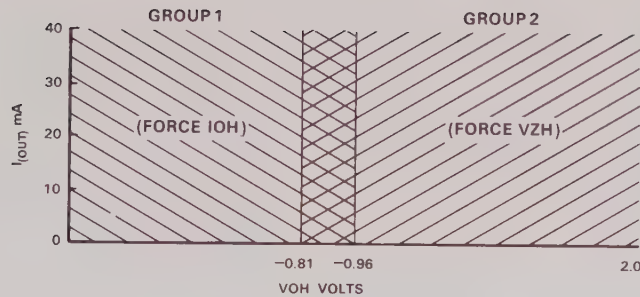


Figure 4-22. VOH testing of an ECL device.

value for VOH of -0.96 V. To force Vmid to be less than VOL(min), the screen entry for VOL must be more negative than the value of VOL expected from the DUT. The testing for the actual values of VOL and VOH is performed by the parametric measurement unit at the rated load.

Vmid must be more negative than VOL(min); thus Vmid(max) is calculated using the formula

$$V_{mid} = \frac{VOL(max) [system] + V_{OH}(min)}{2}$$

where VOL(max) [system] equals -2.5 V.

Substituting for VOL and VOH:

$$V_{mid} = \frac{-2.5 \text{ V} + -0.96 \text{ V}}{2} = -1.73 \text{ V}$$

With a VOL of -2.5 V, a VOH of -0.96 V, and a Vmid of -1.73 V, the diode bridge will always sink current from an ECL output. IOL will never be seen by the DUT, and IOH will be the actual functional load on the DUT at all times.

The enabling of the current generators can now be addressed. To enable IOH, VIL must be more negative than Vmid by at least 250 mV. With Vmid equaling -1.73 V, VIL is selected at the system limit of -2.5 V to ensure the enabling of the IOH current generator. In order to ensure proper operation of the diode bridge and to enable IOL current

generator, the value of VIH is set to 0.0 V. This produces the following set of parameters for pin set 2:

$$\begin{aligned} V_{IL}(func) &= -2.5 \text{ V} \\ V_{IH}(func) &= 0.0 \text{ V} \\ VOL &= -2.5 \text{ V} \\ V_{OH} &= -0.96 \text{ V at } I_{OH}(func) = 8 \text{ mA} \end{aligned}$$

Now when the ECL DUT output is in a logic state, the active load will draw 8 mA from the DUT. If Vout is greater (i.e., more positive) than -0.96 V, a logic 1 is sensed. If Vout is less (i.e., more negative) than -0.96 V but greater than the VOL value of -2.5 V, a high-impedance state T is sensed. Since the ECL output low (-1.65 V at 7 mA to -1.85 V at 3 mA) is no more negative than VOL, some portion (2.5 to 3.0 mA) of IOH will be drawn from the DUT output. This 2.5 to 3.0 mA load is not quite the load specified at a logic 0 of -1.81 V (the specified value is 3.0 mA), but it will ensure that the output is less than VOH and at some value close to VOL.

4.10.4 Parametric Test Structure Figures 4-22 through 4-24

The selected approach for the parametric test of an ECL device uses two groups to bracket the minimum and maximum values of VOH and VOL. Group 1 is used to test for a VOL less positive than or equal to -1.65 V and a VOH less negative than -0.96 V, testing one pair of the output voltage limits. Group 2 tests the other pair of voltage limits, i.e., VOL less negative than -1.85 V and VOH less positive than or equal to -0.81 V. If a DUT passes the parametric VOH tests of both groups 1 and 2, VOH must be between -0.81 V and -0.96 V, as seen in Figure 4-22

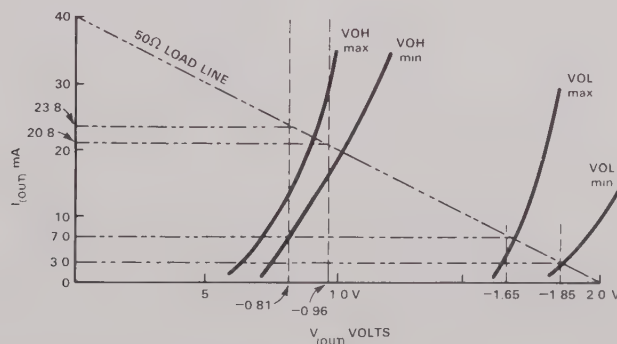


Figure 4-23. ECL output voltage level versus dc loading curve.

which shows the VOH testing of an ECL device. This is also true for VOL; if the DUT passes, then VOL must be between -1.65 V and -1.85 V.

Using two groups to test for Vout minimum and maximum values instead of one group with its associated alternate parameters screen is necessary because of the two different Iout values for the minimum and maximum Vout values.

IOH and IOL Selection.

Unlike TTL and CMOS data sheets, the ECL data sheets do not list values for IOH and IOL. These values must be calculated by the user. The data sheet that outputs are tested when terminated through a 50-ohm resistor to -2 volts. The logic 1 voltage levels are:*

VOH(max) -0.81 V at RL = 50 ohms to -2.0 V

VOH(min) -0.96 V at RL = 50 ohms to -2.0 V

The logic 0 voltage levels are:*

VOL(max) -1.65 V at RL = 50 ohms to -2.0 V

VOL(min) -1.85 V at RL = 50 ohms to -2.0 V

These voltages are specified with the output driving a 50-ohm load termination to -2.0 Vdc at 25 degrees C. Using the 50-ohm load termination and the minimum and maximum values for Vout, the output currents can be determined as follows:

$$IOH(max) = \frac{-0.81 - (-2 \text{ volts})}{50 \text{ ohms}} = 23.8 \text{ mA}$$

$$IOH(min) = \frac{-0.96 - (-2 \text{ volts})}{50 \text{ ohms}} = 20.8 \text{ mA}$$

$$IOL(max) = \frac{-1.65 - (-2 \text{ volts})}{50 \text{ ohms}} = 7.0 \text{ mA}$$

$$IOL(min) = \frac{-1.85 - (-2 \text{ volts})}{50 \text{ ohms}} = 3.0 \text{ mA}$$

These output currents could also be derived from Figure 4-23 showing the ECL output voltage level versus dc loading curve using the Vout listed.

Parametric Testing of ECL Devices.

Once the minimum and maximum values of output current and voltage have been determined, the structure of the parametric tests can be planned. Two different tests must be used to test the minimum and maximum limits of logic highs and lows. Since ECL devices always source current, the tests that the system uses must always sink current. The normal VOL parametric test (VOL sense, IOL force) can't be used because the system sources current during a VOL test. The normal VOH parametric test (VOH sense, IOH force) sinks current, so it can be used to test the minimum limit of VOH.

The IZH test can be used to test the maximum value of current. It forces a voltage on a pin that has been defined as a logic T in the high-impedance state and tests for a value of current. VOH and IZH tests can be used in combination to bracket the minimum and maximum limits of a given logic level. Since IZH is tested only when the pin is

coded T, while VOH is tested only when the pin is coded 1, the parametric test must be divided into two groups.

The actual outputs of the device are determined by the logic states entered in the truth table for the input pins rather than the logic states specified for the outputs. Since the ECL outputs are either a logic 1 or a logic T, as defined by the test procedure, the logic 1 allows normal IOH forcing and VOH testing. The logic T can also be used for parametric testing in the following manner. The logic states defined in the truth table for the outputs are the expected functional results. These output logic states also dictate what parametric test will be performed on a particular pin at a given step of the truth table.

Testing the two limits of the logic low can be done in the same way that the two limits of the logic high were tested, except that the VOL test sources current so VOH and IZH are used in place of the expected VOL. The minimum limit of one logic level can be tested in the same group where the other logic level is being tested for its maximum level, taking advantage of the fact that the actual output of the device is determined by the inputs fed to it rather than the logic state specified for it in the truth table.

The part of the truth table that deals with the parametric test is divided into two portions, one to test VOL(min) and VOH(max) and another to test VOH(min) and VOL(max). In each portion the pattern of the inputs is identical, while the logic codes of the DUT's outputs are reversed. The output states of the DUT are redefined as reverse logic states for the parametric tests. Where a logic high will be coded as a 1 to test VOH(min) and as a T to test VOH(max), a logic low can also be defined as a 1 to test VOL(min) and as a T to test VOL(max). This means that in group 1, a logic high will be a 1 and a logic low will be a T, while in group 2, a logic high will be a T and a logic low will be a 1. This prevents the system from ever seeing a logic 0. The run-mode screen can be used to limit the functional test to a portion of the truth table that is different from that used by the parametric test of group 2. The actual mechanics of this technique will be described in detail below.

To aid in understanding the ECL parametric testing technique, a simplified model of an ECL circuit can be used. The model is a voltage divider as shown in Figure 4-24. This model is only valid at a specific point on the output voltage level versus dc loading curve and does not constitute a truly functional model, but it is sufficient to demonstrate the parametric testing technique.

Using this model, a table can be constructed listing the values of the ECL Ro (static) for specific values of Vout and Iout with a 50-ohm load resistor.

Vout	Iout at 50 ohms RL	Ro (static)*
0.81 V	23.8 mA	34.03 ohms
-0.96 V	20.8 mA	46.15 ohms
-1.65 V	7.0 mA	235.72 ohms
-1.85 V	3.0 mA	616.67 ohms

*Reference Motorola MECL Data Book at 25 degrees C.

*These values of Ro are used only to aid in the discussion of the parametric test technique and should not be used to compute actual test limits or levels.

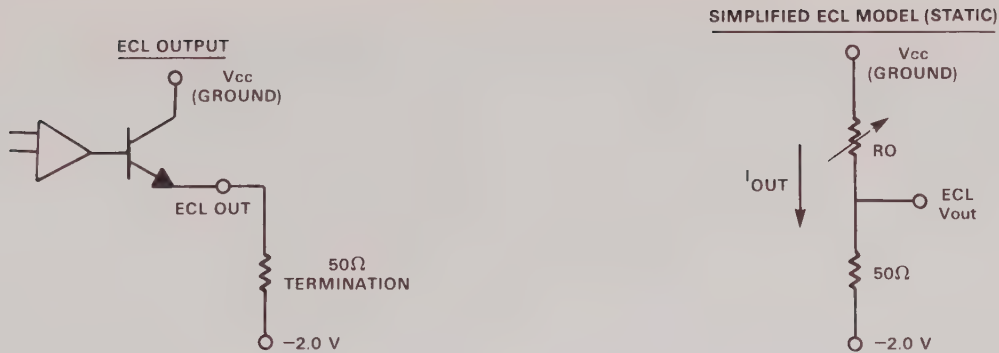


Figure 4-24. Simplified model of an ECL device.

Testing for Minimum Limit.

During a parametric test, a logic 1 in the truth table will direct the parametric measurement unit to sink current (IOH parametric) out of an ECL output and to measure the voltage (VOH). The parametric measurement unit is used to simulate the 50-ohm loading of the output during parametric testing for VOH. The 20.8-mA IOH current simulates a VOH(min) of -0.96 V driving 50 ohms. If Vout was -0.96 V into a 50-ohm load, Ro (static) would be 43.15 ohms; the parametric measurement unit will measure -0.96 V when sinking 20.8 mA across 43.15 ohms. If the actual DUT output was at VOL(max) of -1.65 V, assuming RL of 50 ohms, and the truth table showed it to be a logic 1, the parametric measurement unit would force 20.8 mA out of the DUT. Using the simplified ECL output, Ro would be equal to 235.72 ohm at a VOL of -1.65 V. This 20.8 mA forced across 235.72 ohms would be measured as -4.9 V and the device would fail the VOH parametric test.

This test has not checked the device for the maximum value of VOH. If VOH was -0.81 V into a 50-ohm load, Ro (static) would be 34.03 ohms. When the parametric measurement unit sank 20.8 mA into 34.03 ohms, it would measure Vout as -0.708 V. This would pass, since it is more positive than -0.96 V, but it would not verify that the device can sink 23.8 mA into a 50-ohm load at a Vout of -0.81 V.

Testing for Maximum Limit.

During a parametric test, a logic T in the truth table will direct the parametric measurement unit to force a voltage (VZH) on the ECL output and to measure the current (IZH). During the group 2 test, the system will force a VZH of -0.81 V on the output pin under test when the output is defined as a T. The DUT pin will actually be in a logic 1 state, given the pattern of inputs in the truth table, but it is defined as a logic T in order to allow VZH testing.

NOTE

Functional testing is not done in group 2; therefore, this misdefinition of output states will not cause a functional failure.

The system will then look for a current of 23.8 mA or less in order to verify VOH(max) of the DUT. With an output voltage of -0.81 V forced into a 50-ohm load, Ro is calculated to be 34.03 ohms. The parametric measurement unit will force -0.81 volt through the output (Ro) and

measure 23.8 mA. If, for example, the output was -0.7 V into a 50-ohm termination, Ro would be 26.92 ohms. The parametric measurement unit would force -0.81 V, measure 30.1 mA, and fail the DUT since 30.1 mA is greater than 23.8 mA. If Vout was -1.65 V into a 50-ohm load, Ro would be 235.72 ohms. The parametric measurement unit would force -0.81 V, measure 3.43 mA, and pass the DUT, but this Vout of the DUT would have been previously detected by the group 1 parametric test.

Bracketing the Limits.

In group 1, the minimum limit for VOH was tested; any device which had a VOH more positive than -0.96 V passed, and the test continued to group 2. In group 2, the device was tested for a VOH that was less positive than -0.81 V. If the DUT had a Vout of -0.65 V, it would pass the test in group 1 and be faulted when tested in group 2. Similarly, if the DUT had a Vout of -2.00 V, while it would pass the group 2 test, it would have failed the group 1 test and been previously rejected as faulty. In this fashion, the minimum and maximum limits for VOH and VOL can be tested and devices falling outside the acceptable ranges will be rejected.

4.10.5 Program example, 10101 Figures 4-25 and 4-26

Excerpts from the manufacturer's data sheets for the 10101 quad 2-input OR/NOR gate are shown in Figure 4-25. These excerpts show several characteristics that will affect the test structure.

1. Vee is -5.2 volts. This means that PS3 must be used.
2. Pin 12 is a common input to all 4 gates. It has different values of I_{IH} and I_{IL}, and must be tested separately from the other inputs.
3. Since this is an ECL device, two groups are required to test the outputs parametrically.

Worksheet Organization.

The tests will be structured along the lines described below and illustrated in Figure 4-26.

Describe Screen. All input pins are assigned to pin set 1. All outputs are coded T and are assigned to pin set 2.

Run-mode Screen. Functional testing is enabled from step 2 through the end of the truth table. The functional test will only be performed in group 1.

Parameters Group 1 Screen. The power supply is set for -5.2 volts from PS3. Test limit (I₃) is set at 26 mA from lee in the data sheet. I-max is derived from the formula. The power-supply test is specified for step 13. Only the func-

tional test and the parametric test for VOH(min) and IZL will be performed. The IZL test will test for IOL(max).

Alternate Parameters Group 1 Screen. The parametric start and stop steps for group 1 are 2 and End.

Parameters Group 2 Screen. Only the parametric test for VOH(max) and IZH will be performed. The IZH test will test for IOL(min).

Alternate Parameters Group 2 Screen. The parametric start and stop steps for group 2 are specified as 0 and 1. Note that these steps cannot be tested in the functional test.

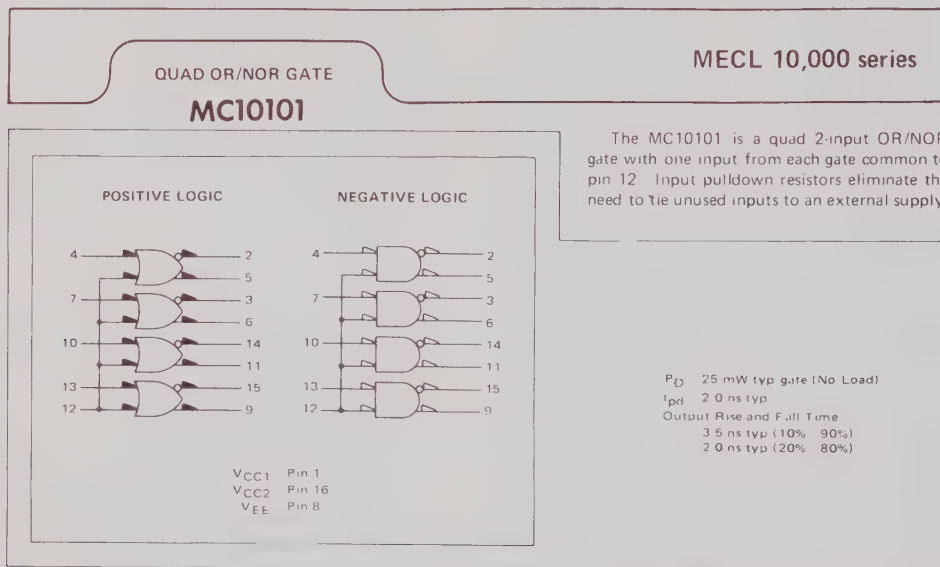
Parameters Group 3 Screen. This group is set up to test pin 12 parametrically.

Alternate Parameters Group 3 Screen. The parametric start and stop steps for group 3 are specified as 2 and 3.

Parameters Group 4 Screen. This group is set up to test all input pins, except pin 12, parametrically.

Alternate Parameters Group 4 Screen. The parametric start and stop steps for group 4 are specified as 4 and 5.

Truth Table Screen. The truth table for this device has been broken down into sections. The first section, steps 0 and 1, tests the output only for VOH(max) and VOL(min). In conjunction with the remainder of the truth table steps used by group 1, these steps will bracket the maximum and minimum values of the output parameters. The input parametric tests are also broken down into two mutually exclusive parts, with group 3 testing the common input, pin 12, in steps 2 and 3, and group testing all other inputs in steps 4 and 5. The power supply test step is set up with all outputs unloaded "don't care".



MC10101P Test Limits											TEST VOLTAGE VALUES					(V _{CC}) Gnd	
											(Volts)						
											V _{IH} max	V _{IL} min	V _{IHA} min	V _{ILA} max	V _{EE}		
											TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
Characteristic	Symbol	P _{in} Under Test	-30°C		+25°C		+85°C		Unit	V _{IH} max	V _{IL} min	V _{IHA} min	V _{ILA} max	V _{EE}			
Power Supply Drain Current	I _E	8			20	26			mAdc					8	1 16		
Input Current	I _{INH}	4				265			μAdc	4				8	1 16		
	I _{INT}	12				535			μAdc	12				8	1 16		
						0.5			μAdc		4	12			8	1 16	
Logic 1 Output Voltage	V _{OH}	5	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	12				8	1 16		
		5	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		4				8	1 16		
		2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700						8	1 16		
Logic 0 Output Voltage	V _{OL}	5	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc					8	1 16		
		5	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615						8	1 16		
		2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		12	4						
Logic 1 Threshold Voltage	V _{OHA}	5	-1.080		-0.980	-0.910		-0.910	Vdc			12		8	1 16		
		5	-1.080		-0.980	-0.910		-0.910				12		8	1 16		
		2	-1.080		-0.980	-0.910		-0.910					12		8	1 16	
Logic 0 Threshold Voltage	V _{OLA}	5		-1.655		-1.630		-1.595	Vdc				12	8	1 16		
		5		-1.655		-1.630		-1.595					12	8	1 16		
		2		-1.655		-1.630		-1.595						12	8	1 16	
Switching Times (50-ohm load)																	
Propagation Delay	t _{pd}	2			1.0	2.0	2.9		ns								
	t _{pd}	2															
	t _{pd}	5															
	t _{pd}	5															
Rise Time (20 to 80%)	t _r	2			1.1		3.3										
	t _r	5															
	t _r	2															
	t _r	5															
Fall Time (20 to 80%)	t _f	2															
	t _f	5															
	t _f	2															
	t _f	5															

Figure 4-25. Excerpt from Semiconductor Data Library, vol. 4, Motorola 1974, pages 3-5 and 3-7.

1732 DESCRIBE SCREEN WORKSHEET

A. Program Name: 10101

Type of Device (if different from program name) or other comment: _____

B. Number of pins per device: 16
Number of Test Groups per Test Program: 4

C. Clocks
CU: 4.00 MHz (One of these fifteen choices)

8.00	2.29	1.33
5.33	2.00	1.23
4.00	1.78	1.14
3.20	1.60	1.07
2.66	1.45	1.00

Sync: C1 = C0/1 C8 = C0/8
 C2 = C0/2 CF = C0/16
X C4 = C0/4 External

D. Pin Assignments

ID	S	ID	S	ID	S
1.	<u>G</u>	17.	<u> </u>	33.	<u> </u>
2.	<u>T2</u>	18.	<u> </u>	34.	<u> </u>
3.	<u>T2</u>	19.	<u> </u>	35.	<u> </u>
4.	<u>I1</u>	20.	<u> </u>	36.	<u> </u>
5.	<u>T2</u>	21.	<u> </u>	37.	<u> </u>
6.	<u>T2</u>	22.	<u> </u>	38.	<u> </u>
7.	<u>I1</u>	23.	<u> </u>	39.	<u> </u>
8.	<u>V3</u>	24.	<u> </u>	40.	<u> </u>
9.	<u>T2</u>	25.	<u> </u>	41.	<u> </u>
10.	<u>I1</u>	26.	<u> </u>	42.	<u> </u>
11.	<u>T2</u>	27.	<u> </u>	43.	<u> </u>
12.	<u>I1</u>	28.	<u> </u>	44.	<u> </u>
13.	<u>I1</u>	29.	<u> </u>	45.	<u> </u>
14.	<u>T2</u>	30.	<u> </u>	46.	<u> </u>
15.	<u>T2</u>	31.	<u> </u>	47.	<u> </u>
16.	<u>G</u>	32.	<u> </u>	48.	<u> </u>

Definitions (for ID)
I (1,2) = Input
O (1,2) = Output
B = Bidirectional
T = Tristate
X = Don't Care
V (1,2,3) = Power
G = Ground
C (1,2,3) = Clock
S = Pin Set
(Default is 1)

Figure 4-26a. Describe screen worksheet for MC10101 program.

1732 RUN-MODE SCREEN WORKSHEET

A. Test Sequence: CFP (for example: CFP, CPF, F, or CP)

B.

	Bin 1	Bin 2	Bin 3	Bin 4	Bin 5
	F	P	F	P	F
G 1	<u>*</u>	<u>*</u>	<u> </u>	<u> </u>	<u> </u>
R 2	<u>*</u>	<u>*</u>	<u> </u>	<u> </u>	<u> </u>
O 3	<u>*</u>	<u>*</u>	<u> </u>	<u> </u>	<u> </u>
U 4	<u>*</u>	<u>*</u>	<u> </u>	<u> </u>	<u> </u>
P 5	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
S 6	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>

Test Procedure

C. Functional Test: Step 2 to step END

D. All Groups First Failure
X All Groups (use if binning is needed)
 Stop After Each Group
 Test Continuously to Failure
 Test Continuously

E. Single Step

F. Keyboard IS (NOT) Locked. (Password = up to 6 characters)

Figure 4-26b. Run-mode screen worksheet for MC10101 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 4 groups Program Name 10101

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step 13

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage Test Limit
V1 = + _____ V I1 = _____ mA
V2 = + _____ V I2 = _____ mA
V3 = -5.20 V I3 = 26.0 mA 32.5 mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>-1.53</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>-1.05</u> V
VOL = <u>-1.65</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA (uA)
VOH = <u>-960m</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA (uA)
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>-2.50</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>0.0</u> V
VOL = <u>-2.50</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA (uA)
VOH = <u>-960m</u> V	@ IOH = <u>20.8</u> mA/uA	<u>8.0</u> mA (uA)
IZL = <u>7.0</u> mA/uA	@ VZL = <u>-1.65</u> V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

Figure 4-26c. Parameters screen worksheet, group 1, for MC10101 program.

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 4 groups Program Name 10101

(A) Range of steps within which to do all parametric tests: step 2 to step END

(B) Close relays during:

Parametric Test Limits	Test Limit	Parametric	Functional
V1 = + XXXX* V	I1 = XXXX mA	K1	K1
V2 = + XXXX V	I2 = XXXX mA	K2	K2
V3 = - XXXX V	I3 = XXXX mA	K3	K3
		K4	K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	@ VOS = XXXX V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	@ VOS = XXXX V	

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-26d. Alternate parameters screen worksheet, group 1, for MC10101 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 4 groups Program Name 10101

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = + _____ V	I2 = _____ mA	_____ mA
V3 = <u>-5.20</u> V	I3 = _____ mA	<u>32.5</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>-1.53</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>-1.05</u> V
VOL = <u>-1.65</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>-960m</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

Figure 4-26e. Parameters screen worksheet, group 2, for MC10101 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>-2.50</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>0.0</u> V
VOL = <u>-2.50</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>-1.85</u> V	@ IOH = <u>3.0</u> mA/uA	<u>3.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = <u>23.8</u> mA/uA	@ VZH = <u>-810m</u> V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 4 groups Program Name 10101

(A) Range of steps within which to do all parametric tests: step 0 to step 1 (B) Close relays during: Parametric Functional

Voltage	Test Limit		
V1 = + XXXX* V	I1 = XXXX mA	_____ K1	_____ K1
V2 = + XXXX V	I2 = XXXX mA	_____ K2	_____ K2
V3 = - XXXX V	I3 = XXXX mA	_____ K3	_____ K3
		_____ K4	_____ K4

Figure 4-26f. Alternate parameters screen worksheet, group 2, for MC10101 program.

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

* XXXX represents a value determined by an entry on the parameters screen.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 4 groups Program Name 10101

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = + _____ V	I2 = _____ mA	_____ mA
V3 = <u>-5.20</u> V	I3 = _____ mA	<u>32.5</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = <u>535</u> mA/uA	@ VIL = <u>-1.53</u> V	<u>-1.53</u> V
IIH = <u>535</u> mA/uA	@ VIH = <u>-1.05</u> V	<u>-1.05</u> V
VOL = <u>-1.65</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>-960m</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

(C) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>-2.50</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>0.0</u> V
VOL = <u>-2.50</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>-960m</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

Figure 4-26g. Parameters screen worksheet, group 3, for MC10101 program.

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 4 groups Program Name 10101

(A) Range of steps within which to do all

parametric tests: step 2 to step 3

(B) Close relays during:

Voltage	Test Limit	Parametric	Functional
V1 = + XXXX* V	I1 = XXXX mA	_____ K1	_____ K1
V2 = + XXXX V	I2 = XXXX mA	_____ K2	_____ K2
V3 = - XXXX V	I3 = XXXX mA	_____ K3	_____ K3
		_____ K4	_____ K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = <u>500nA</u> mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max)	@ VOS = XXXX V

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max)	@ VOS = XXXX V

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-26h. Alternate parameters screen worksheet, group 3, for MC10101 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 4 of 4 groups Program Name 10101

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = + _____ V	I2 = _____ mA	_____ mA
V3 = <u>-5.20</u> V	I3 = _____ mA	<u>92.5</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = <u>265</u> mA/uA	@ VIL = <u>-1.53</u> V	<u>-1.53</u> V
IIH = <u>265</u> mA/uA	@ VIH = <u>-1.05</u> V	<u>-1.05</u> V
VOL = <u>-1.65</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>-960m</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

Figure 4-26i. Parameters screen worksheet, group 4, for MC10101 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>-2.50</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>0.0</u> V
VOL = <u>-2.50</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>-960m</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 4 of 4 groups Program Name 10101

(A) Range of steps within which to do all parametric tests: step 4 to step 5

(B) Close relays during:

Voltage	Test Limit	Parametric	Functional
V1 = + XXXX* V	I1 = XXXX mA	_____ K1	_____ K1
V2 = + XXXX V	I2 = XXXX mA	_____ K2	_____ K2
V3 = - XXXX V	I3 = XXXX mA	_____ K3	_____ K3
		_____ K4	_____ K4

Figure 4-26j. Alternate parameters screen worksheet, group 4, for MC10101 program.

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = <u>500nA</u> mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	@ VOS = XXXX V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	@ VOS = XXXX V	

* XXXX represents a value determined by an entry on the parameters screen.

1732 TRUTH-TABLE WORKSHEET

Sheet 1 of 1

Device number if different from program name

PROGRAM NAME 10101

		Pin no (Cross out two lines)		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
				17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
				33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Step	Function or Constant	ID	Vcc1	0	0	I	0	0	I	Vcc	0	I	0	I	I	0	0	Vcc2	
			G	T	T	I	T	T	I	V	T	I	T	I	I	T	T	G	Step
0			G	I	I	i	T	T	i	V	T	i	T	i	i	I	I	G	0
1			G	T	T	0	I	I	0	V	I	0	I	0	0	T	T	G	1
2			G	X	X	X	X	X	X	V	X	X	X	i	X	X	X	G	2
3			G	X	X	X	X	X	X	V	X	X	X	0	X	X	X	G	3
4			G	X	X	i	X	X	0	V	X	i	X	X	0	X	X	G	4
5			G	X	X	0	X	X	i	V	X	0	X	X	i	X	X	G	5
6			G	T	T	i	I	I	I	V	I	I	I	i	i	T	T	G	6
7			G	T	I	i	I	T	0	V	T	0	T	0	0	I	I	G	7
8			G	I	T	0	T	I	i	V	T	0	T	0	0	I	I	G	8
9			G	I	I	0	T	T	0	V	T	i	I	0	0	T	I	G	9
10			G	T	T	0	I	I	0	V	I	0	I	i	0	T	T	G	0
1			G	I	I	0	T	T	0	V	I	0	T	0	i	I	T	G	1
2			G	I	I	0	T	T	0	V	T	0	T	0	0	I	I	G	2
3			G	X	X	0	X	X	0	V	X	0	X	0	0	X	X	G	3
4			E																4
5																			5
6																			6
7																			7
8																			8
9																			9
0																			0

Figure 4-26k. Truth table screen worksheet for MC10101 program. This worksheet shows the characters I and o where the display screen would show 1 and 0 in reverse video.

4.11 PROGRAMMING FOR MEMORY DEVICES

4.11.1 General

While memory devices are usually considered to be LSI devices, they will be discussed before other LSI devices because they are somewhat easier to test. Memories come in all three families of devices discussed so far. In addition to the differences due to the family type, the memory devices are broken down into different types by function: RAM, ROM, PROM (both blank and programmed), and EPROM (both blank and programmed).

Some MOS devices require 3 power-supply voltages, while others require only one and can operate over a range of 5 to 15 volts. Still other MOS devices only operate at the same voltage as TTL devices, 5 V. ECL devices generally operate at -5.2 V.

Developing a program for use in testing memory devices requires a certain amount of familiarity with the system, since it can only handle 4K minus 1 steps in a test program. Up to 46 inputs or outputs can be tested with a full 48-pin system, so this limitation doesn't have much impact on memory devices with fewer than 4K minus 1 words of memory, e.g., a 16K ROM organized to provide $2K \times 8$ -bit words, but it can pose a problem testing a $4K \times 1$ -bit device. The 4K minus 1 step limitation on the length of a program means that a 4K device, whether $4K \times 1$ -bit or $4K \times 8$ -bit, can't be tested. A $4K \times 1$ RAM couldn't be tested, because separate steps are required to write and read data. A $4K \times 1$ ROM couldn't be tested because the last address location could not be addressed. Subroutines, jumps, specialized electronics on the socket adaptor, or some other method must be employed if a device with more than 4K minus one words of memory is to be tested.

The different types of devices use different solutions; ROM, PROM, and EPROM devices require a software solution, since their contents are fixed and generally each location contains different data. A typical solution, which could also be applicable to RAM devices, might be to break the test program down into several smaller programs, each to be called from the tape cartridge. Each of these smaller programs tests fewer than 4K address locations of the DUT and overlaps the preceding and following tests. In this way, parametric and functional operation of the entire device can be tested, although at the expense of increased testing and programming time.

Using a software approach to testing RAM is usually not the best way to test RAM devices. RAM devices can use a hardware approach, in that the socket adaptor can incorporate a counter to generate address counts. The Dynamic RAM Adaptor contains such a counter, along with a multiplexer to route the address information to the proper pins; this socket adaptor allows the system to test dynamic RAMs with up to 64K address locations. Program looping is used to toggle the counter through the required number of locations, rather than step through several thousand steps of a truth table. The 1732-9617 Dynamic RAM Adaptor is designed to be used with systems numbered 1732-9720 through 9724. The 1732-9616 Static RAM Adaptor is to be used with systems numbered 1732-9720 through 9724.

The use of the special Dynamic RAM Adaptor socket adaptor is recommended because, without a special socket adaptor containing an address counter and multiplexer, it would take several steps in the truth table to check each address location of the DUT. The system would have to use one step to set the address, another to send the RAS signal, and a third step for the CAS signal in order to complete a single write operation. To perform a read operation on the same location, it would again require a step to set up the address inputs, another step for the RAS signal, and a third step for the CAS signal to complete the read operation. Static RAMs would take fewer steps, but they still require separate steps for addressing and read/write operations for each memory location. The number of steps that a large RAM would require using this technique would be likely to exceed the number available in a single test program.

It is quite time-consuming to write a full 4K step program which will check only a portion of a device. The Dynamic RAM Adaptor socket adaptor contains an internal counter which generates the address sequence. RAS and CAS signals are generated automatically in one step of the truth table; thus, only a single step of the truth table is required to test a single memory location. An address march routine using 4 truth-table steps looped 4K times with a Jump command will go through all 16K address locations of a 16K RAM. This is obviously a much simpler program to construct than one which goes through each memory location using six or more truth-table steps to write, read, and write data into each memory location. RAM test programs which are available from GenRad in the Program Library use this socket adaptor to simplify and speed up the tests.

4.11.2 RAM

RAM devices can be divided into two subclasses, static RAM and dynamic RAM. Dynamic RAMs require refresh pulses in order to maintain the stored data. This tends to make the socket adaptor and truth table of a dynamic RAM slightly more complicated than those of a static RAM of comparable capacity. If the DUT has multiplexed address lines, the socket adaptor and truth table will again be more complex; generally, the best solution is to include a counter and/or a multiplexer in the socket adaptor as in the Dynamic RAM Adaptor in order to operate the device. The use of this adaptor, or one similar to it, allows simpler and more compact test programs for dynamic RAMs.

Testing of RAM devices can be divided into two portions. During the first portion of the program, the dc parameters of the RAM are tested; for dynamic RAMs, this means any electronics in the socket adaptor must be isolated from the DUT. After applying power to the device and waiting the number of read/write cycles specified by the manufacturer's data sheets, all pins are exercised to test their high and low states parametrically. The second portion of the program tests the RAM functionally. Dynamic RAMs must have the address lines connected to the refresh circuits. Using a socket adaptor such as the Dynamic RAM Adaptor, the quickest way to test the device is to perform a march test as follows:

- Starting at address 0, march through the device writing 0 into each location until the counter has gone through all the address locations.

- March through again, reading the 0's and writing 1's into each location.
- March through reading the 1's and writing 0's into each location.

NMOS dynamic RAMs usually require 3 different power-supply voltages, Vdd, Vcc, and Vbb. A few newer N-channel Scaled-MOS (SMOS) devices require only a single power-supply voltage.

CMOS static RAMs require a single supply voltage. For some devices, this voltage can range from 5 V to 15 V, while several others can operate only with a supply voltage of 5 V. Since they do not have any refresh requirements, the truth table is somewhat simpler than that for a dynamic RAM. SMOS static RAMs share many of the same requirements and characteristics of CMOS static RAMs, and the same handling and test procedures should be followed for both types of devices. Neither CMOS nor SMOS require clock pulses; instead, they use the chip select or address signals to strobe data in or out.

TTL bipolar RAMs are usually static devices. They are similar to CMOS static RAMs in that they require only a single supply voltage, with a range of 4.75 V to 5.25 V, and they also use the chip select or address signals instead of clock pulses.

ECL static RAMs are also bipolar and operate with a single power supply voltage at a range of -4.94 V to 5.46 V. Like dynamic RAMs, ECL static RAMs require clocking.

4.11.3 Program Example, 4116 Figures 4-27 through 4-29 General.

The 4116 is a 16K $\times$ 1 dynamic RAM. As shown in the pin diagram from the manufacturer's data sheets, (see Figure 4-27), it has multiplexed address lines and requires two different clocks, one to clock the RAS L line and one to clock the CAS L line. Since the Dynamic RAM Adaptor socket adaptor is fairly complex (as described in Section 3), it is available from the factory wired and configured for the 4116. The Dynamic RAM Adaptor will be described briefly here in order to facilitate the discussion of the program.

from the system to the DUT by jumper wires inside the socket adaptor. Output data from the DUT are fed into a J-K flip-flop before being returned to the system.

While the 4116 has only 16 pins, 24 driver/sensor pins are required by the socket adaptor. The eight extra pins are required because of the counter and timing control circuitry and because of the requirement that all timing and counter electronics be isolated from the DUT when the dc parametric tests are being performed. One driver/sensor pin controls a number of CMOS switches, which open during the parametric tests to isolate the timing and counter electronics. Pin connections between the socket adaptor and the system and between the socket adaptor and the DUT are listed on the block diagram, Figure 4-28a. The function of each pin is listed in Table 4-11.

Table 4-11
DYNAMIC RAM ADAPTOR DRIVER/SENSOR PIN FUNCTIONS

Pin No.	Signal Name	Function
1	- RESET	Resets counters to zero
2	- CON ADPT	Connects adaptor electronics to the adaptor
3	+ CNT DWN	Control for "Count down" on counter
4	- CNT ENB	Enables counter
5	- CYC ENB	Cycle enable for timing generator
6	- X	Not used
7	WRITE L	Writes data into the RAM
8	Data in	Parametric line for Din on RAM
9	Latch Data	Latched data output from RAM
10	Data out	Parametric line for Dout from RAM
11	RAS L	Parametric line for RAS L on RAM
12	CAS L	Parametric line for CAS L on RAM
13	X	Not used
14	X	Not used
15	X	Not used
16	X	Not used
17	A0	Address input 0 to the RAM
18	A1	Address input 1 to the RAM
19	A2	Address input 2 to the RAM
20	A3	Address input 3 to the RAM
21	A4	Address input 4 to the RAM
22	A5	Address input 5 to the RAM
23	A6	Address input 6 to the RAM
24	A7	Address input 7 to the RAM (used for 64K RAM only; not used for 16K)

Test Philosophy.

This program example is structured to perform dc parametric and functional tests on the 4116. Continuity tests are not possible on the 4116 due to the electronics incorporated in the Dynamic RAM Adaptor. Six parameters group screens are required. The first two test the parameters of the output at minimum and maximum supply voltages. The second two groups test the parameters of the inputs at minimum and maximum supply voltages, and the last two groups test the output for high-impedance conditions at both minimum and maximum supply voltages. Incorporated in these six parameters groups are power-supply checks on the device at operating, standby, and refresh conditions. It should be noted that supply PS2 is also used to power the CMOS switches within the socket adaptor, and thus the test limit must be increased by the amount of current that the socket adaptor draws.

The parametric and functional testing performed on the 4116 is detailed in the program layout chart. At the start of

this testing, the device is disconnected from the adaptor electronics and cycled through some initial refreshing to achieve proper device operation. While the device is still disconnected from the adaptor electronics (by CMOS switches), all parametric testing and some operational functional tests are performed. The operation of the RAS L, CAS L, WRITE L, and Din inputs and the Dout output are tested at a single address location by wiring and reading first a 0 and then a 1. After the DUT is connected to the adaptor electronics, the same exercise is essentially repeated; at each address location both a 0 and 1 are written in and read out to the J-K flip-flop. These latched data are clocked out of the socket adaptor on the next step of the truth table. All further testing on the device uses a march technique where 0's or 1's are written into each address location and verified. This technique makes use of the Dynamic RAM Adaptor's internal counter, which is connected to the input address lines on the DUT. Once the counter is enabled, 0's are written into the first 16 addressed locations. The truth table is structured to loop on these 16 steps 1023 times and thus write a 0 in all 16K locations. A delay is then placed in the program to insure that the data are retained for 2 ms before being refreshed and read out. Another 16K march reads the 0 in each location while writing 1's behind. Another delay of 2 ms is placed in the program to insure that data are again retained before a final march reads the 1's in each address location while writing 0's behind.

NOTE

The jump loop count of 1023 used for the 4116 RAM can be modified easily, allowing this program to be used with other dynamic RAM address configurations. For example, an 8K march is possible by simply changing the 1023 to 511.

Worksheet Organization.

Describe Screen. The pins of the DUT will not correspond directly to the pin numbers and IDs on the describe screen, since there is special circuitry on the Dynamic RAM Adaptor. In order to fill out the describe screen, the pins are identified according to their function on the socket adaptor. Pin set selection will be governed by the fact that pins connected only to the adaptor electronics are assigned to pin set 2. All pins that connect to the DUT, except for the RAS L, CAS L, and WRITE L pins, are assigned to pin set 1. Those pins are placed in pin set 2 because they have a higher minimum VIH than the inputs assigned to pin set 1.

4 MHz is selected as the clock frequency, and C4 is entered as the sync value, for a resulting 1-MHz clock for functional testing.

Parameters Group 1 Screen. The device is tested under operating conditions with Vbb, Vcc, and Vdd at minimum voltage. The functional and parametric tests are performed at minimum voltage in this group. Notice that VIL(func) is

the same in both pin sets but that VIH(func) is higher in pin set 2; this is because of the higher voltage required by the RAS L, CAS L, and WRITE L inputs. IOL and IOH are set at 0.0 μ A because the socket adaptor acts as the load. This group tests the output parametrically; note that no parametric tests will be performed in pin set 2.

Alternate Parameters Group 1 Screen. The parametric test is started at step 19 and stopped at step 25. These values are entered after the truth table is completed.

Parameters Group 2 Screen. The device is tested under operating conditions with Vbb, Vcc, and Vdd at maximum voltage. The functional and parametric tests at maximum voltage will be performed here.

Alternate Parameters Group 2 Screen. The parametric test is started at step 19 and stopped at step 25.

Parameters Group 3 Screen. The device is tested under standby conditions with Vbb, Vcc, and Vdd at minimum voltage in this group. Parametric testing of the inputs at minimum voltage is performed in this group.

Alternate Parameters Group 3 Screen. The parametric test runs from step 3 through step 13.

Parameters Group 4 Screen. The device is tested under standby conditions with Vbb, Vcc, and Vdd at maximum voltage. This group also tests the inputs parametrically at maximum voltage.

Alternate Parameters Group 4 Screen. The parametric test runs from step 3 through step 13.

Parameters Group 5 Screen. The device is tested under refresh conditions with Vbb, Vcc, and Vdd at minimum voltage. The output is checked for leakage current at minimum voltage while in the high-impedance state.

Alternate Parameters Group 5 Screen. The parametric test in this group is performed at step 27.

Parameters Group 6 Screen. The device is tested under refresh conditions with Vbb, Vcc, and Vdd at maximum voltage in this group. The output is checked for leakage current at maximum voltage while in the high-impedance state.

Alternate Parameters Group 6 Screen. This group also performs the parametric test on step 27.

Truth Table Screen. Refer to the program layout chart for an overview of the truth-table's construction. Note that, after power-up, the 4116 requires 8 memory cycles in order to achieve proper operation before parametric and functional testing is begun. Refresh is done by strobing row addresses with RAS low on the 4116. Steps 1 and 2 toggle the RAS L line, so, by using a Jump command, the required number of memory cycles will be performed.

Run-mode Screen. The functional and parametric tests are selected. As mentioned above, the continuity test cannot be run because of the circuitry contained in the special socket adaptor. Functional testing is enabled in groups 1 and 2; parametric testing is performed in all six groups. The functional test is written to begin at step 0 and run through the truth table to the E command line, so the default values (0 and End) are selected.



MCM4116

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116 is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116 requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116 is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- $\pm 10\%$ Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 462 mW Active, 20 mW Standby (Max)
- Fast Access Time Options: 150 ns — MCM4116L-15, C-15
200 ns — MCM4116L-20, C-20
250 ns — MCM4116L-25, C-25
300 ns — MCM4116L-30, C-30
- Easy Upgrade from 16-Pin 4K RAMs
- Pin Compatible with 2117, 2116, 6616, μ PD416, and 4116

ABSOLUTE MAXIMUM RATINGS (See Note 1)

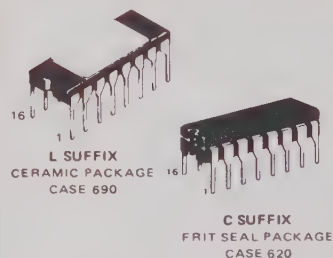
Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V _{BB}	V _{in} , V _{out}	-0.5 to +20	Vdc
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Power Dissipation	P _D	1.0	W
Data Out Current	I _{out}	50	mA

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

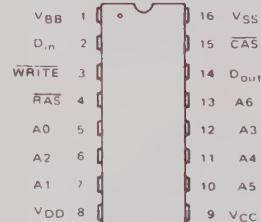
MOS

(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY



PIN ASSIGNMENT



PIN NAMES

A ₀ –A ₆	Address Inputs
CAS	Column Address Strobe
D _{in}	Data In
D _{out}	Data Out
RAS	Row Address Strobe
WRITE	Read/Write Input
V _{BB}	Power (-5 V)
V _{CC}	Power (+5 V)
V _{DD}	Power (+12 V)
V _{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 4-27a. Excerpt from Motorola Microcomputer Data Library, Motorola, 1978, page 5-31.

DC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V _{DD}	10.8	12.0	13.2	Vdc	1
	V _{CC}	4.5	5.0	5.5	Vdc	1, 2
	V _{SS}	0	0	0	Vdc	1
	V _{BB}	-4.5	-5.0	-5.5	Vdc	1
Logic 1 Voltage, RAS, CAS, WRITE	V _{IHC}	2.7	—	7.0	Vdc	1
Logic 1 Voltage, all inputs except RAS, CAS, WRITE	V _{IH}	2.4	—	7.0	Vdc	1
Logic 0 Voltage, all inputs	V _{IL}	-1.0	—	0.8	Vdc	1

DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Max	Units	Notes
Average V _{DD} Power Supply Current	I _{DD1}	—	35	mA	4
V _{CC} Power Supply Current	I _{CC}	—	—	mA	5
Average V _{BB} Power Supply Current	I _{BB1,3}	—	200	μA	
Standby V _{BB} Power Supply Current	I _{BB2}	—	100	μA	
Standby V _{DD} Power Supply Current	I _{DD2}	—	1.5	mA	6
Average V _{DD} Power Supply Current during "RAS only" cycles	I _{DD3}	—	27	mA	4
Input Leakage Current (any input)	I _{I(L)}	—	10	μA	
Output Leakage Current	I _{O(L)}	—	10	μA	6, 7
Output Logic 1 Voltage @ I _{out} = -5 mA	V _{OH}	2.4	—	Vdc	2
Output Logic 0 Voltage @ I _{out} = 4.2 mA	V _{OL}	—	0.4	Vdc	

NOTES:

- 1 All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
- 2 Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH(min)} specification is not guaranteed in this mode.
- 3 Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
- 4 Current is proportional to cycle rate, maximum current is measured at the fastest cycle rate.
- 5 I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
- 6 Output is disabled (open circuit) and RAS and CAS are both at a logic 1.
- 7 0 V ≤ V_{out} ≤ +5.5 V
- 8 Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$

BLOCK DIAGRAM

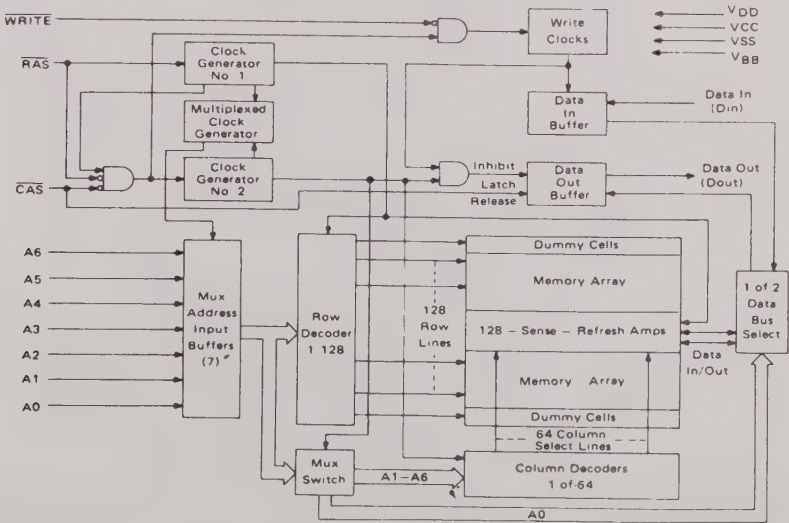


Figure 4-27b. Excerpt from Motorola Microcomputer Data Library, Motorola, 1978, page 5-32.

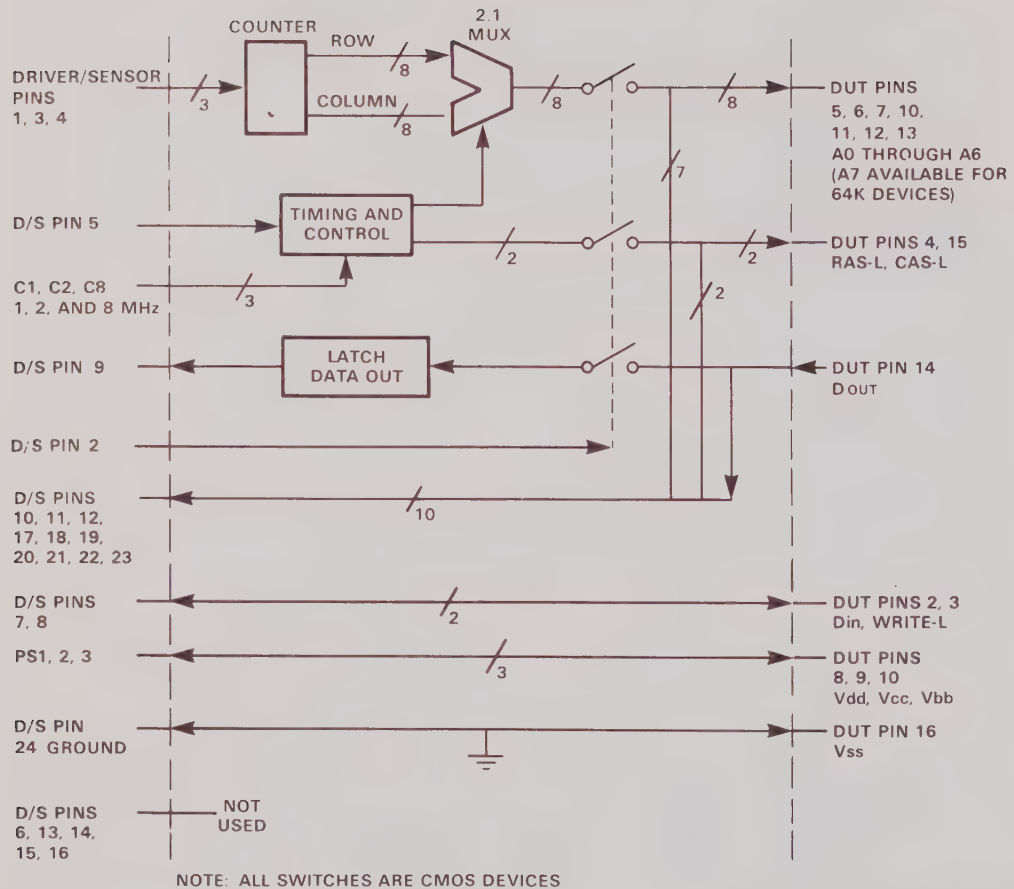


Figure 4-28a. Dynamic RAM adaptor simplified block diagram.

Step Number	Activity Start
0-2	Power up. Refresh, RAS input cycled.
3-13	Parametric tests on all 4116 inputs, walk ones through. Power supply operating current checked in step 3 with RAS, CAS both low.
14-16	Cycle RAS, CAS, write to 0 to DATA IN. Power-supply refresh current checked in Step 14 with RAS LOW, CAS HIGH.
17-18	Cycle RAS, CAS to try write 1 to DATA IN with WRITE disabled.
19	Check DATA OUT for 0. Parametric test of DATA OUT in low state.
20-22	Cycle RAS, CAS to try write 1 to DATA IN.
22-24	Cycle RAS, CAS to try write 0 to DATA IN with WRITE disabled.
25	Check DATA OUT for 1. Parametric test of DATA OUT in high state.
26-27	Cycle RAS to check DATA OUT as high-impedance state with CAS high. Parametric test of DATA OUT in high-impedance condition.
28-29	Connect Dynamic RAM Adaptor adaptor electronics and cycle for refresh.
30-31	Cycle and write A0 on DATA IN to one address location.
32-33	Cycle and read the 0 to LATCHED DATA out. Write a 1 on DATA IN to same address location.
34-35	Cycle and read the 1 on LATCHED DATA out.
36	Reset adaptor counter.
37-53	Enable adaptor counter to count up through 16 address locations while writing 0s into the DATA IN. Loop on these 16 steps 1023 times to count up and write 0s into all 16K address locations.
54-55	Wait 2 ms since all of the 128 rows were last refreshed to verify refresh period.
56	Reset adaptor counter.
57-88	Cycle and read the 0 on the LATCHED DATA out. Write a 1 on DATA IN. This two step process is repeated 16 times. Loop on these 32 steps 1023 times to count up, reading 0s and writing 1s into all 16K address locations.
89-90	Wait 2 ms since all of the 128 rows were last refreshed to verify refresh period.
91	Adaptor counter set to count down.
92-123	Cycle and read the 1 on the LATCHED DATA out. Write a 1 on DATA IN. This process repeated 16 times. Loop on these 32 steps 1023 times count up, reading 1s and writing 0s into all 16K address locations.
END	

Figure 4-28b. Program layout chart for MK4116 program example.

1732 DESCRIBE SCREEN WORKSHEET

A. Program Name: MK 4116

Type of Device (if different from program name) or other comment:
USE DYNAMIC RAM ADAPTOR

B. Number of pins per device: 24
Number of Test Groups per Test Program: 16

C. Clocks
CU: 4 MHz (One of these fifteen choices) | 8.00 2.29 1.33
| 5.33 2.00 1.23
| 4.00 1.78 1.14
Sync: — C1 = CU/1 — C8 = C0/8 | 3.20 1.60 1.07
— C2 = CU/2 — C4 = C0/16 | 2.66 1.45 1.00
X C4 = CU/4 — External

D. Pin Assignments

	ID	S	ID	S	ID	S
1.	<u>I2</u>		17.	<u>I1</u>	33.	
2.	<u>I2</u>		18.	<u>I1</u>	34.	
3.	<u>I2</u>		19.	<u>I1</u>	35.	
4.	<u>I2</u>		20.	<u>I1</u>	36.	
5.	<u>I2</u>		21.	<u>I1</u>	37.	
6.	<u>X</u>		22.	<u>I1</u>	38.	
7.	<u>I2</u>		23.	<u>I1</u>	39.	
8.	<u>I1</u>		24.	<u>G</u>	40.	
9.	<u>O2</u>		25.		41.	
10.	<u>I1</u>		26.		42.	
11.	<u>I2</u>		27.		43.	
12.	<u>I2</u>		28.		44.	
13.	<u>V1</u>		29.		45.	
14.	<u>V2</u>		30.		46.	
15.	<u>K3</u>		31.		47.	
16.	<u>X</u>		32.		48.	

Definitions (for ID)

I (1,2) = Input
O (1,2) = Output
B = Bidirectional
T = Tristate
X = Don't Care
V (1,2,3) = Power
G = Ground
C (1,2,3) = Clock
S = Pin Set
(Default is 1)

Figure 4-29a. Describe screen worksheet for 4116 program.

1732 RUN-MODE SCREEN WORKSHEET

A. Test Sequence: FP (for example: CFP, CPF, F, or CP)

B.

	Bin 1	Bin 2	Bin 3	Bin 4	Bin 5
	F	P	F	P	F
G 1	<u>X</u>	<u>X</u>			
R 2	<u>X</u>	<u>X</u>			
O 3	<u>X</u>				
U 4	<u>X</u>				
P 5	<u>X</u>				
S 6	<u>X</u>				

Test Procedure

C. Functional Test: Step O to step E

D. X All Groups First Failure
— All Groups (use if binning is needed)
— Stop After Each Group
— Test Continuously to Failure
— Test Continuously

E. — Single Step

F. Keyboard IS NOT Locked. (Password = up to 6 characters)

Figure 4-29b. Run-mode screen worksheet for 4116 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 6 groups Program Name MX 4116

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step 3

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+4.50</u> V	I1 = <u>4.00</u> mA	<u>5.00</u> mA
V2 = <u>+10.8</u> V	I2 = <u>35.7</u> mA	<u>50.0</u> mA
V3 = <u>-4.50</u> V	I3 = <u>200.4</u> mA	<u>2.00</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.20</u> V
VOL = <u>0.40</u> V	@ IOL = <u>4.20</u> mA/uA	<u>4.20</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = <u>5.00</u> mA/uA	<u>5.00</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	mA/uA(max) @ VOS = _____ V	

Figure 4-29c. Parameters screen worksheet, group 1, for 4116 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.40</u> V
VOL = <u>0.40</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	mA/uA(max) @ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 6 groups Program Name MX 4116

(A) Range of steps within which to do all
parametric tests: step 19 to step 25

(B) Close relays during:

Voltage	Test Limit	Parametric	Functional
V1 = + XXXX* V	I1 = XXXX mA	_____ K1	_____ K1
V2 = + XXXX V	I2 = XXXX mA	_____ K2	_____ K2
V3 = - XXXX V	I3 = XXXX mA	_____ K3	_____ K3
		_____ K4	_____ K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-29d. Alternate parameters screen worksheet, group 1, for 4116 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 6 groups Program Name MK4116

Power Supplies 1 2 3

(A) Power Supplies tested at step 3

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+5.50</u> V	I1 = <u>4.00</u> mA	<u>5.00</u> mA
V2 = <u>+13.2</u> V	I2 = <u>35.8</u> mA	<u>50.0</u> mA
V3 = <u>-5.70</u> V	I3 = <u>200.0</u> mA	<u>2.00</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.20</u> V
VOL = <u>0.90</u> V	@ IOL = <u>4.20</u> mA/uA	<u>4.20</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = <u>5.00</u> mA/uA	<u>5.00</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

Figure 4-29e. Parameters screen worksheet, group 2, for 4116 program.

(C) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.40</u> V
VOL = <u>0.90</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 6 groups Program Name MK4116

(A) Range of steps within which to do all parametric tests: step <u>12</u> to step <u>23</u>	(B) Close relays during: Parametric Functional
Voltage	Test Limit
V1 = +XXXX* V	I1 = XXXX mA
V2 = +XXXX V	I2 = XXXX mA
V3 = XXXX V	I3 = XXXX mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-29f. Alternate parameters screen worksheet, group 2, for 4116 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 6 groups Program Name MK 4116

Power Supplies ①②③

(A) Power Supplies tested at step 14
 (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = <u>+4.50</u> V	I1 = <u>10.0</u> mA	<u>5.00</u> mA
V2 = <u>+10.8</u> V	I2 = <u>25.7</u> mA	<u>30.0</u> mA
V3 = <u>-5.00</u> V	I3 = <u>200</u> mA	<u>2.00</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = <u>10.0</u> mA (uA)	@ VIL = <u>0.00</u> V	<u>0.00</u> V
IIH = <u>10.0</u> mA (uA)	@ VIH = <u>7.00</u> V	<u>2.20</u> V
VOL = <u>0.40</u> V	@ IOL = _____ mA/uA	<u>4.20</u> mA (uA)
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>5.00</u> mA (uA)
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

Figure 4-29g. Parameters screen worksheet, group 3, for 4116 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = <u>10.0</u> mA (uA)	@ VIL = <u>0.00</u> V	<u>0.00</u> V
IIH = <u>10.0</u> mA (uA)	@ VIH = <u>7.00</u> V	<u>2.40</u> V
VOL = <u>0.40</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA (uA)
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA (uA)
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 3 of 6 groups Program Name MK 4116

(A) Range of steps within which to do all parametric tests: step 3 to step 13
 (B) Close relays during: Parametric Functional

Voltage	Test Limit	K1	K1
V1 = <u>+XXXX</u> V	I1 = <u>XXXX</u> mA	K2	K2
V2 = <u>+XXXX</u> V	I2 = <u>XXXX</u> mA	K3	K3
V3 = <u>-XXXX</u> V	I3 = <u>XXXX</u> mA	K4	K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = <u>XXXX</u> V	<u>XXXX</u> V
IIH = _____ mA/uA	@ VIH = <u>XXXX</u> V	<u>XXXX</u> V
VOL = _____ V	@ IOL = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
VOH = _____ V	@ IOH = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
IZL = _____ mA/uA	@ VZL = <u>XXXX</u> V	
IZH = _____ mA/uA	@ VZH = <u>XXXX</u> V	
IOS = <u>XXXX</u> mA/uA(min)	<u>XXXX</u> mA/uA(max) @ VOS = <u>XXXX</u> V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = <u>XXXX</u> V	<u>XXXX</u> V
IIH = _____ mA/uA	@ VIH = <u>XXXX</u> V	<u>XXXX</u> V
VOL = _____ V	@ IOL = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
VOH = _____ V	@ IOH = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
IZL = _____ mA/uA	@ VZL = <u>XXXX</u> V	
IZH = _____ mA/uA	@ VZH = <u>XXXX</u> V	
IOS = <u>XXXX</u> mA/uA(min)	<u>XXXX</u> mA/uA(max) @ VOS = <u>XXXX</u> V	

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-29h. Alternate parameters screen worksheet, group 3, for 4116 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 4 of 6 groups Program Name MX 4116

Power Supplies ①②③

(A) Power Supplies tested at step 14

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+5.50</u> V	I1 = <u>10.0</u> mA	<u>5.00</u> mA
V2 = <u>+13.2</u> V	I2 = <u>25.8</u> mA	<u>50.0</u> mA
V3 = <u>-5.00</u> V	I3 = <u>200</u> mA	<u>2.00</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = <u>10.0</u> mA/μA	@ VIL = <u>0.00</u> V	<u>0.00</u> V
IIH = <u>10.0</u> mA/μA	@ VIH = <u>7.00</u> V	<u>2.20</u> V
VOL = <u>0.40</u> V	@ IOL = _____ mA/μA	<u>4.20</u> mA/μA
VOH = <u>2.40</u> V	@ IOH = _____ mA/μA	<u>5.00</u> mA/μA
IZL = _____ mA/μA	@ VZL = _____ V	
IZH = _____ mA/μA	@ VZH = _____ V	
IOS = _____ mA/μA(min)	_____ mA/μA(max) @ VOS = _____ V	

Figure 4-29i. Parameters screen worksheet, group 4, for 4116 program.

(C) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = <u>10.0</u> mA/μA	@ VIL = <u>0.00</u> V	<u>0.00</u> V
IIH = <u>10.0</u> mA/μA	@ VIH = <u>7.00</u> V	<u>2.40</u> V
VOL = <u>0.40</u> V	@ IOL = _____ mA/μA	<u>20.0</u> mA/μA
VOH = <u>2.40</u> V	@ IOH = _____ mA/μA	<u>20.0</u> mA/μA
IZL = _____ mA/μA	@ VZL = _____ V	
IZH = _____ mA/μA	@ VZH = _____ V	
IOS = _____ mA/μA(min)	_____ mA/μA(max) @ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 4 of 6 groups Program Name MX 4116

(A) Range of steps within which to do all parametric tests: step <u>3</u> to step <u>13</u>	(B) Close relays during:
Voltage	Parametric Functional
	K1 K1
V1 = + XXXX* V	K2 K2
V2 = + XXXX V	K3 K3
V3 = - XXXX V	K4 K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/μA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/μA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/μA	XXXX mA/μA
VOH = _____ V	@ IOH = XXXX mA/μA	XXXX mA/μA
IZL = _____ mA/μA	@ VZL = XXXX V	
IZH = _____ mA/μA	@ VZH = XXXX V	
IOS = XXXX mA/μA(min)	XXXX mA/μA(max) @ VOS = XXXX V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/μA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/μA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/μA	XXXX mA/μA
VOH = _____ V	@ IOH = XXXX mA/μA	XXXX mA/μA
IZL = _____ mA/μA	@ VZL = XXXX V	
IZH = _____ mA/μA	@ VZH = XXXX V	
IOS = XXXX mA/μA(min)	XXXX mA/μA(max) @ VOS = XXXX V	

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-29j. Alternate parameters screen worksheet, group 4, for 4116 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 5 of 6 groups Program Name MX 9116Power Supplies ①②③(A) Power Supplies tested at step 27(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+4.50</u> V	I1 = <u>10.04</u> mA	<u>5.00</u> mA
V2 = <u>+10.8</u> V	I2 = <u>2.2</u> mA	<u>50.0</u> mA
V3 = <u>-4.50</u> V	I3 = <u>100.4</u> mA	<u>2.00</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.40</u> V
VOL = <u>0.90</u> V	@ IOL = _____ mA/uA	<u>4.80</u> mA (uA)
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>5.00</u> mA (uA)
IZL = <u>10.0</u> mA (uA)	@ VZL = <u>0.00</u> V	
IZH = <u>10.0</u> mA (uA)	@ VZH = <u>5.50</u> V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

Figure 4-29k. Parameters screen worksheet, group 5, for 4116 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.00</u> V
VOL = <u>0.90</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA (uA)
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA (uA)
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 5 of 6 groups Program Name MX 9116

(A) Range of steps within which to do all parametric tests: step <u>27</u> to step <u>27</u>	(B) Close relays during:
Voltage	Parametric Functional
Test Limit	K1 K1
V1 = + XXXX* V	I1 = XXXX mA K2 K2
V2 = + XXXX V	I2 = XXXX mA K3 K3
V3 = - XXXX V	I3 = XXXX mA K4 K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max) @ VOS = XXXX V	

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-29l. Alternate parameters screen worksheet, group 5, for 4116 program.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 6 of 6 groups Program Name MX 4116

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step 27

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+5.50</u> V	I1 = <u>10.0</u> mA	<u>5.00</u> mA
V2 = <u>+13.2</u> V	I2 = <u>2.30</u> mA	<u>50.0</u> mA
V3 = <u>-5.70</u> V	I3 = <u>100.0</u> mA	<u>2.00</u> mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.20</u> V
VOL = <u>0.40</u> V	@ IOL = _____ mA/uA	<u>4.20</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>5.00</u> mA/uA
IZL = <u>10.0</u> mA/uA	@ VZL = <u>0.00</u> V	
IZH = <u>10.0</u> mA/uA	@ VZH = <u>5.50</u> V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

Figure 4-29m. Parameters screen worksheet, group 6, for 4116 program.

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.80</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.40</u> V
VOL = <u>0.40</u> V	@ IOL = _____ mA/uA	<u>20.0</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>20.0</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 6 of 6 groups Program Name MX 4116

(A) Range of steps within which to do all parametric tests: step 27 to step 27

(B) Close relays during: Parametric Functional

Voltage	Test Limit		
V1 = + XXXX* V	I1 = XXXX mA	_____ K1	_____ K1
V2 = + XXXX V	I2 = XXXX mA	_____ K2	_____ K2
V3 = - XXXX V	I3 = XXXX mA	_____ K3	_____ K3
		_____ K4	_____ K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max)	@ VOS = XXXX V

(D) ----- Pin Set 2 -----

Parametric Test Limits	-----Test Conditions-----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VOH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max)	@ VOS = XXXX V

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-29n. Alternate parameters screen worksheet, group 6, for 4116 program.

TRUTH TABLE

4116

```

-----
Pin:      11111111122222
:123456789012345678901234
-----X-----
Pin ID:IIIIIXIIOTIIIVVVXIIIIIIIG
-----
S 0000:XXXXXXXXXXXXVVVXXXXXXXXXG
T 0001:iiioXiiXXoiVVVXooooooioG
E 0002:iiioXiiXXiiVVVXooooooioG
P :J 0001-0008
  0003:iiiiXooXooVVVXooooooioG
  0004:iiiiXooXooVVVXooooooioG
  0005:iiiiXooXooVVVXooooooioG
  0006:iiiiXooXooVVVXooooooioG
  0007:iiiiXooXooVVVXooooooioG
  0008:iiiiXooXooVVVXooooooioG
  0009:iiiiXooXooVVVXooooooioG
S 0010:iiiiXooXoiVVVXooooooioG
T 0011:iiiiXooXioVVVXooooooioG
E 0012:iiiiXoiXXooVVVXooooooioG
P 0013:iiiiXioXXooVVVXooooooioG
  0014:iiioXioXXoiVVVXooooooioG
  0015:iiioXioXXooVVVXooooooioG
  0016:iiioXooXooVVVXooooooioG
  0017:iiioXiiXXoiVVVXooooooioG
  0018:iiioXiiXXoiVVVXooooooioG
  0019:iiioXiiXXoiVVVXooooooioG
  0020:iiioXiiXXoiVVVXooooooioG
S 0021:iiioXiiXXooVVVXooooooioG
T 0022:iiioXoiXXooVVVXooooooioG
E 0023:iiioXiiXXoiVVVXooooooioG
P 0024:iiioXioXXooVVVXooooooioG
  0025:iiioXiiXioVVVXooooooioG
  0026:iiioXiiXXoiVVVXooooooioG
  0027:iiioXiiXTiiVVVXooooooioG
  0028:iiioXioXXXXVVVXXXXXXXXXG
  0029:iiioXioXXXXVVVXXXXXXXXXG
      :J 0028-0008
  0030:iiioXioXXXXVVVXXXXXXXXXG
S 0031:iiioXooXXXXVVVXXXXXXXXXG
T 0032:iiioXiiXXXXVVVXXXXXXXXXG
E 0033:iiioXoiXXXXVVVXXXXXXXXXG
P 0034:iiioXioXXXXVVVXXXXXXXXXG
  0035:iiioXioXXXXVVVXXXXXXXXXG
  0036:iiioXioXXXXVVVXXXXXXXXXG
  0037:iiioXioXXXXVVVXXXXXXXXXG
  0038:iiioXooXXXXVVVXXXXXXXXXG
  0039:iiioXooXXXXVVVXXXXXXXXXG
  0040:iiioXooXXXXVVVXXXXXXXXXG
  0041:iiioXooXXXXVVVXXXXXXXXXG
S 0042:iiioXooXXXXVVVXXXXXXXXXG
T 0043:iiioXooXXXXVVVXXXXXXXXXG
E 0044:iiioXooXXXXVVVXXXXXXXXXG
P 0045:iiioXooXXXXVVVXXXXXXXXXG
  0046:iiioXooXXXXVVVXXXXXXXXXG
  0047:iiioXooXXXXVVVXXXXXXXXXG
  0048:iiioXooXXXXVVVXXXXXXXXXG
  0049:iiioXooXXXXVVVXXXXXXXXXG

```

TRUTH TABLE

4116

```

-----
Pin:      11111111122222
:123456789012345678901234
-----X-----
Pin ID:IIIIIXIIOTIIIVVVXIIIIIIIG
-----
  0050:iooooXooXXXXVVVXXXXXXXXXG
  0051:iooooXooXXXXVVVXXXXXXXXXG
  0052:iooooXooXXXXVVVXXXXXXXXXG
S 0053:iooooXooXXXXVVVXXXXXXXXXG
T :J 0038-1023
E 0054:ooiiiXioXXXXVVVXXXXXXXXXG
P 0055:ooiiiXioXXXXVVVXXXXXXXXXG
      :W 1870
  0056:ooiiiXioXXXXVVVXXXXXXXXXG
  0057:iooooXioXXXXVVVXXXXXXXXXG
  0058:iooooXoiXXXXVVVXXXXXXXXXG
  0059:iooooXioXXXXVVVXXXXXXXXXG
  0060:iooooXoiXXXXVVVXXXXXXXXXG
  0061:iooooXioXXXXVVVXXXXXXXXXG
S 0062:iooooXoiXXXXVVVXXXXXXXXXG
T 0063:iooooXioXXXXVVVXXXXXXXXXG
E 0064:iooooXoiXXXXVVVXXXXXXXXXG
P 0065:iooooXioXXXXVVVXXXXXXXXXG
  0066:iooooXoiXXXXVVVXXXXXXXXXG
  0067:iooooXioXXXXVVVXXXXXXXXXG
  0068:iooooXoiXXXXVVVXXXXXXXXXG
  0069:iooooXioXXXXVVVXXXXXXXXXG
  0070:iooooXoiXXXXVVVXXXXXXXXXG
  0071:iooooXioXXXXVVVXXXXXXXXXG
  0072:iooooXoiXXXXVVVXXXXXXXXXG
S 0073:iooooXioXXXXVVVXXXXXXXXXG
T 0074:iooooXoiXXXXVVVXXXXXXXXXG
E 0075:iooooXioXXXXVVVXXXXXXXXXG
P 0076:iooooXoiXXXXVVVXXXXXXXXXG
  0077:iooooXioXXXXVVVXXXXXXXXXG
  0078:iooooXoiXXXXVVVXXXXXXXXXG
  0079:iooooXioXXXXVVVXXXXXXXXXG
  0080:iooooXoiXXXXVVVXXXXXXXXXG
  0081:iooooXioXXXXVVVXXXXXXXXXG
  0082:iooooXoiXXXXVVVXXXXXXXXXG
  0083:iooooXioXXXXVVVXXXXXXXXXG
S 0084:iooooXoiXXXXVVVXXXXXXXXXG
T 0085:iooooXioXXXXVVVXXXXXXXXXG
E 0086:iooooXoiXXXXVVVXXXXXXXXXG
P 0087:iooooXioXXXXVVVXXXXXXXXXG
  0088:iooooXoiXXXXVVVXXXXXXXXXG
      :J 0057-1023
  0089:ioiiiXiiXXXXVVVXXXXXXXXXG
  0090:ioiiiXiiXXXXVVVXXXXXXXXXG
      :W 1742
  0091:ioiiiXiiXXXXVVVXXXXXXXXXG
  0092:iooooXiiXXXXVVVXXXXXXXXXG
S 0093:iooooXoiXXXXVVVXXXXXXXXXG
T 0094:iooooXiiXXXXVVVXXXXXXXXXG
E 0095:iooooXoiXXXXVVVXXXXXXXXXG
P 0096:iooooXiiXXXXVVVXXXXXXXXXG
  0097:iooooXoiXXXXVVVXXXXXXXXXG

```

Figure 4-29a. Truth table worksheet for 4116 program.

TRUTH TABLE

4116

```

-----
Pin:          11111111122222
:123456789012345678901234
-----*-----
Pin ID:IIIIIXIIOTIIIVVVXIIIIIIIG
-----
0098:ioioXiiXXXXVVVXXXXXXXXXG
0099:ioioXoo1XXXVVVXXXXXXXXXG
0100:ioioXiiXXXXVVVXXXXXXXXXG
0101:ioioXoo1XXXVVVXXXXXXXXXG
0102:ioioXiiXXXXVVVXXXXXXXXXG
0103:ioioXoo1XXXVVVXXXXXXXXXG
S 0104:ioioXiiXXXXVVVXXXXXXXXXG
T 0105:ioioXoo1XXXVVVXXXXXXXXXG
E 0106:ioioXiiXXXXVVVXXXXXXXXXG
F 0107:ioioXoo1XXXVVVXXXXXXXXXG
0108:ioioXiiXXXXVVVXXXXXXXXXG
0109:ioioXoo1XXXVVVXXXXXXXXXG
0110:ioioXiiXXXXVVVXXXXXXXXXG
0111:ioioXoo1XXXVVVXXXXXXXXXG
0112:ioioXiiXXXXVVVXXXXXXXXXG
0113:ioioXoo1XXXVVVXXXXXXXXXG
0114:ioioXiiXXXXVVVXXXXXXXXXG
S 0115:ioioXoo1XXXVVVXXXXXXXXXG
T 0116:ioioXiiXXXXVVVXXXXXXXXXG
E 0117:ioioXoo1XXXVVVXXXXXXXXXG
F 0118:ioioXiiXXXXVVVXXXXXXXXXG
0119:ioioXoo1XXXVVVXXXXXXXXXG
0120:ioioXiiXXXXVVVXXXXXXXXXG
0121:ioioXoo1XXXVVVXXXXXXXXXG
0122:ioioXiiXXXXVVVXXXXXXXXXG
0123:ioioXoo1XXXVVVXXXXXXXXXG
:J 0092-1023
S 0124:XXXXXXXXXXXXVVVXXXXXXXXXG
T      :E
E 0125:
F      :

```

Figure 4-29p. Truth table worksheet for 4116 program.

4.11.4 ROM

ROMs are divided by device family the same way that the RAMs are. One thing common to all types of ROM devices is that the outputs of the truth table have already been established at the time of manufacture. The truth-table worksheet for testing ROMs with less than 4K words of data can be easily prepared. This is done by calling up the binary macro, weighting the input pins, and generating as many steps of binary code as there are words of data in the DUT, coding all the outputs L. The first step of the truth-table should have all input address lines low. The next step would call up the binary macro, with the inputs weighted from 0 up. The number of steps of binary code to be generated is determined by the size of the ROM. The program should then be run in the learn mode with a known-good device.

ROMs with more than 4K minus 1 words of data will require the use of more than one test program in order to accommodate the test. The easiest way to generate the several programs that will be required to test a large ROM is to use the binary macro to generate the twelve least-significant bits of the address locations. A 16K ROM, for example, requires a 14-bit address word to address each location uniquely in its memory. The binary macro in the system can generate 12 bits of binary code. Manually entering the two most significant bits of the address (00, 01, 10, and 11), weighting the twelve least significant bits in the appropriate order, coding the outputs L, and generating 4090 steps of binary code, can make the system do the bulk of the program generation. Five programs will be required to test a 16K ROM, because only 4K minus 1 steps are available (one step is required for system initialization). While this means that several addresses must be manually entered, it allows for overlapping portions of each program, and ensures that no memory location is left untested. Parametric testing must be performed during the first test program, but would not be necessary (although desirable) in the subsequent programs for the device.

After the address locations have been generated using the binary macro, it is recommended that the programs be copied onto another tape cartridge prior to executing the learn routine; this will prevent having to generate the series of programs a second time if the first ROM used in the learn mode contains a defect.

Owing to the fixed nature of the data in the ROM, parametric testing should run from the step when normal operation is assured after applying power to the step where all pins have been exercised through high, low, and, if applicable, high-impedance states. Functional testing should also not begin until the step when normal operation is assured.

Some NMOS ROMs require 3 power supplies, while others only need one. Like NMOS RAMs, they use chip select or address signals to strobe data out. Most CMOS ROMs use a single power supply at 5 V, while some can operate at 5, 10, or 15 V.

TTL ROMs also require only one power supply voltage and use chip select or address signals to strobe data.

4.11.5 PROM (BLANK AND PROGRAMMED)

PROM families can be subdivided into two classes: blank and programmed. Test procedures for either class

are very similar to the procedures used for testing ROMs of that device family. The truth table is determined by the data programmed in. In the case of blank PROMs, these data will be either all 1's or all 0's, as noted in the manufacturer's data sheet for that particular device. In the case of programmed PROMs, the data will be whatever data the users have programmed into the devices.

Parametric testing of the blank PROMs will be somewhat limited in that not all possible states will be available for test on every pin. Some devices have extra fuses for test purposes that were programmed by the manufacturer to ensure proper functioning of the fuses. These devices can have those addresses checked for the opposite logic state of the unprogrammed fuses. Parametric testing of programmed PROMs will require that the test step through each possible logic state of every pin; depending upon the data programmed into the device, this may take a large portion of the truth table. Functional testing for PROMs takes the same form as the tests for ROMs.

In testing either blank or programmed PROMs, care must be taken that the voltages applied to the device do not blow the remaining fuse links, rendering the device useless. This programming voltage can be quite close to the normal operating voltage.

TTL PROMs use a normal operating voltage between 4.75 V and 5.25 V. For some devices, the programming voltage can be as low as 5.75 V, although it can be as high as 12.25 V.

ECL PROMs do not require the same close attention, since they normally operate between -5.46 V and -4.94 V. The fuse links in an ECL PROM are blown by a programming voltage between +6 V and +7.5 V, so the major precaution is to ensure that the correct polarity power supply is selected.

4.11.6 EPROM (BLANK AND PROGRAMMED)

Like PROMs, EPROM families can be subdivided into two classes, blank and programmed. The voltage ranges required for programming EPROMs generally fall outside the voltage ranges of the system. This greatly reduces the chance of inadvertent programming. Unlike PROMs, however, inadvertent application of the programming voltage to the devices may be corrected by erasing and reprogramming the device. Test procedures for either class are very similar to the procedures used for testing PROMs of that device family. The truth table is determined by the data programmed in. In the case of blank EPROMs, these data will be either all 1's or all 0's, as noted in the data sheet for that particular device. In the case of programmed EPROMs, the data will be whatever values the users have entered.

Parametric testing of the blank EPROMs will be somewhat limited in that not all possible states will be available for test on every pin. Parametric testing of programmed EPROMs will require that the test step through each possible logic state of every pin; this may take a large portion of the truth table, depending upon the data stored in the device. Functional testing for EPROMs takes the same form as the tests for ROMs and PROMs.

NMOS EPROMs use either only 1 supply voltage or 3 supply voltages; those that use a single supply voltage are

programmed at 24 V to 26 V. Devices which use 3 supply voltages require a programming voltage between 25 V and 27 V.

CMOS EPROMs using a +5-V supply for normal operation require -40-V pulses for programming.

In both families described above, the programming voltages fall well outside the capabilities of the system's device power supplies.

4.11.7 Program Example, 2716 Figures 4-30 through 4-32 General.

The 2716 is a 2K × 8 EPROM. The procedure used in this example can be applied to ROMs and PROMs as well as EPROMs.

CAUTION

Continuity tests should not be performed because the system delivers 1.25 mA during the continuity test, and the DUT could be damaged. If a continuity test must be performed, the current level can be lowered by changing the system software (which is beyond the scope of this discussion).

Program Layout Chart.

This program is designed to perform dc parametric and functional tests on the 2716. The truth table is generated using the binary macro to create 2K steps of binary code for the memory input address lines with the outputs automatically put into the learn mode, then writing 2 more steps to test the power supply. This produces a program which can be written onto another tape cartridge, before the learn mode is executed, for future use in testing 2716 EPROMs programmed with different data. Once this has been done, the same basic program can be used to test blank or programmed devices.

Two groups are used because the portion of the truth table where all inputs change states may not be near the portion of the truth table where all the outputs change states. The alternate parameters screen for the first group will specify the start and stop steps required to test the inputs parametrically, while the alternate parameters screen for the second group will specify the start and stop steps required to test the outputs. This will allow the truth table to be structured to test the inputs in a portion of the truth table that will be the same regardless of the data stored in the device. The portion of the truth table used to test the outputs will change when the data stored in the device are changed.

In this example, most of the pins will change state in the last few steps of the truth table, so the parametric test start and stop steps will reflect this. The parametric results

screen should be selected in the display-mode screen; this will show which pins are not being exercised. The portion of the truth table used in the parametric test sequence should be expanded until all the inputs and outputs are being exercised. The power supply test will be performed at step 2049.

NOTE

Since pin 21 is the programming enable pin (Vpp), it should be wired to +5 V on the socket adaptor and entered as a logic 1 throughout the truth table. This means that IIL cannot be tested on pin 21.

Worksheet Organization.

Describe Screen. Pin 21 is placed in pin set 2 because it requires a VIH higher than the other inputs. The clock frequency is 1 MHz; combined with the sync value of C4, the frequency to the DUT will be 250 kHz.

Parameters Group 1 Screen. The power supply is set for 5.25 V and is tested at 30 mA with an I-max of 150 mA. The current test limit is calculated by adding Icc and Ipp. In pin set 1, IIL and IZH are tested parametrically, while VOL and VOH are tested functionally. No tests are performed in pin set 2.

Alternate Parameters Group 1 Screen. Parametric testing of the inputs is specified from step 2046 through the end of the truth table.

Parameters Group 2 Screen. The power supply is set for 5.25 V because pin 21 must have 5 V at all times. This device cannot be tested at minimum Vcc below 5 V. VOL and VOH are tested both parametrically and functionally in this group.

Alternate Parameters Group 2 Screen. Parametric testing of the outputs is enabled from step 2045 through the end of the truth table.

Truth Table Screen. As described above, the truth table is generated by the use of the binary macro. In the first step of the truth table, all address line inputs are set to 0 and all outputs are set to L. The binary macro command is entered to generate 2047 steps, with the address line inputs weighted from 0 to 10 ("A" in hexadecimal). The binary macro command is executed, producing a truth table 2048 steps long, and the final step is entered to test the power supplies and to end the test program.

Run-mode Screen. Functional and parametric tests are selected and are enabled in both groups. Continuity testing is not selected because of the high current level produced by the system during that test. The functional test start and stop default values are entered.



2716 16K (2K × 8) UV ERASABLE PROM

- **Fast Access Time**
 - 350 ns Max. 2716-1
 - 390 ns Max. 2716-2
 - 450 ns Max. 2716
 - 490 ns Max. 2716-5
 - 650 ns Max. 2716-6
- **Single +5V Power Supply**
- **Low Power Dissipation**
 - 525 mW Max. Active Power
 - 132 mW Max. Standby Power
- **Pin Compatible to Intel® 2732 EPROM**
- **Simple Programming Requirements**
 - Single Location Programming
 - Programs with One 50 ms Pulse
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

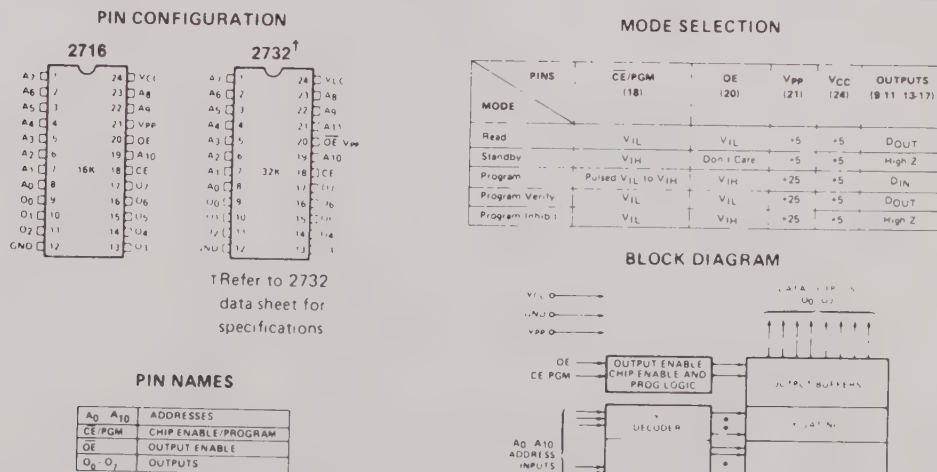


Figure 4-30a. Excerpt from Intel Component Data Catalog, Intel, 1980, page 2-7.

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to -0.3V
V _{PP} Supply Voltage with Respect to Ground During Program	+26.5V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2	2716-5	2716-6
Temperature Range	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
V _{CC} Power Supply [1,2]	5V ±5%	5V ±10%	5V ±5%	5V ±5%	5V ±5%
V _{PP} Power Supply [2]	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}

READ OPERATION

D.C. and Operating Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ. [3]	Max.		
I _{LI}	Input Load Current			10	μA	V _{IN} = 5.25V
I _{LO}	Output Leakage Current			10	μA	V _{OUT} = 5.25V
I _{PP1} [2]	V _{PP} Current			5	mA	V _{PP} = 5.25V
I _{CC1} [2]	V _{CC} Current (Standby)		10	25	mA	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$
I _{CC2} [2]	V _{CC} Current (Active)		57	100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V _{IL}	Input Low Voltage	-0.1		0.8	V	
V _{IH}	Input High Voltage	2.0		V _{CC} +1	V	
V _{OL}	Output Low Voltage			0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -400 μA

- NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
 2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
 3. Typical values are for T_A = 25°C and nominal supply voltages.
 4. This parameter is only sampled and is not 100% tested.

Typical Characteristics

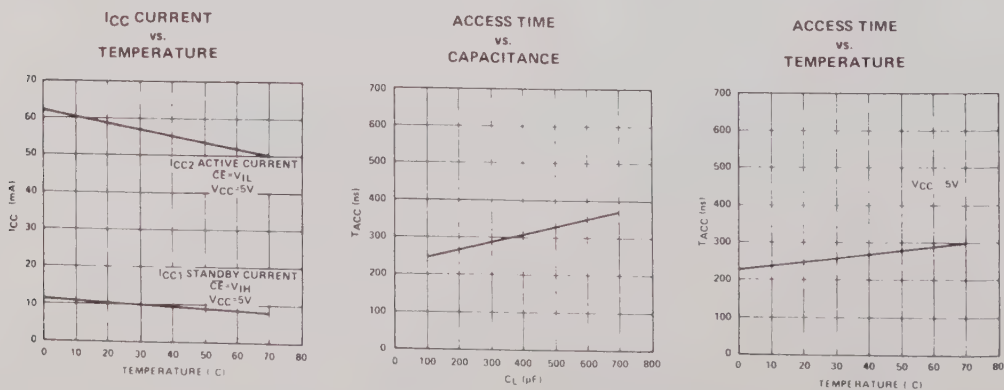


Figure 4-30b. Excerpt from Intel Component Data Catalog, Intel, 1980, page 2-8.

Step Number	Activity Start																								
	Fill out Describe, Run-Mode, and Parameters Groups 1 and 2 worksheets. Enter data into 1732 screens. Begin truth table worksheet.																								
0	Set all inputs except pin 21 to 0, set pin 21 to 1, set all outputs to L. Use the binary macro command to generate 2047 steps: [B] [2] [0] [4] [7] [ENTER] and weight the input pins as follows: <table><tr><td>input pins</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>19</td><td>22</td><td>23</td></tr><tr><td>weights</td><td>[7]</td><td>[6]</td><td>[5]</td><td>[4]</td><td>[3]</td><td>[2]</td><td>[1]</td><td>[0]</td><td>[A]</td><td>[9]</td><td>[8]</td></tr></table> and execute the binary macro by pressing [ENTER].	input pins	1	2	3	4	5	6	7	8	19	22	23	weights	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[A]	[9]	[8]
input pins	1	2	3	4	5	6	7	8	19	22	23														
weights	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[A]	[9]	[8]														
2048	Set pins 18, 20, and 21 high and all other inputs low. Set all outputs to L.																								
2049	Set all inputs except pin 21 low. Set all outputs to X. Enter End command. Specify power supply test at step 2049 on parameters screen for group 1. Set parametric start and stop steps on the alternate parameters screen for group 1 at 2046 and End. This will test the inputs parametrically. Copy program onto another tape cartridge. Run learn mode. Examine truth table for a group of steps where all outputs change state. Set parametric test start and stop steps on alternate parameters screen for group 2 to include those steps found above. Run test. Call up the parametric results display screen and check that all pins except pin 21 are changing state. If not, expand the area of the truth table that is checked in the parametric test.																								
	END																								

Figure 4-31 Program layout chart 2716 program example.

1732 DESCRIBE SCREEN WORKSHEET

A. Program Name: 2716

Type of Device (if different from program name) or other comment: _____

B. Number of pins per device: 24
 Number of Test Groups per Test Program: 2

C. Clocks
 C0: 1.00 MHz (One of these fifteen choices) | 8.00 2.29 1.33
 | 5.53 2.00 1.23
 | 4.00 1.78 1.14
 Sync: C1 = C0/1 C8 = C0/8 | 3.20 1.60 1.07
 C2 = C0/2 CF = C0/16 | 2.66 1.45 1.00
X C4 = C0/4 External

D. Pin Assignments

	ID	S	ID	S	ID	S
1.	<u>I</u>	<u>I</u>	17.	<u>I</u>	<u>I</u>	<u> </u>
2.	<u>I</u>	<u>I</u>	18.	<u>I</u>	<u>I</u>	<u> </u>
3.	<u>I</u>	<u>I</u>	19.	<u>I</u>	<u>I</u>	<u> </u>
4.	<u>I</u>	<u>I</u>	20.	<u>I</u>	<u>I</u>	<u> </u>
5.	<u>I</u>	<u>I</u>	21.	<u>I</u>	<u>2</u>	<u> </u>
6.	<u>I</u>	<u>I</u>	22.	<u>I</u>	<u>I</u>	<u> </u>
7.	<u>I</u>	<u>I</u>	23.	<u>I</u>	<u>I</u>	<u> </u>
8.	<u>I</u>	<u>I</u>	24.	<u>V</u>	<u>I</u>	<u> </u>
9.	<u>I</u>	<u>I</u>	25.	<u> </u>	<u> </u>	<u> </u>
10.	<u>I</u>	<u>I</u>	26.	<u> </u>	<u> </u>	<u> </u>
11.	<u>I</u>	<u>I</u>	27.	<u> </u>	<u> </u>	<u> </u>
12.	<u>G</u>	<u> </u>	28.	<u> </u>	<u> </u>	<u> </u>
13.	<u>I</u>	<u>I</u>	29.	<u> </u>	<u> </u>	<u> </u>
14.	<u>I</u>	<u>I</u>	30.	<u> </u>	<u> </u>	<u> </u>
15.	<u>I</u>	<u>I</u>	31.	<u> </u>	<u> </u>	<u> </u>
16.	<u>I</u>	<u>I</u>	32.	<u> </u>	<u> </u>	<u> </u>

Definitions (for ID)

I (1,2) = Input
 O (1,2) = Output
 B = Bidirectional
 T = Tristate
 X = Don't Care
 V (1,2,3) = Power
 G = Ground
 C (1,2,3) = Clock
 S = Pin Set
 (default is 1)

Figure 4-32a. Describe screen worksheet for 2716 program example.

1732 RUN-MODE SCREEN WORKSHEET

A. Test Sequence: FP (for example: CFP, CPF, F, or CP)

B.

	Bin 1	Bin 2	Bin 3	Bin 4	Bin 5	
	F	P	F	P	F	P
G 1	<u>X</u>	<u>X</u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
R 2	<u>X</u>	<u>X</u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
O 3	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
U 4	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
P 5	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
S 6	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>

Test Procedure

C. Functional Test: Step to step

D. All Groups First Failure
X All Groups (use if binning is needed)
 Stop After Each Group
 Test Continuously to Failure
 Test Continuously

E. Single Step

F. Keyboard IS NOT Locked. (Password = up to 6 characters)

Figure 4-32b. Run-mode screen worksheet for 2716 program example.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 2 groups Program Name 2716

Power Supplies (1) 2, 3)

(A) Power Supplies tested at step 2049

(B) Power Supply
Shutdown Current
I-max
(for this group)

Voltage	Test Limit	
V1 = <u>+5.25</u> V	I1 = <u>30</u> mA	<u>150</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = <u>10.0</u> mA/uA	@ VIL = <u>5.25</u> V	<u>450m</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.00</u> V
VOL = <u>450m</u> V	@ IOL = _____ mA/uA	<u>2.10</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	<u>400</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = <u>10.0</u> mA/uA	@ VZH = <u>5.25</u> V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

Figure 4-32c. Parameters screen worksheet, group 1, for 2716 program example.

(C) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.000</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>5.00</u> V
VOL = <u>450m</u> V	@ IOL = _____ mA/uA	_____ mA/uA
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	@ VOS = _____ V	

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 1 of 2 groups Program Name 2716

(A) Range of steps within which to do all parametric tests: step 2046 to step END

(B) Close relays during:

Test Limit	Parametric	Functional
V1 = <u>+XXXX</u> V	I1 = <u>XXXX</u> mA	_____ K1
V2 = <u>+XXXX</u> V	I2 = <u>XXXX</u> mA	_____ K2
V3 = <u>-XXXX</u> V	I3 = <u>XXXX</u> mA	_____ K3
		_____ K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = <u>XXXX</u> V	<u>XXXX</u> V
IIH = _____ mA/uA	@ VIH = <u>XXXX</u> V	<u>XXXX</u> V
VOL = _____ V	@ IOL = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
VOH = _____ V	@ IOH = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
IZL = _____ mA/uA	@ VZL = <u>XXXX</u> V	
IZH = _____ mA/uA	@ VZH = <u>XXXX</u> V	
IOS = <u>XXXX</u> mA/uA(min)	@ VOS = <u>XXXX</u> V	

(C) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = <u>XXXX</u> V	<u>XXXX</u> V
IIH = _____ mA/uA	@ VIH = <u>XXXX</u> V	<u>XXXX</u> V
VOL = _____ V	@ IOL = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
VOH = _____ V	@ IOH = <u>XXXX</u> mA/uA	<u>XXXX</u> mA/uA
IZL = _____ mA/uA	@ VZL = <u>XXXX</u> V	
IZH = _____ mA/uA	@ VZH = <u>XXXX</u> V	
IOS = <u>XXXX</u> mA/uA(min)	@ VOS = <u>XXXX</u> V	

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-32d. Alternate parameters screen worksheet, group 1, for 2716 program example.

1732 PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 2 groups Program Name 2716

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____ (B) Power Supply Shutdown Current I-max (for this group)

Voltage	Test Limit	
V1 = <u>+5.25</u> V	I1 = _____ mA	<u>150</u> mA
V2 = <u>+</u> V	I2 = _____ mA	_____ mA
V3 = <u>-</u> V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>450m</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>2.00</u> V
VOL = <u>450m</u> V	@ IOL = <u>2.10</u> mA/uA	<u>2.10</u> mA/uA
VOH = <u>2.40</u> V	@ IOH = <u>400</u> mA/uA	<u>4.00</u> mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

Figure 4-32e. Parameters screen worksheet, group 2, for 2716 program example.

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	<u>0.000</u> V
IIH = _____ mA/uA	@ VIH = _____ V	<u>5.00</u> V
VOL = <u>450m</u> V	@ IOL = _____ mA/uA	_____ mA/uA
VOH = <u>2.40</u> V	@ IOH = _____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max)	@ VOS = _____ V

1732 ALTERNATE PARAMETERS SCREEN WORKSHEET

Device Number (if different from program name) _____

Group 2 of 2 groups Program Name 2716

(A) Range of steps within which to do all parametric tests: step 2045 to step 2049 (B) Close relays during: Parametric Functional

Voltage	Test Limit		
V1 = + XXXX* V	I1 = XXXX mA	_____ K1	_____ K1
V2 = + XXXX V	I2 = XXXX mA	_____ K2	_____ K2
V3 = - XXXX V	I3 = XXXX mA	_____ K3	_____ K3
		_____ K4	_____ K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VCH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max)	@ VOS = XXXX V

(D) ----- Pin Set 2 -----

Parametric Test Limits	Test Conditions	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = XXXX V	XXXX V
IIH = _____ mA/uA	@ VIH = XXXX V	XXXX V
VOL = _____ V	@ IOL = XXXX mA/uA	XXXX mA/uA
VCH = _____ V	@ IOH = XXXX mA/uA	XXXX mA/uA
IZL = _____ mA/uA	@ VZL = XXXX V	
IZH = _____ mA/uA	@ VZH = XXXX V	
IOS = XXXX mA/uA(min)	XXXX mA/uA(max)	@ VOS = XXXX V

* XXXX represents a value determined by an entry on the parameters screen.

Figure 4-32f. Alternate parameters screen worksheet, group 2, for 2716 program example.

Device number if different from program name

PROGRAM NAME 2716

Pin no. (Cross out two lines)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Function	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	DO ₀	DO ₁	DO ₂	V _{SS}	DO ₃	DO ₄	DO ₅	DO ₆
Step	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	[ENTER]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[L]	[L]	[L]	[G]	[L]	[L]	[L]
1	[ENTER]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[L]	[L]	[L]	[G]	[L]	[L]	[L]
2																
3																
4																
5																
6																
7																
8																
9																
10																
11																
12																
13																
14																
15																
16																

Device number if different from program name

PROGRAM NAME 2716

Pin no. (Cross out two lines)	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Function	DO ₇	E	A ₁₀	G	V _{PP}	A ₉	A ₈	V _{CC}								
Step	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	[L]	[O]	[O]	[O]	[I]	[O]	[O]	[V]								
1	[L]	[O]	[O]	[O]	[I]	[O]	[O]	[V]								
2																
3																
4																
5																
6																
7																
8																
9																
10																
11																
12																
13																
14																
15																
16																

Figure 4-32g. Truth table work worksheet for 2716 program example prior to executing binary macro command.

1732 TRUTH-TABLE WORKSHEET

Sheet 1 of 2

Device number if different from program name

PROGRAM NAME 2716

Pin no. (Cross out two lines)		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
		33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Step	Command / Function	ID	A7	A6	A5	A4	A3	A2	A1	A0	D0	D1	D2	Vss	D3	D4	D5
0			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
1	USE BINARY MAPPED		0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
2			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
3			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
4			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
5			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
6			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
7			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
8			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
9			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
10																	
1																	
2																	
3																	
4																	
5																	
6																	
7																	
8																	
9																	
2040																	
1																	
2																	
3																	
4																	
2045			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
5			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
6			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
7			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
8			0	0	0	0	0	0	0	0	L	L	L	G	L	L	L
9			0	0	0	0	0	0	0	0	X	X	X	G	X	X	X

1732 TRUTH TABLE WORKSHEET

Sheet 2 of 2

Device number if different from program name

PROGRAM NAME 2716

Pin no. (Cross out two lines)		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
		33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Step	Command / Function	ID	D0	E	A0	G	Vpp	A9	A8	Vcc							
0			L	0	0	0	0	0	0	V							
1			L	0	0	0	0	0	0	V							
2			L	0	0	0	0	0	0	V							
3			L	0	0	0	0	0	0	V							
4			L	0	0	0	0	0	0	V							
5			L	0	0	0	0	0	0	V							
6			L	0	0	0	0	0	0	V							
7			L	0	0	0	0	0	0	V							
8			L	0	0	0	0	0	0	V							
9			L	0	0	0	0	0	0	V							
10																	
1																	
2																	
3																	
4																	
5																	
6																	
7																	
8																	
9																	
10																	
1																	
2																	
3																	
4																	
5			L	0	0	0	0	0	0	V							
6			L	0	0	0	0	0	0	V							
7			L	0	0	0	0	0	0	V							
8			L	0	0	0	0	0	0	V							
9			X	0	0	0	0	0	0	V							

Figure 4-32h. Truth table worksheet for 2716 program example prior to executing learn mode.

Device number if different from program name

PROGRAM NAME 2716

		Pin no. (Cross out two times)																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
		A7	A6	A5	A4	A3	A2	A1	A0	DP0	DP1	DP2	Vss	DP3	DP4	DP5	DP6		
Step	Cross out	ID	1	1	1	1	1	1	1	T	T	T	G	T	T	T	T	Step	
0			0	0	0	0	0	0	0	0	0	0	G	1	0	0	1	0	
1			0	0	0	0	0	0	0	0	0	0	G	0	1	0	0	1	
2			0	0	0	0	0	0	0	0	0	0	G	1	0	0	1	2	
3			0	0	0	0	0	0	0	0	0	0	G	0	1	0	1	3	
4			0	0	0	0	0	0	0	0	0	0	G	1	0	1	1	4	
5			0	0	0	0	0	0	0	0	0	0	G	1	0	1	0	5	
6			0	0	0	0	0	0	0	0	0	0	G	0	0	1	0	6	
7			0	0	0	0	0	0	0	0	0	0	G	1	1	1	0	7	
8			0	0	0	0	0	0	0	0	0	0	G	0	0	1	0	8	
9			0	0	0	0	0	0	0	0	0	0	G	0	0	1	0	9	
0																		0	
1																		1	
2																		2	
3																		3	
4																		4	
5																		5	
6																		6	
7																		7	
8																		8	
9																		9	
0																		0	
1																		1	
2																		2	
3																		3	
4																		4	
5			1	1	1	1	1	0	0	0	1	0	G	0	1	0	1	5	
6			1	1	1	1	1	0	0	0	1	0	G	0	0	0	0	6	
7			1	1	1	1	1	0	0	0	1	1	G	1	0	1	0	7	
8			0	0	0	0	0	0	0	0	T	T	T	G	T	T	T	8	
9			0	0	0	0	0	0	0	0	X	X	X	G	X	X	X	9	

Device number if different from program name

PROGRAM NAME 2716

		Pin no. (Cross out two times)																		
		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
		DP7	E	A0	G	Vpp	A9	A8	Vcc											
Step	Cross out Concurent	Futurism ID	1	1	1	1	1	1	1	V									Step	
0			1	0	0	0	1	0	0	V									0	
1			1	0	0	0	1	0	0	V									1	
2			0	0	0	0	1	0	0	V									2	
3			1	0	0	0	1	0	0	V									3	
4			1	0	0	0	1	0	0	V									4	
5			1	0	0	0	1	0	0	V									5	
6			0	0	0	0	1	0	0	V									6	
7			0	0	0	0	1	0	0	V									7	
8			0	0	0	0	1	0	0	V									8	
9			1	0	0	0	1	0	0	V									9	
0																			0	
1																			1	
2																			2	
3																			3	
4																			4	
5																			5	
6																			6	
7																			7	
8																			8	
9																			9	
0																			0	
1																			1	
2																			2	
3																			3	
4																			4	
5																			5	
6																			6	
7																			7	
8																			8	
9																			9	
0																			0	
1																			1	
2																			2	
3																			3	
4																			4	
5			1	0	1	0	1	1	1	1	V									5
6			1	0	1	0	1	1	1	1	V									6
7			0	0	1	0	1	1	1	1	V									7
8			T	1	0	1	1	0	0	0	V									8
9			X	0	0	0	0	1	0	0	V									9

Figure 4-32i. Truth table worksheet for 2716 program example after executing learn mode.

4.12 PROGRAMMING FOR LSI DEVICES

4.12.1 Z-80 Timing vs 1732 Timing

Figure 4-33

In planning a test program for the Z-80 microprocessor, the main consideration is to be sure that the clock to the Z-80 is the same clock as for the system SYNC input. Thus, the Z-80 and the system are synchronized. The timing of the Z-80 cycles will have a direct relationship to the "Gate/Strobe" of the system.

A 1-MHz clock with a SYNC of C1 is shown in the timing figure of a fetch cycle. The gate (sending data to the DUT) and the strobe (receiving data from the DUT) are shown in the preset power-up position, 312 μ sec for the gate and 875 μ sec for the strobe. The address lines, data lines, MREQ L, RD L, M1 L, and RFSH L lines are chosen to demonstrate how the system generates the necessary levels for the Z-80 inputs and how the system senses outputs. (The L after a signal name indicates an active-low signal, the same as a superior bar.)

The system will emulate the world surrounding the Z-80. Since it will serve as memory to the Z-80, the system needs to know when to supply data to the Z-80 or, (in the case of a Z-80 memory write instruction) when to read data from the Z-80. The address lines and control signals are forced or sensed by the system when the Z-80 timing requires, as a function of the truth table.

As an example, assume the op code fetched is from address A00E(hex) and the code is a "jump 0D(hex) locations from A00E(hex)" command. During the fetch cycle, the address bus will be A00E(hex), which the system will sense. The data bus will be required to contain the op code for the "jump relative" JRe (18 in hex). The system drives the data bus, forcing the data bits to the proper levels representing the jump-command code 18(hex). The Z-80 will require a "memory-read" to obtain the count, the operand (0D in hex). The address bus will be A00F(hex) and the data will be 0D(hex). The system will have supplied the data and the Z-80 will have output the address bus to the system to sense.

At this point, the Z-80 will execute the jump instruction by placing on the address bus A01D(hex) and attempting to read the contents of A01D(hex). The system will supply to the data bus the next op code requested by the Z-80 during the fetch cycle.

4.12.2 Truth Table Requirements

Figure 4-34

M L, RD L, WR L, and RFSH L are sensed high and low as a function of the truth table as seen in Figure 4-34. The Z-80 timing for the fetch cycle is what dictates the gate strobe position so that the system knows when to sense the qualified level. Synchronization implies a superposition of the Z-80 timing for the fetch cycle over the system of the same fetch cycle. The data-input pins can be gated later than the control lines by selecting gate/strobe set A for the control pins and gate/strobe set B for the data-input pins.

The system timing with respect to the Z-80 timing has more than sufficient resolution to functionally force inputs and sense outputs. With control of gate/strobe timing and knowledge of the sync relationships between the Z-80 and the system, definition of the test program op code sequence can begin.

4.12.3 Program Example, Z-80

The program example for the Z-80 consists of the portion of the program layout chart dealing with the functional testing of the DUT, a commentary on a portion of the truth table that is used to test the Z-80, and the presentation of the screen printouts. Refer to the **Z-80 Technical Manual** by Zilog for the specifications and description of the Z-80.

Z-80 Program Layout Chart

This chart is not a complete program layout chart; it deals only with the functional testing of the Z-80 on the system. The major factor that has to be taken into consideration is that the 1732 represents the entire outside operating system the Z-80 normally operates in, and has to function as clock, memory, input, and output for the Z-80 as it executes the test program.

Z-80 Program Layout Chart

Step No.	Function or Comment
00 - 03	Reset of the Z-80.
00 - 01	Pin 26 (RESET) held low for 6 T-states.
02 - 03	Pin 26 forced high for 3 T-states. The address bus is checked for a high-impedance condition.
At this point, the Z-80 is reset and will commence a fetch sequence to address 0000H. The system will drive the DATA lines to simulate an address fetch of an XOR A (AFH).	
05 - 08 (XOR A)	This is the fetch sequence; it requires 4 T-states. Each step of the truth table is a single T-state.
05 - 06	The instruction is fetched from memory. (See following discussion.)
07 - 08	Refresh cycle for the dynamic RAMs.
09 - 20 (LD(2000),A)	Fetch and execution of loading the location 2000H with the contents of the A register.
09 - 12	The fetch cycle obtains the op code for the LD (2000), A (3EH) from location 0001H.
13 - 15	Read memory for the address destination (2000H). The Z-80 reads the low-order byte (00H) at location 0002H first, followed by the high-order byte (20H) from location 0003H.

At this point, the Z-80 has read in the instruction LD (2000), A, and is about to write the contents of the A register to memory. By writing to memory, the system can check the results of the XOR A by expecting the data bus to be all zeros. This is the method by which the system can check the internal data paths and register manipulations of the DUT.

19 - 21	The contents of the A register are placed on the data bus and the address line goes to an address of 2000H.
22 - 28 (LD B, 3DH)	Fetch the instruction to load the B register with the bit pattern that placed alternate ones and zeros on the data bus (3DH).
22 - 25	Fetch from location 0004H the LD B op code (06H)
26 - 28	Read from memory the data 3DH from location 0005H.
29 - 32	Fetch from location 0006H the op code 78H and execute the transfer of (B register) to A register.

At this point, the A Register equals B Register equals 3DH. To check this data transfer, the contents of the A Register will be written to memory at location AAAAH.

33 - 45 (LD(AAAA),A)	Load the memory location with the contents of the register.
-------------------------	---

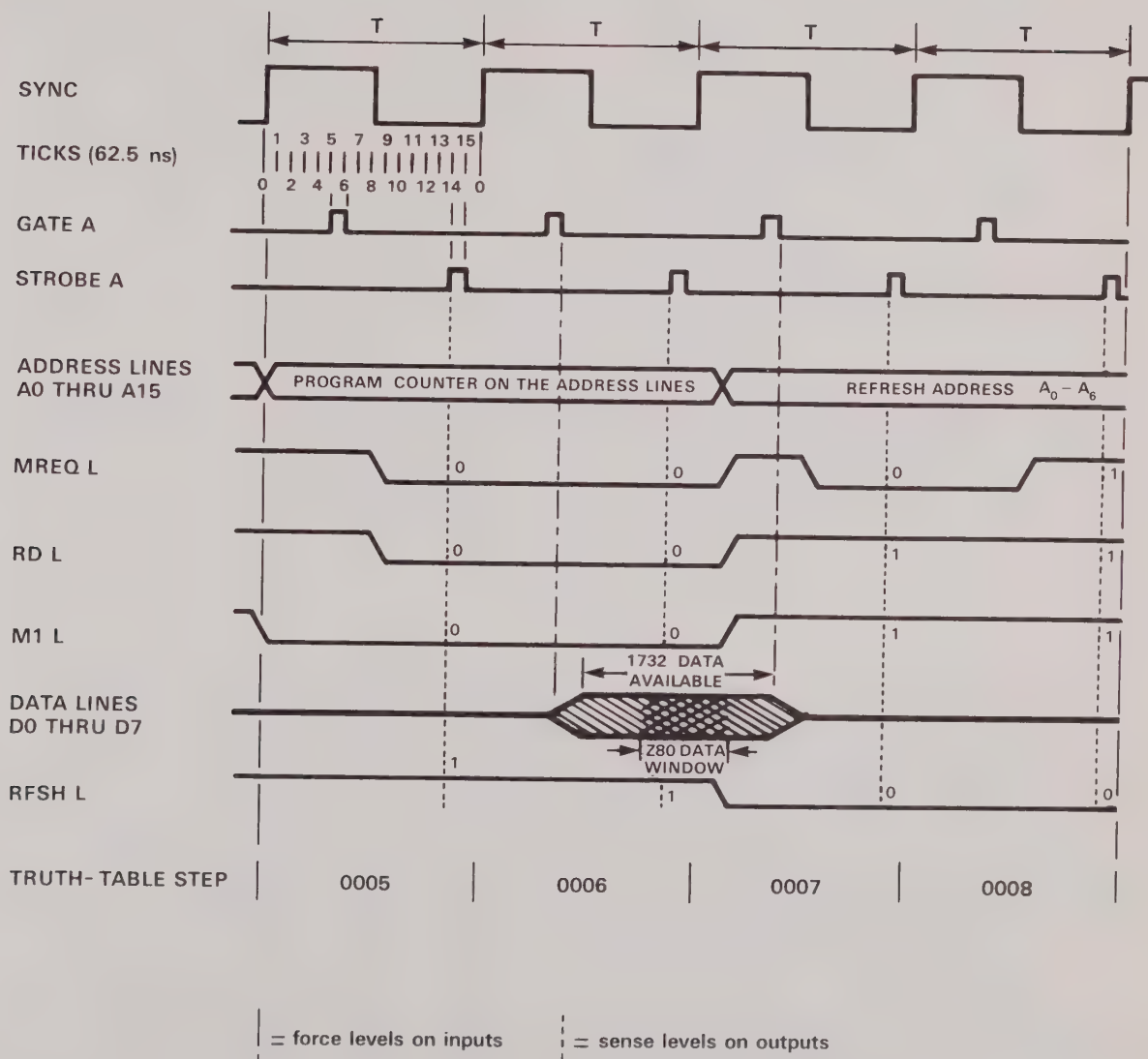


Figure 4-33. Timing diagram for the Z-80.

Location	Contents	Mnemonics and Comments
0000	AF	XOR, A
0001	3E	LD (2000), A
0002	00	Low order byte of address
0003	20	High order byte of address
0004	06	LD B, 3D
0005	3D	Data (3D) for load command in previous step
0006	78	LD A, B
0007	32	Op code for LD (AAAA), A
0008	AA	Low order byte of operand
0009	AA	High order of byte operand
0010	-	
2000	00	From location 0001, load this location with the contents of the A register.
-	-	
AAAA	3D	From locations 0007 through 0009, load this location with the contents of the A register.

This is an example of the method of testing the MPU. The main thrust of the sample program is to allow the MPU do the internal transfers and manipulations and then use the system to check the results by storing register contents in memory.

The system presents data to the Z-80 that simulates the addresses and data that it would obtain from devices external to the Z-80 in an actual operating system. The following is a tabulation of the 1732 test program as the Z-80 perceives it.

Truth Table Effects on DUT Actions

The following examinations of two steps of the truth table will illustrate how the 1732 simulates an operating system for the Z-80. It lists the step number, the address and data in hexadecimal, the function being performed, the pins performing it, and the logic state found at each pin.

Step 0004

Address 0000(hex), data 00(hex)

Address Lines: A0 A1 A2 A3 A4 A5 A6 A7

Pin Numbers: 30 31 32 33 34 35 36 37

Logic State: 0 0 0 0 0 0 0 0

Address Lines: A8 A9 A10 A11 A12 A13 A14 A15

Pin Numbers: 38 39 40 1 2 3 4 5

Logic State: 0 0 0 0 0 0 0 0

Function: MREQ L

Pin Numbers: 19

Logic State: 1

Function: RD L

Pin Numbers: 21

Logic State: 1

Function: M1 L

Pin Numbers: 27

Logic State:

Function: REFSH L

Pin Numbers: 28

Logic State: 1

Data Lines: D0 D1 D2 D3 D4 D5 D6 D7

Pin Numbers: 14 15 12 8 7 9 10 13

Logic State: 0 0 0 0 0 0 0 0

Step 0005

Address 0000(hex), data AF(hex)

Address Lines: A0 A1 A2 A3 A4 A5 A6 A7

Pin Numbers: 30 31 32 33 34 35 36 37

Logic State: 0 0 0 0 0 0 0 0

Address Lines: A8 A9 A10 A11 A12 A13 A14 A15

Pin Numbers: 38 39 41 1 2 3 4 5

Logic State: 0 0 0 0 0 0 0 0

Function: MREQ L

Pin Numbers: 19

Logic State: 1

Function: RD L

Pin Numbers: 21

Logic State: 1

Function: M1 L

Pin Numbers: 27

Logic State: 1

Function: REFSH L

Pin Numbers: 28

Logic State: 1

Data Lines: D0 D1 D2 D3 D4 D5 D6 D7

Pin Numbers: 14 15 12 8 7 9 10 13

Logic State: 1 0 1 0 1 1 1 1

4.12.4 Demonstration Program Screens

Figure 4-35

The following figures show the printed versions of the screens for the test program described above.

```

DESCRIBE          Name: Z80
1JULY.80
# of Pins = 40    # of Groups = 2

```

```

-----
Pin IDs : # ID S: # ID S: # ID S
I In    :-----:-----:-----
O Out   : 1 T  1:17 I  1:33 T  1
B Bidir: 2 T  1:18 O  1:34 T  1
T Trist: 3 T  1:19 T  1:35 T  1
G Gnd   : 4 T  1:20 T  1:36 T  1
X Don't: 5 T  1:21 T  1:37 T  1
Vi Pwr.i: 6 C1  :22 T  1:38 T  1
Clocks  : 7 T  1:23 T  1:39 T  1
C0       : 8 T  1:24 I  1:40 T  1
  1.00MHz: 9 T  1:25 I  1:
  1000ns :10 T  1:26 I  1:
Senc C1:11 V1  :27 O  1:
C1=C0/1 :12 T  1:28 O  1:
C2=C0/2 :13 T  1:29 G  :
C4=C0/4 :14 T  1:30 T  1:
C8=C0/8 :15 T  1:31 T  1:
CF=C0/16:16 I  1:32 T  1:
*****

```

SYSTEM RUN MODE

```

-----
Test Sequence: [CFP]
-----

```

```

          Bin1 Bin2 Bin3 Bin4 Bin5  0
          FP   FP   FP   FP   FP
G 1 : **                                     F
r 2 : **                                     A
o   :                                         I
u   :                                         L
p   :
s   :
-----

```

```

Functional: Step 0000 to End
          All Groups First Failure
          * All Groups
          Stop After Each Group
          Test Continuously to Failure
          Test Continuously
-----

```

```

Keyboard NOT Locked
*****

```

Figure 4-35a. Program screens for Z-80.

```

SYSTEM DISPLAY MODE      Pins: 1-8
                        9-16
                        17-24
* Pass/Fail/Bin         25-32
  Result Summary        33-40
  Parametric Results
*****

```

```

TEST STATISTICS
Comment:
-----

```

```

Reset:   Clock
         Counter      Times Reset
-----

```

```

REAL TIME CLOCK
Day 1 Month 1 Year
Hour   Minute
                00:36:28 01JAN00
-----

```

```

TOTAL TESTED: 00000006

```

```

TOTAL PASSED: 00000000
                Bin 1: 00000000
                Bin 2: 00000000
                Bin 3: 00000000
                Bin 4: 00000000
                Bin 5: 00000000

```

```

TOTAL FAILED: 00000006
*****

```

```

SYSTEM OUTPUT MODE
-----

```

```

ENABLE      SCREEN COPIES
  IEEE      Truth Table
* 20mA      * All Others
-----

```

```

RESULTS FORMAT:

```

```

  Pass/Fail/Bin      : Groups *1
  Results Summary    :      *2
* Parametric Results :
                    :
  Failures Only      :
                    :
                    :
                    :
-----

```

```

HANDLER:      Debounce:
* Off
  Stop on      Consecutive Fails
  Continue
*****

```

```

PARAMETERS Group 1 Z80
SUPPLIES Step 0067
  Voltage Test Limit I-max
V1= 5.25 V I1= 250. mA 350. mA
V2=          I2=
V3=          I3=

```

```

--- S1 ---Param---Func---
IIL 10.0uA @VIL 800.mV 500.mV
IIH 10.0uA @VIH 2.00 V 3.00 V
VOL 400.mV @IOL 1.80mA 1.80mA
VOH 2.40 V @IOH 250.uA 250.uA
IZL 250.uA @VZL 400.mV
IZH 250.uA @VZH 2.40 V

```

```

IOS @VDS
--- S2 ---Param---Func---
IIL @VIL
IIH @VIH
VOL @IOL
VOH @IOH
IZL @VZL
IZH @VZH
IOS @VDS

```

```

*****

```

```

PARAMETERS Group 2 Z80
SUPPLIES Step 0000
  Voltage Test Limit I-max
V1= 4.75 V I1= 150. mA 350. mA
V2=          I2=
V3=          I3=

```

```

--- S1 ---Param---Func---
IIL 10.0uA @VIL 800.mV 800.mV
IIH 10.0uA @VIH 2.00 V 2.00 V
VOL 400.mV @IOL 1.80mA 1.80mA
VOH 2.40 V @IOH 250.uA 250.uA
IZL 10.0uA @VZL 400.mV
IZH 10.0uA @VZH 2.40 V

```

```

IOS @VDS
--- S2 ---Param---Func---
IIL @VIL
IIH @VIH
VOL @IOL
VOH @IOH
IZL @VZL
IZH @VZH
IOS @VDS

```

```

*****

```

Figure 4-35b. Program screens for Z80.

```

ALT PARAM Group 1 Z80
Parm Step 0003 to End Parm Func
Voltage Test Limit K1 K1
V1= 5.25 V I1= 250.mA K2 K2
V2= I2= K3 K3
V3= I3= K4 K4

```

```

--- S1 ---Parm----Func--
IIL @VIL 800.mV 500.mV
IIH @VIH 2.00 V 3.00 V
VOL @IOL 1.80mA 1.80mA
VOH @IOH 250.uA 250.uA
IZL @VZL 400.mV
IZH @VZH 2.40 V
IOS @VOS

```

```

ALT PARAM Group 2 Z80
Parm Step 0003 to End Parm Func
Voltage Test Limit K1 K1
V1= 4.75 V I1= 150.mA K2 K2
V2= I2= K3 K3
V3= I3= K4 K4

```

```

--- S1 ---Parm----Func--
IIL @VIL 800.mV 800.mV
IIH @VIH 2.00 V 2.00 V
VOL @IOL 1.80mA 1.80mA
VOH @IOH 250.uA 250.uA
IZL @VZL 400.mV
IZH @VZH 2.40 V
IOS @VOS

```

```

--- S2 ---Parm----Func--
IIL @VIL
IIH @VIH
VOL @IOL
VOH @IOH
IZL @VZL
IZH @VZH

```

```

IOS @VOS
*****

```

```

GATE/STROBE Z80

```

```

Sync Clock TIMING
1.00MHz Unit Sec

```

```

I-----I-----I 0016 1.00u

```

```

G/S Set A
G: -----*----- 005 312.n
S: -----*----- 014 875.n

```

```

G/S Set B
G: -----*----- 005 312.n
S: -----*----- 014 875.n

```

```

Pin #: 0000000011111111122222
123456789012345678901234

```

```

GS Set: AAAAA BBBB BBBBBAAAAAAAAA

```

```

Pin #: 22222333333333334
5678901234567890

```

```

GS Set: AAAA AAAAAAAAAAAAA
*****

```

TRUTH TABLE Z80

```

Pin: 111111111122222222223333333334
:1234567890123456789012345678901234567890

```

```

Pin ID:TTTTCTTTTUTTTTTIOTTTTTIIIOGTTTTTTTTTTT

```

```

S 0000:XXXXXCXXXXVXXXXiiXXXXXXiiXXGXXXXXXXXXXXX
T 0001:XXXXXCXXXXVXXXXiiXXXXXXiiXXGXXXXXXXXXXXX
E :W 0006
P 0002:TTTTCTTTTUTTTTTiXXXXXXiiXXGTTTTTTTTTTTT
0003:TTTTCTTTTUTTTTTiXXXXXXiiXXGTTTTTTTTTTTT
0004:TTTTCTTTTUTTTTTiXXXXXXiiXXGTTTTTTTTTTTT
0005:00000CooooVooooii10101111101G000000000000
0006:00000CoiioViiiii10101111101G000000000000
0007:00000CoiioViiiii10111111110G000000000000
0008:00000CooooVooooii11111111110G000000000000
0009:00000CooooVooooii10101111101G100000000000
:
:

```

Figure 4-35c. Program screens for Z-80.

736

```
Pin:      1111111111222222222233333333334
:1234567890123456789012345678901234567890
```

File ID:TTTTTCTTTTTTTTIIOTTTTTIIIOGGTTTTTTTTTTTT

```

S 0010:00000CioioVooooiii101011111101G10000000000
T 0011:00000CioioVooooiii101111111110G10000000000
E 0012:00000CioioVooooiii111111111110G10000000000
F 0013:00000CooooVooooiii101011111111G10000000000
0014:00000CooooVooooiii10101111111G10000000000
0015:00000CooooVooooiii111111111111G10000000000
0016:00000CooioVooooiii101011111111G11000000000
0017:00000CooioVooooiii101011111111G11000000000
0018:00000CooioVooooiii111111111111G11000000000
0019:00100CooooVooooiii101111111111G00000000000
0020:00100C0000V0000iii101101111111G00000000000

```

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

TRUTH TABLE 290

```
Pin:      1111111111222222222233333333334
:1234567890123456789012345678901234567890
```

Fin ID:TTTTTCTTTTVTTTTIIIOTTTTTIIIOUGTTTTTTTTTTTT

```
S 0021:00100C0000V0000i111111111111G000000000000
T 0022:00000C0000V0000i1101011111101G001000000000
E 0023:00000C0000V0000i1101011111101G001000000000
F 0024:00000C0000V0000i110111111111G010000000000
0025:00000C0000V0000i111111111111G010000000000
0026:00000C0000V0000i110101111111G101000000000
0027:00000C0000V0000i110101111111G101000000000
0028:00000C0000V0000i111111111111G101000000000
0029:00000C0000V0000i110101111111G011000000000
0030:00000C0000V0000i110101111111G011000000000
0031:00000C0000V0000i110111111111G011000000000
:
```

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Figure 4-35d. Program screens for Z-80.

280

Pin ID:TTTTTCTTTTVTTTTIIOTTTTTIIIOOGTTTTTTTTTTTTT

```
S 0032:00000CooooVooooiii111111iii10G11000000000
T 0033:00000CooooVooooiii101011iii01G11100000000
E 0034:00000CioioVooooiii101011iii01G11100000000
F 0035:00000CioioVooooiii101111iii10G00100000000
0036:00000CooooVooooiii111111iii10G00100000000
0037:00000CooooVooooiii101011iii11G00010000000
0038:00000CoioVoioiii101011iii11G00010000000
0039:00000CoioVoioiii111111iii11G00010000000
0040:00000CooooVooooiii101111iii11G10010000000
0041:00000CoioVoioiii101011iii11G10010000000
0042:00000CoioVoioiii111111iii11G10010000000
```

780

Pin ID:TTTTTCTTTTUTTTTTIIOTTTTIIIOOGTTTTTTTTTTTT

```
S 0043:10101CooooVooooiii101111111111G0101010101010
T 0044:10101C1010V1010iii101101111111G0101010101010
E 0045:10101C1010V1010iii111111111111G0101010101010
P      :E
0046:
```

0046:

◆ ◆ ◆ ◆ ◆

◆◆

Figure 4-35e. Program screens for Z-80.

1732 DESCRIBE SCREEN WORKSHEET

A. Program name: _____

Type of device (if different from program name) or comment:

B. Number of pins per device: _____

Number of test groups per test program: _____

C. Clocks:

CO: _____ MHz (one of these fifteen values)	8.00	2.29	1.33
	5.33	2.00	1.23
	4.00	1.78	1.14
	3.20	1.60	1.07
	2.66	1.45	1.00

Sync: _____ C1 = CO/1	_____ C8 = CO/8
_____ C2 = CO/2	_____ CF = CO/16
_____ C4 = CO/4	_____ External

D. Pin assignments:

	ID	S	ID	S	ID	S

Definitions (for ID)	1.	_____	17.	_____	33.	_____
-----	2.	_____	18.	_____	34.	_____
I (1,2) = Input	3.	_____	19.	_____	35.	_____
O (1,2) = Output	4.	_____	20.	_____	36.	_____
B = Bidirectional	5.	_____	21.	_____	37.	_____
T = Tristate	6.	_____	22.	_____	38.	_____
X = Don't Care	7.	_____	23.	_____	39.	_____
V (1,2,3) = Power	8.	_____	24.	_____	40.	_____
G = Ground	9.	_____	25.	_____	41.	_____
C (1,2,3) = Clock	10.	_____	26.	_____	42.	_____
	11.	_____	27.	_____	43.	_____
	12.	_____	28.	_____	44.	_____
S = Pin Set	13.	_____	29.	_____	45.	_____
(Default is 1)	14.	_____	30.	_____	46.	_____
	15.	_____	31.	_____	47.	_____
	16.	_____	32.	_____	48.	_____

1732 RUN-MODE SCREEN WORKSHEET

A. Test Sequence: _____ (for example, CKFP, CP, F, CK)

		Bin 1		Bin 2		Bin 3		Bin 4		Bin 5	
		F	P	F	P	F	P	F	P	F	P
G	1	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
R	2	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
O	3	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
U	4	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
P	5	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
S	6	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____

Test Procedure

C. Functional Test: Step _____ to Step _____

- D. _____ All Groups First Failure
 _____ All Groups (use if binning is required)
 _____ Stop After Each Group
 _____ Test Continuously to Failure
 _____ Test Continuously

E. _____ Single Step

F. Keyboard IS/NOT Locked. (Password = up to 6 characters)

----- **1732 PARAMETERS SCREEN WORKSHEET** -----

Device Number (if different from program name) _____

Group _____ of _____ groups Program Name: _____

Power Supplies (1, 2, 3)

(A) Power Supplies tested at step _____

(B) Power Supply
 Shutdown Current
 I-max
 (for this group)

Voltage	Test Limit	
V1 = + _____ V	I1 = _____ mA	_____ mA
V2 = + _____ V	I2 = _____ mA	_____ mA
V3 = - _____ V	I3 = _____ mA	_____ mA

(C) ----- Pin Set 1 -----

Parametric Test Limits	----- Test Conditions -----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	_____ V
VOL = _____ V	@ IOL = _____ mA/uA	_____ mA/uA
VOH = _____ V	@ IOH = _____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

(D) ----- Pin Set 2 -----

Parametric Test Limits	----- Test Conditions -----	
	Parametric	Functional
IIL = _____ mA/uA	@ VIL = _____ V	_____ V
IIH = _____ mA/uA	@ VIH = _____ V	_____ V
VOL = _____ V	@ IOL = _____ mA/uA	_____ mA/uA
VOH = _____ V	@ IOH = _____ mA/uA	_____ mA/uA
IZL = _____ mA/uA	@ VZL = _____ V	
IZH = _____ mA/uA	@ VZH = _____ V	
IOS = _____ mA/uA(min)	_____ mA/uA(max) @ VOS = _____ V	

----- **1732 ALTERNATE PARAMETERS SCREEN WORKSHEET** -----

Device Number (if different from program name) _____

Group ____ of ____ groups Program Name: _____

(A) Range of steps within which
 to do all parametric tests:
 step ____ to step ____

(B) Close relays during:
 Parametric Functional

Voltage	Test Limit	_____ K1	_____ K1
V1 = +_xxxx_ V	I1 = _xxxx_ mA	_____ K2	_____ K2
V2 = +_xxxx_ V	I2 = _xxxx_ mA	_____ K3	_____ K3
V3 = -_xxxx_ V	I3 = _xxxx_ mA	_____ K4	_____ K4

(C) ----- Pin Set 1 -----

Parametric Test Limits	----- Test Conditions ----- Parametric Functional
IIL = _____ mA/uA	@ VIL = _xxxx_ V _xxxx_ V
IIH = _____ mA/uA	@ VIH = _xxxx_ V _xxxx_ V
VOL = _____ V	@ IOL = _xxxx_ mA/uA _xxxx_ mA/uA
VOH = _____ V	@ IOH = _xxxx_ mA/uA _xxxx_ mA/uA
IZL = _____ mA/uA	@ VZL = _xxxx_ V
IZH = _____ mA/uA	@ VZH = _xxxx_ V
IOS = _xxxx_ mA/uA(min)	_xxxx_ mA/uA(max) @ VOS = _xxxx_ V

(D) ----- Pin Set 2 -----

Parametric Test Limits	----- Test Conditions ----- Parametric Functional
IIL = _____ mA/uA	@ VIL = _xxxx_ V _xxxx_ V
IIH = _____ mA/uA	@ VIH = _xxxx_ V _xxxx_ V
VOL = _____ V	@ IOL = _xxxx_ mA/uA _xxxx_ mA/uA
VOH = _____ V	@ IOH = _xxxx_ mA/uA _xxxx_ mA/uA
IZL = _____ mA/uA	@ VZL = _xxxx_ V
IZH = _____ mA/uA	@ VZH = _xxxx_ V
IOS = _xxxx_ mA/uA(min)	_xxxx_ mA/uA(max) @ VOS = _xxxx_ V

xxxx represents a value determined on the parameters screen

Sheet _____ of _____

PROGRAM NAME: _____

[illegible]

System Extensions – Section 5

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5.1 INTRODUCTION

Figure 5-1

The 1732 test system alone provides the hardware and software tools for thorough, rapid testing of digital integrated circuits. Its interfaces provide further versatility by facilitating extension of its capabilities, so that (for example) production-line throughput can be increased. With a computer, an extended system can be assembled with the capability of selecting data to be recorded, analyzing it, or even changing test parameters automatically according to a sophisticated program. Basically, the test system can be expanded to include the peripherals shown in the accompanying figure.

Five major interface connectors are provided; refer to Table 1-2, in Section 1. Installation details are contained in Section 2. Briefly, the connectors and their applications are as follows:

HANDLER CONTROL. This connector is used to interface the control signals necessary to operate an automatic or manual handler. In addition, this interface can be used with a footswitch or other remote switch for "start".

IEEE-488. This connector provides input/output connections that conform to the IEEE Standard 488-1978. Practical application is for remotely programming and controlling the test system via a network from a remote station.

PORT I. Provides input/output for a serial device and

for an auxiliary display screen. Serial operation is internally switchable from 20-mA current loop to RS232 Standard interface via separate rear-panel connectors. Common serial devices are printers and teletypes, but system controllers are also included. For the recommended auxiliary display screens, refer to the table of available accessories in paragraph 1.4.

TAPE. This connector is used to interface to a peripheral tape drive for additional mass storage.

FOOTSWITCH. This connector receives the cable provided on footswitch 1732-9681 for remote "start" control. Refer to the table of accessories in paragraph 1.4.*

5.2 HANDLERS AND PROBES

Figure 5-2

5.2.1 General

The test system has been designed for easy interface to automatic and manual device handlers as well as wafer probe testers. The pin electronics module (PEM) can be mounted on or close to the handler while the program display unit can be located for convenience of the operator. For interfacing a handler to the system, there are three main interfaces to be considered, as follows:

- Handler control signals
- Measurement lines
- Handler mounting.

Handler control signals, identified in Section 2, are available at the HANDLER CONTROL connector at the rear of the program display unit. These are standard TTL logic signals, normally active low (negative true). Because of the wide variety of handlers and probes available, it may be necessary to condition these control signals. For 1732 systems with serial numbers beginning with letters before and including ... JE, JF, JG, an additional digital interface board may be required (installed in the top of the program display unit). This addition will not be required for systems that have all necessary interface capability built in, as scheduled for serial numbers beginning JR, JS, JT, ... If there is any doubt, especially for serial numbers between JG and JR, ask a service technician to look at the I/O No. 1 board. The old style is 1731-4740. The new 1731-4603 board is configurable by jumpers in the external cable; for details refer to the 1732-1819 handler interface manual, which is included in handler interface kits after about September, 1983, or to the 1731 service manual after about December, 1983.

Measurement lines that connect the test circuits to the socket adaptor and ultimately to the DUT must be extended from the pin electronics module and interfaced to the handler. This extension requires adaptors: one that replaces the socket adaptor mounts on the pin electronics module; one that mounts on the handler and contains the standard adaptor wiring such as the clock, ground, and supply jumpers; and short ribbon cables.

* Footswitch 1732-9680 connects to the HANDLER CONTROL connector; 1732-9681, to the FOOTSWITCH connector.

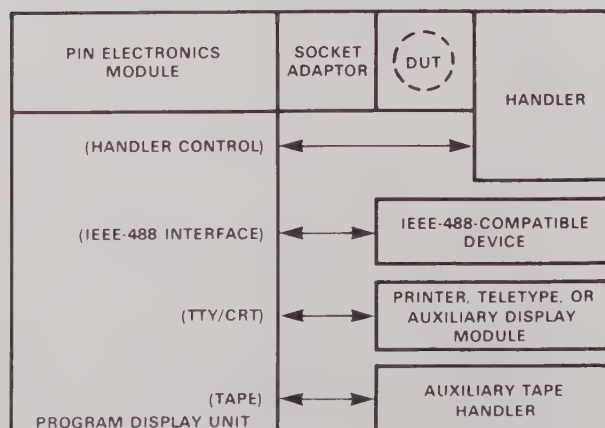


Figure 5-1. Extended system.

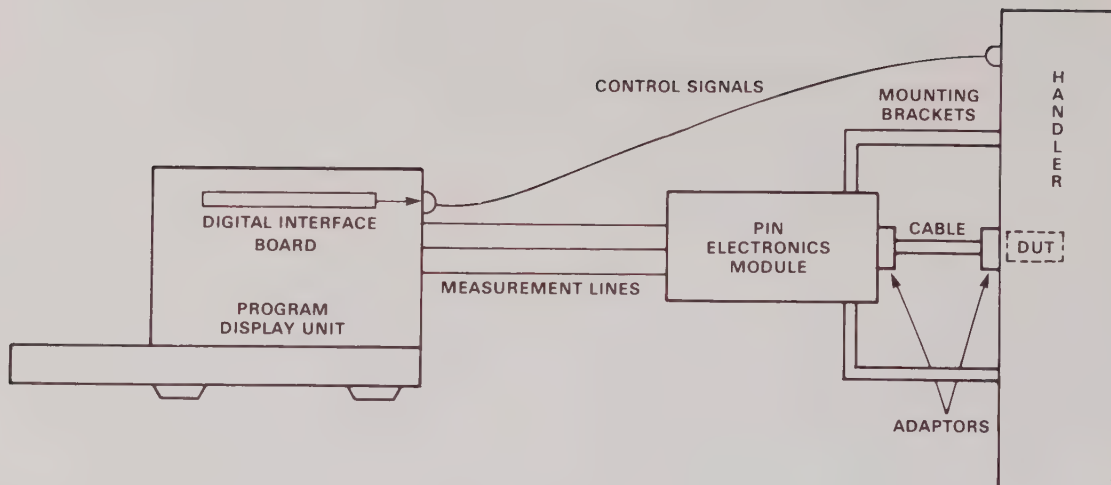


Figure 5-2. Handler interfacing.

The pin electronics module must be mechanically fixed to the handler to insure that vibrations will not affect continuity. Mounting design should take advantage of the four screw positions available on the module.

5.2.2 Interfaces Available from GenRad

GenRad will design and install handler interfaces for customers and strongly recommends that users take advantage of our expertise and experience. The benefits to the customer both in time and expense are worthwhile. Presently two options are available for each interface: an installation kit or a GenRad factory installation.

Interface kits for the more common handlers and probers are available from GenRad and special design kits for others will become available. Interface kits will be installed at the customer's plant by a service engineer. The customer's handler must be available and working at the time of installation.

Factory installed interfaces ensure system integration and verification on the day of delivery. However, the customer's handler must be shipped to GenRad prior to the installation.

5.2.3 Customer Designed Interfaces

Customers who want to design their own interfaces should follow "good practices" in their use of interface lines, i.e., use short lines and provide sufficient grounding. Interface circuits between the I/O No. 1 board and the handler should provide adequate drive and prevent spurious activity on the control signals lines.

5.2.4 Operation with a Handler or Prober

When operating with a handler and a typical device program, it is usually necessary to make certain minor adjustments as follows:

STOP ON n CONSECUTIVE FAILS or to CONTINUE

The operator must then load the test program. If the handler has a selection of modes, set it to "normal." The handler then asserts the RDY line, which functions as the test-system start command. When testing is completed, the test system asserts the DONE signal to notify the handler.

If the handler sends the RDY signal while a test is in progress (or if it sends a train of these signals due to contact bounce), the system will not respond. However, you can abort a test by pressing the START button on the system keyboard.

If the system halts because the specified number of consecutive failures does occur, you can restart testing by pressing the START button. After completion of one test, then, subsequent start signals will be accepted from the handler or foot switch.

5.3 MANUAL HANDLER

5.3.1 General

A manual handler assembly, 1732-9710 is available for use with the 1732 test system. The unit mounts onto the PEM module. Indicators on the manual handler show, after each test, the bin assignment for the DUT.

5.3.2 Mounting

The manual handler should be mounted to the PEM module by use of a single screw. Plug the interface cable, which is part of the manual handler assembly, into the rear panel at the connector labeled HANDLER CONTROL.

Empty IC tubes can be used as pass/fail bins and should be mounted on the handler by use of the fingers provided. The number of bins depends on the test program (see run-mode screen) and can include five "pass" and one "fail" categories. The fail bin is the one farthest to the right.

Notice that 2 fingers are provided for mounting each tube. Tubes with 0.762-cm (0.3-inch) and 1.016-cm (0.4-inch) spacing should be mounted on the left finger. Tubes with 1.524-cm (0.6-inch) spacing should be held in place using both fingers.

Run-mode Screen — set to ALL GROUPS
System-output-mode Screen — set HANDLER to



Figure 5-3. A command-address-data block.

5.3.3 Operation

When using the manual handler, set the run mode selection to ALL GROUPS. The display mode should be set up for the pass/fail indication. The handler selection on the output-mode screen should be set up either to STOP ON n CONSECUTIVE FAILS or to CONTINUE.

The manual-handler START button should be used to start testing. This button acts like the start signal for an automatic handler. (See Table 2-1, the RDY signal.) Following a test, the system automatically lights the indicator lamp on the manual handler, just above the bin where the DUT is to be placed. Pass bins 1 to 5 run from left to right, with the fail bin being the sixth (farthest right) bin.

Because the pass/fail mode is selected, the display screen indicates PASS or FAIL, and the assigned bin number. If STOP ON n CONSECUTIVE FAILS is selected, and the "stop" condition occurs, the screen displays the message: THE HANDLER HAS BEEN STOPPED AFTER n CONSECUTIVE FAILURES.

5.4 REMOTE PROGRAMMING

5.4.1 General

Figure 5-3

Operating Characteristics. The 1732 test system can transmit and receive data to and from peripheral devices (such as the CRT displays, printers, remote terminals, calculators, etc) through the IEEE-488 bus — if set up in the talk/listen mode*. Much of the operator/system dialog that normally takes place through the display screen and keyboard can be handled (generally with less convenience) through peripherals.

Local control (manual operation) is enabled in the IEEE-488 talk-only mode, in which this system is originally supplied, unless a "go to remote" command via the serial interface has established remote control. Local control is accomplished via the keyboard, with reference to displayed screens. Screen data selected in the output-mode screen can then be sent over the serial interface bus or (provided the system is in the talk-only mode) over the IEEE-488 bus.

Talk-only mode enables local control, all serial interface features, and output of data via the IEEE-488 bus to one or more compatible "listen only" devices, such as printers. The IEEE-488 handshake may constrain operation in some way. For example, a slow printer may limit measurement rate.

If internal switching is changed to enable IEEE-488 talk/listen mode, normal locally-controlled operation is possible provided also that the output-mode screen does NOT select the IEEE-488 bus for output and, of course, provided that a IEEE-488 controller has NOT issued a remote-enable command. (If talk/listen mode is enabled by internal switching but there is no IEEE-488 controller connected, control is local. However, the following situation is possible. If the IEEE-488 bus output is selected in the output-mode screen, the system will "hang up" during a test, i.e., testing will not proceed to completion because the test system is then programmed for a dialog with the missing controller. In this situation, press ABORT so that you can rectify the situation either by a change in the output-mode

screen or by connecting a suitable IEEE-488-bus controller and through it establishing remote control. See below.)

Remote control and programming of this test system via serial interface (20-mA loop) are generally possible in talk-only mode and conditionally possible if internal switching enables IEEE-488 talk/listen mode. This condition is that the IEEE-488-bus controller has NOT issued a remote-enable command. In either case, the serial device establishes remote control by issuing a "go to remote" command (see paragraph 5.4.2), which disables manual (keyboard) control.

Remote control and programming of this system via the IEEE-488 bus are generally possible only if internal switching enables the talk/listen mode and this mode is implemented with a suitable controller in an extended system. This controller establishes remote control by issuing a remote-enable command, which disables both serial-interface and manual control. (Refer to paragraph 2.6 and service-manual paragraph 2.9.) If the system was in serial-interface remote control when the IEEE-488 controller issues the remote-enable command, the latter controller sends the serial device a status message (see paragraph 5.4.5) and locks out both the serial device and the keyboard.

In a remote-control situation, all operations are controller-initiated by remote commands or device-dependent commands.

NOTE

When using the IEEE-488 bus, it is necessary to wait about one second between the go-to-remote command and any additional commands. This allows time for the system to process the command.

Records, Tfields, and Vfields. Data sent between devices on either of the above-mentioned interfaces are defined as records, each comprised of a Tfield followed by a Vfield; records are separated by delimiters. A record is a collection of adjacent data items treated as a unit; two or more records are considered a data block. The accompanying figure illustrates a typical block.

A Tfield contains a one-character code that defines the type of information (command, address, data, or status) that follows in the Vfield. The Tfield character usually implies the number of the Vfield data byte(s) and is always first in a record. The Tfield entries are listed in Table 5-1.

Table 5-1
TFIELD ENTRIES

Entry	Description
C	Command indicator
A	Index address
H	Memory address
M	Truth-table line address
B	Binary data (8 bits)
D	Double precision binary data (16 bits)
N	Floating point exponent data
P	Alphanumeric data
I	Alphanumeric data
G	Truth table data

* Refer to para. 2.6 for details, which include internal switch setting, cable connections, and key to interface signals.

A Vfield contains the actual "action" command or datum that is transferred via the interface. A Vfield contains a specific number of characters, depending on the preceding Tfield entry, for example:

- 1-character code for a command
- 2-character code for binary data
- 4-character code for hexadecimal data
- 10- to 12-character code for NR3 (numeric representation 3) data
- 32 ASCII-code characters for CRT line data (after a "P" Tfield).

Delimiters are characters that are used to mark the beginning or ending of a unit of data. There are two types of delimiters available for remote programming: a semicolon (;) which is used to delimit a record, and carriage return/line feed (designated {CR&LF}), which is used to delimit a block and the final record in that block.

5.4.2 Command Records

A command record consists of a "C" Tfield entry and one of 14 Vfield entries. (The Tfield entry must be followed by a Vfield character or the delimiter {CR&LF}; otherwise, an error message will result.) the "C" Tfield entry indicates that the character contained in the Vfield will be a data-manipulation command. The 14 Vfield entries are given in Table 5-2.

Table 5-2
VFIELD COMMAND ENTRIES

Command	Purpose
T	Send after test*
S	Send immediately*
L	Load data in
D	Delete truth-table line
G	Trigger
O	Continue test
B	Blank CRT display
E	Enable CRT
M	Do tape operation
W	Wide screen (64 characters)
N	Narrow screen (32 characters)
ETX	Reinitialization**

*See paragraph 5.4.9.

**The ETX command is a single ASCII character.

The T, S, L, and D Vfield characters require a command block (i.e., more than one record) for implementation, because send, load, and deletion commands require address and/or data records. All the other commands can be implemented with a command record.

5.4.3 Address Records

An address record consists of an A, H, or M Tfield entry followed by a four-bit value.

An "A" Tfield entry is followed by a hexadecimal value that represents the beginning of a system data field peculiar to test data. There are a total of 314 (013B hexadecimal) test data areas available in the system. Each address implies the type of information and the number of data words in the corresponding data field (alphanumeric, NR3, binary, etc.).

An "H" Tfield entry (reserved for GenRad service procedures) is followed by a hexadecimal number and indicates a hexadecimal address in the Z80 resident memory. Only binary data can be loaded by an H Tfield block and only 8 bits can be loaded at a time.

An "M" Tfield entry followed by a four-character decimal entry describes a decimal line address of the truth table. (See example under Data Records, below.) This address accepts only G Tfield entries, i.e., entries that are valid for a line of the truth table.

5.4.4 Data Records

A data record consists of any of six Tfield entries, B, D, N, P, I, or G followed by the data to be entered.

The "B" Tfield entry announces a binary data byte, which must be represented by two hexadecimal digits (before the delimiter).

The "D" Tfield entry indicates that the Vfield will contain a double-precision binary data byte, which must be represented by four hexadecimal digits before the delimiter.

The "N" Tfield entry indicates that the Vfield will contain 10-to-12 character numerical-representation-3 (NR3) data, a skip code, or an undefined code. The NR3 in the Vfield has this form: sign, mantissa, E, sign, exponent. The mantissa must have 6 digits and decimal point; the exponent, 2 digits. The signs can be omitted (default being +), for the minimum of 10 characters. If both signs are entered, there are 12 characters.

The skip code mentioned above is a single-character Vfield entry, either S or U. The S means "skip this data field and point the data-field pointer to the next data field to be filled." The U means "designate this data field as undefined and point to the next available data field."

The "P" Tfield entry indicates that the Vfield will contain CRT-line data, i.e., characters of a display-screen line. The accompanying Vfield must contain exactly 32 alphanumeric characters before the delimiters. (The delimiter {CR&LF} or a del entered before completion of the record results in a voided entry.) Notice that 32 characters fill the CRT line for the narrow display mode. However, 64 characters are required for the line for wide display mode, two "P" Tfield data records per line.

An "I" Tfield entry indicates that the Vfield will contain a comment, corresponding to the comment field of a particular test-program screen. The entry MUST be followed by the exact number of alphanumeric characters that will fill that particular comment field. Spaces can be used to satisfy this number requirement.

A "G" Tfield indicates that the data in the Vfield will be a truth-table entry, such as a pin functional test pattern entered in the same manner as it would be at the test-system keyboard. (Do not enter power, ground, etc., which are automatic entries.) Any illegal entry will result in an error message. Other valid truth-table entries (besides a functional test pattern) are:

- N start a new truth table.
- G (length) gray op-code and its length.
- P (length) psuedo op-code and its length.
- J (destination) (-) (repetition number) a jump instruction.
- W (delay) a wait and its delay count.
- S (destination) a sub-routine jump.
- R a return instruction to terminate a subroutine.
- E the end instruction.

It is important to enter 4 decimal characters for each length, destination, repetition number, and delay count. (See example below.) Note also that all the G-Tfield instructions are limited by the restrictions that apply to the corresponding keyboard entries.

An M-Tfield record and one G-Tfield record are typically associated in a block, to write a truth-table data line alone (or a truth-table command line). However, an alternative form of block can be entered, having two G-Tfield records to write both a data line and associated truth-table command line.

The following examples illustrate two alternative methods of remote programming to enter a certain logic pattern (zeros and ones) at line 20 of the truth table and to enter an associated jump command that calls for jumping 6 times back to line 17. In the examples, the DUT has 14 pins, with power at pin 1 and ground at pin 7. (Because those 2 pins cannot accommodate logic-state assignments, there are 12 logic states defined in the commands.) Example 1 shows two blocks, one to enter a data line and one to enter a truth-table command line. Example 2 shows how a single block with two G-Tfield records will accomplish the same purpose.

Example 1: M0020;G010101101010{CR&LF}
M0020;GJ0017-0006{CR&LF}

Example 2:
M0020;G010101101010;GJ0017-0006{CR&LF}

Reverse-video characters are generated by preceding them with an ASCII (OE) character.

5.4.5 Status Messages

There are no facilities for host-initiated test-system status transfers, because some operations are time related and interrupt handling could cause erroneous results. However, the test system can initiate its own status messages. For IEEE operating states, this is accomplished by an SRQ and serial poll. For 20-mA operation, the status will be sent with an X Tfield terminated with a {CR&LF}. Table 5-3 lists the status messages and their definitions. For example, a wrong character will result in the transfer of one of the following messages:

XE{CR+LF} (for 20 mA operation)
E{CR+LF} (for IEEE operation)

Table 5-3
1732 STATUS MESSAGES

Message	Definition
A	Wrong Tfield
B	Too fast to handle (20 mA indicates that some characters are lost)
D	Tape finished
E	Wrong character
H	Handler stopped
L	Wrong label
M	Not in remote
@	Need to talk

NOTE: All IEEE status messages (except @) have a value of 128 (decimal) added.

It is essential, when programming via an IEEE Bus Controller, to monitor the SRQ line. If an error occurs or the 1732 wants to talk to the controller (i.e. send data after test), the SRQ line is flagged by the 1732 and a status call is issued. If this status is not cleared by a serial-poll sequence, the 1732 hangs on any additional status calls (i.e. another error).

5.4.6 Programming Example

The following tabulation is an example of remote programming used to load data for testing a device. The example is for a 74LS161A and is based on the worksheets illustrated in paragraph 4.8. The example includes the describe-screen, parametric-screen (six groups), and run-mode-screen programming. The programming technique begins by explicitly indicating each entry, but, beginning at Parameter Group 2, implicit entries are used.

To program successfully, one must understand the basic format for remote programming and know the index addresses, the data format, and the options for each entry. For best understanding of this example, refer to the programming reference information contained below in paragraph 5.4, which illustrates the programmable-data screens (except truth table, which is described by example under Data Records, above). Each entry location in the screen is numbered. An accompanying table for each screen tabulates (for each entry location) the index address and associated data requirements.

Also notice the following points:

- All addresses are hexadecimal.
- Some addresses represent several entries in sequence.
- A few entries have the same address for several screens.
- Enter data in hexadecimal form, as in example, (not binary).
- All units are standard, i.e., volts, amperes, ohms, etc.
- I and P data must have spaces to fill out the length requirement.
- Use the S Vfield entry to skip entries within a sequence.
- Blank entries need not be specified.
- Beware: entry numbers are not always shown in the same up-down, or left-right order.

Entry #	Programming Statement*
---------	------------------------

```

1 CL;A00A8;I74LS161ΔΔΔΔ{CR&LF}
2 CL;A00A9;I1.OCT.1980AAAAAAAAAAAAAAAAAAAAAA{CR&LF}
3 CL;A00AA;B10{CR&LF}
4 CL;A00A2;B06{CR&LF}
5 CL;A00A3;B013{CR&LF}
6 CL;A00A4;B03{CR&LF}
7 CL;A00AB;IΔIΔΔΔ1{CR&LF}
10 CL;A00AE;IΔIΔΔΔ2{CR&LF}
13 CL;A00B1;IΔIΔΔΔ1{CR&LF}
16 CL;A00B4;IΔIΔΔΔ1{CR&LF}
19 CL;A00B7;IΔIΔΔΔ1{CR&LF}
22 CL;A00BA;IΔIΔΔΔ1{CR&LF}
25 CL;A00BD;IΔIΔΔΔ1{CR&LF}
28 CL;A00C0;IΔGΔΔΔ{CR&LF}
31 CL;A00C3;IΔIΔΔΔ2{CR&LF}
34 CL;A00C6;IΔIΔΔΔ2{CR&LF}
37 CL;A00C9;IΔOΔΔΔ1{CR&LF}
40 CL;A00CC;IΔOΔΔΔ1{CR&LF}
43 CL;A00CF;IΔOΔΔΔ1{CR&LF}
46 CL;A00D2;IΔOΔΔΔ1{CR&LF}
49 CL;A00D5;IΔOΔΔΔ1{CR&LF}
50 CL;A00D8;IΔVΔΔΔ1{CR&LF}

```

* Spaces are essential, as indicated by the symbol Δ .

PARAMETERS GROUP #1

Entry #	Programming Statement
1	CL;A0004;D0041{CR&LF}
2-4	CL;A0000;N + 5.25000E + 00;NS;NS{CR&LF}
5-7	CL;A0001;N + 3.25000E -02;NS;NS{CR&LF}
8-10	CL;A0002;N + 1.00000E -01;NS;NS{CR&LF}
11-17	CL;A0003;N + 4.00000E -04;N + 2.00000E -05;N + 4.00000 -01;N + 2.70000E + 00; NS;NS;N + 2.00000E -02{CR&LF}
18-23	CL;A000A;N + 4.00000E -01;N + 2.70000E + 00;NS;NS;NS;NS{CR&LF}
24-27	CL;A000C;N + 8.00000E -01;N + 2.00000E + 00;N + 4.00000E -03; N + 4.00000E -04{CR&LF}
28	CL;A0012;N + 1.00000E -01{CR&LF}
29	CL;A000F;N + 0.00000E + 00{CR&LF}
30-36	CL;A0007;N + 8.00000E -04;N + 4.00000E -05;N + 4.00000E -01;N + 2.70000E + 00; NS;NS;NS{CR&LF}
37-42	CL;A000B;N + 4.00000E -01;N + 2.70000E + 00;NS;NS;NS;NS{CR&LF}
43-46	CL;A0010;N + 8.00000E -01;N + 2.00000E + 00;N + 4.00000E -03; N + 4.00000E -04{CR&LF}

PARAMETERS GROUP #2

Entry #	Programming Statement
1	CL;A0018;D0000{CR&LF}
2	CL;A0014;N4.75000E00{CR&LF}
8	CL;A0016;N1.00000E-01{CR&LF}
11-14	CL;A0017;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
18-21	CL;A001C;NS;NS;N4.00000E-03;N4.00000E-04{CR&LF}
24-27	CL;A0020;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}
30-33	CL;A001B;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
43-46	CL;A0024;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}

PARAMETERS GROUP #3

Entry #	Programming Statement
1	CL;A002C;D0000{CR&LF}
2	CL;A002B;N4.75000E00{CR&LF}
8	CL;A002A;N1.00000E-03{CR&LF}
11-14	CL;A002B;NS;NS;N5.00000E-01;N2.70000E00{CR&LF}
18-20	CL;A0030;NS;NS;N8.00000E-03{CR&LF}
24-27	CL;A0034;N8.00000E-01;N2.00000E00;N8.00000E-03; N4.00000E-04{CR&LF}
30-33	CL;A002F;NS;NS;N5.00000E-01;N2.70000E00{CR&LF}
43-46	CL;A0038;N8.00000E-01;N2.00000E00;N8.00000E-03; N4.00000E-04{CR&LF}

PARAMETERS GROUP #4

Entry #	Programming Statement
1	CL;A0040;D0042{CR&LF}
2	CL;A003C;N5.25000E00{CR&F}
5	CL;A003D;N3.20000E-02{CR&LF}
8	CL;A003E;N1.00000E-01{CR&LF}
11-14	CL;A003F;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
24-27	CL;A0048;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}
30-33	CL;A0043;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
43-46	CL;A004C;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}

PARAMETERS GROUP #5

Entry #	Programming Statement
1	CL;A0054;D0043{CR&LF}
2	CL;A0050;N5.25000E00{CR&LF}
5	CL;A0051;N3.10000E-02{CR&LF}
8	CL;A0052;N1.00000E-01{CR&LF}
11-14	CL;A0053;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
24-27	CL;A005C;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}
30-33	CL;A0057;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
43-46	CL;A0060;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}

PARAMETERS GROUP #6

Entry #	Programming Statement
1	CL;A0068;D0044{CR&LF}
2	CL;A0064;N5.25000E00{CR&LF}
5	CL;A0065;N3.10000E-01{CR&LF}
8	CL;A0066;N1.00000E-02{CR&LF}
11-14	CL;A0067;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
24-27	CL;A0070;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}
30-33	CL;A006B;NS;NS;N4.00000E-01;N2.70000E00{CR&LF}
43-46	CL;A0074;N8.00000E-01;N2.00000E00;N4.00000E-03; N4.00000E-04{CR&LF}

RUN MODE SCREEN

Entry #	Programming Statement
1	CL;A0083;ICFP{CR&LF}
2	CL;A0084;B07{CR&LF}
3	CL;A0085;B1F{CR&LF}
12	CL;A008E;D0000{CR&LF}
13	CL;A008F;D000E{CR&LF}
14	CL;A0090;B01{CR&LF}
16	CL;A0092;B01{CR&LF}

5.4.7 Remote Programming For Tape Operation

Tape operation is controlled by input to one of three test system screens. Keyboard controlled operations consist of loading a program from tape, recording a program onto tape, listing, deleting, and restoring files, and compressing and formatting tapes. Remote programming can perform these same functions.

However, to use remote programming for tape operation, the operator (or computer) must load a tape-operation selection bit into a general address (0080), prior to entering the operation code. This entry will select one of the three tape operation screens, PROGRAM CALL, TAPE OPERATION, or PROGRAM RECORD. This instruction differs slightly from normal remote programming, which requires only the entry location address, whereas remote tape operation requires that the appropriate screen be called. The programmer must then enter address and data, and initiate the operation by use of the command record CM.

For example, to call a device test program named 7400, enter the following blocks:

```
CL;A0080;B00{CR&LF}
CL;A007B;7400AAAAAAAA{CR&LF}
CM{CR&LF}
```

5.4.8 Remote Programming Screen Data

Figures 5-4 through 5-32

The programming information contained below illustrates the programmable-data screens (except truth table, which is described by example under Data Records, above). Each entry location (data field) in the screen is numbered. An accompanying table for each screen tabulates (for each entry location) the index address and associated data requirements, which are essential for remote programming.

In the tables, the column headed "No. of Entries or Characters" gives two kinds of information. If the data type implies strictly numerical data, this column indicates the number of data entries, which must be separated by delimiters. If the data type (P or I) implies an alphanumeric string, this column indicates the number of such characters (including spaces) that are required.

The following screen layouts and accompanying Tables 5-4 through 5-30 of addresses and data for remote programming are arranged in this order:

- System setup
- Device-test programming
- Tape operation

5.4.9 Remote-Controlled Data Sending

When sending data from the 1732 test system to a remote location, be sure to enable the desired channel (either IEEE or 20-mA) on the output-mode screen (see Figure 5-11). Failing to do so will effectively disable the send command, S or T (see Table 5-2). However, if the channel is enabled but the "listening" device (for talk-only mode) or the controller (for talk/listen mode) is missing, the 1732 system will "hang up" as described in paragraph 5.4.1.

System Setup Screens and Tables

Table 5-4
RUN-MODE SCREEN ENTRIES (Compare Figure 5-4.)

#"	Index Address	Data Type	No. of Entries or Characters*	Entry Options
1	0083	I	3	'C' - Continuity 'F' - Functional 'P' - Parametric Any sequence or combination can be used. Any unused places must have spaces entered.
2	0084	B	1	Binning requirements. Five bins. BinFi is the functional bin requirement for Bini. BinPi is the parametric bin requirement for Bini. 0 = don't care. 1 = must pass this test group to be put into this bin.
3	0085	B	1	Same as #2#
4	0086	B	1	Same as #2#
5	0087	B	1	Same as #2#
6	0088	B	1	Same as #2#
7	0089	B	1	Same as #2#
8	008A	B	1	Same as #2#
9	008B	B	1	Same as #2#
10	008C	B	1	Same as #2#
11	008D	B	1	Same as #2#
12	008E	D	1	The Functional test is from the truth-table step STPFIR to step STPEND. If STPEND = 28XXH, then it means the last step in the truth table.
13	008F	D	1	Read #12# comment.
14	0090	B	1	Do-TEST Indicator. Value from 1 to 5. 1 = Do all groups until first failure 2 = All groups 3 = Stop after each group 4 = Test continuously until first failure. 5 = Test continuously.
15	0091	B	1	Single step function; 0 = Disable, 1 = Enable.
16	0092	B	1	1 = Keyboard unlocked, 0 = Keyboard locked.
17	0093	I	6*	Code word

*See comment in text.

```

*****
*SYSTEM RUN MODE                                     *
*-----*
*Test Sequence: [#1#]                                *
*-----*
*      Bin1 Bin2 Bin3 Bin4 Bin5 0*
*      FP  FP  FP  FP  FP  *
*G 1 | ##  ##  ##  ##  ##  F*
*r 2 | ##  ##  ##  ##  ##  A*
*o 3 | 23  45  67  89 1011 I*
*u 4 | ##  ##  ##  ##  ##  L*
*p 5 | ##  ##  ##  ##  ##  *
*s 6 | ##  ##  ##  ##  ##  *
*-----*
*Functional: Step #12# to#13#                         *
*####All Groups First Failure                         *
*####All Groups                                       *
*#14#Stop After Each Group                           *
*####Test Continuously to Failure*
*####Test Continuously                             *
*#15#Single Step Functional                           *
*-----*
*Keyboard#16#Locked #17#                             *
*****

```

Figure 5-4. Run-mode screen.

```

*****
*SYSTEM DISPLAY MODE          * *RESULT SUMMARY          xxxxxxxxxxxx*
*                             * *Group #1#                      *
*-----*                   * *Functional Failure at Step ##2# *
*#1#Pass/Fail/Bin           * *
*  RESult Summary           * *          C FP| C FP| C FP*
*  PARAMetric Results       * * *Pin #3# |-----*
*          Pins:##1-8       * * 1 #4# | 17 | 33 * or *
*          #2#9-16          * * 2 | 18 | 34 *
*          ###17-24         * * *IIL= | 3 | 19 | 35 *
*          ###25-32         * * * x.xxmA | 4 | 20 | 36 *
*          ###33-40         * * *IIH= | 5 | 21 | 37 *
*          ###41-48         * * * x.xxmA | 6 | 22 | 38 *
*                             * * *VOL= | 7 | 23 | 39 *
*                             * * * x.xx V | 8 | 24 | 40 *
*                             * * *VOH= | 9 | 25 | 41 *
*                             * * * x.xx V | 10 | 26 | 42 *
*                             * * *IZL= | 11 | 27 | 43 *
*                             * * * x.xxmA | 12 | 28 | 44 *
*                             * * *IZH= | 13 | 29 | 45 *
*                             * * * x.xxmA | 14 | 30 | 46 *
*                             * * *IOS= | 15 | 31 | 47 *
*                             * * * x.xxmA | 16 | 32 | 48 *
*****

```

Figure 5-5. Display-mode screen.

Figure 5-6. Result summary screen.

Table 5-5
DISPLAY-MODE SCREEN ENTRIES (Refer to Figure 5-5.)

##	Index Address	Data Type	No. of Entries or Characters	Entry Options														
1	0094	B	1	Results-display mode = 1 For Pass/fail/bin = 2 For Summary = 3 For Parametrics														
2	0095	B	1	Which pins to display on the parametrics screen <table><tr><td>Bit</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr><tr><td>Pin</td><td>1-8</td><td>9-16</td><td>17-24</td><td>25-32</td><td>33-40</td><td>41-48</td></tr></table>	Bit	0	1	2	3	4	5	Pin	1-8	9-16	17-24	25-32	33-40	41-48
Bit	0	1	2	3	4	5												
Pin	1-8	9-16	17-24	25-32	33-40	41-48												

Table 5-6
RESULT SUMMARY SCREEN ENTRIES (Refer to Figure 5-6.)

##	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	00E2	B	1	The present test group number.
2	00E6	D	1	Functional failure test for the present test group. Two-byte binary number, limited to 4 decimal digits of truth table.
3	00E1	B	1	Pins 1 - 48 (See describe-screen pin information.)

```

*****
*PARAMETER RESULTS      xxxxxxxxxxxx*
*Group x                *
*-----*
*Test|Pin xx|Pin xx|Pin xx|Pin xx*
*IIL | #1# |      |      |      *
*IIH | #2# |      |      |      *
*VOL | #3# |      |      |      *
*VOH | #4# |      |      |      *
*IZL | #5# |      |      |      *
*IZH | #6# |      |      |      *
*IOS | #7# |      |      |      *
*-----*
*Test|Pin xx|Pin xx|Pin xx|Pin xx*
*IIL |      |      |      |      *
*IIH |      |      | V2= |      *
*VOL |      |      | x.xx |      *
*VOH |      |      | I2= |      *
*IZL |      |      | x.xxm |      *
*IZH |      |      |      |      *
*IOS |      |      |      |      *
*-----*
*Push ENTER to view next Pins *
*****

```

Figure 5-7. Parameter results screen.

Table 5-7
PARAMETER RESULTS SCREEN ENTIRE (Refer to Figure 5-7.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	00E7	N	7	Pin 1, 1st Word
2				2nd Word
3				3rd Word
4				4th Word
5				5th Word
6				6th Word
7				7th Word
	00E8	N	7	Pin 2
	00E9	N	7	Pin 3
	00EA	N	7	Pin 4
	00EB	N	7	Pin 5
	00EC	N	7	Pin 6
	00ED	N	7	Pin 7
	00EE	N	7	Pin 8
	00EF	N	7	Pin 9
	00F0	N	7	Pin 10
	00F1	N	7	Pin 11
	00F2	N	7	Pin 12
	00F3	N	7	Pin 13
	00F4	N	7	Pin 14
	00F5	N	7	Pin 15
	00F6	N	7	Pin 16
	00F7	N	7	Pin 17
	00F8	N	7	Pin 18
	00F9	N	7	Pin 19
	00FA	N	7	Pin 20
	00FB	N	7	Pin 21
	00FC	N	7	Pin 22
	00FD	N	7	Pin 23
	00FE	N	7	Pin 24
	00FF	N	7	Pin 25
	0100	N	7	Pin 26
	0101	N	7	Pin 27
	0102	N	7	Pin 28
	0103	N	7	Pin 29
	0104	N	7	Pin 30
	0105	N	7	Pin 31
	0106	N	7	Pin 32
	0107	N	7	Pin 33
	0108	N	7	Pin 34
	0109	N	7	Pin 35
	010A	N	7	Pin 36
	010B	N	7	Pin 37
	010C	N	7	Pin 38
	010D	N	7	Pin 39
	010E	N	7	Pin 40
	010F	N	7	Pin 41
	0110	N	7	Pin 42
	0111	N	7	Pin 43
	0112	N	7	Pin 44
	0113	N	7	Pin 45
	0114	N	7	Pin 46
	0115	N	7	Pin 47
	0116	N	7	Pin 48

[illegible]

Figure 5-9. Fail screen.

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	00E2	B	1	The present test group number. Binning flag: 0 means "Do not display the bin information." Flag 1,2,3,4, or 5 means "Display the actual bin number." Flag 6 means "Display the bin-0 result."
2	00E5	B	1	

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	00E2	B	1	The present test group number.
2	00E3	I	3	The failure mode for this test group
				Byte: 1 2 3
				Value: C/blank F/blank P/blank

```

*****
*TEST STATISTICS*
*Comment:#15#*
*-----*
*Reset: % Clock*
* % Counter#14#Times Reset*
*-----*
*REAL TIME CLOCK*
*Day #1# Month #2# Year #3#*
*Hour #4# Minute #5#*
* hh:mm:ss ddMMyy*
*-----*
*
*TOTAL TESTED: #6#*
*
*TOTAL PASSED: #7#*
* Bin 1: #8#*
* Bin 2: #9#*
* Bin 3: #10#*
* Bin 4: #11#*
* Bin 5: #12#*
*
*TOTAL FAILED: #13#*
*****

```

Figure 5-10. Test statistics screen.

Table 5-10
TEST STATISTICS SCREEN ENTRIES (Refer to Figure 5-10.)

##	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	00DC	B	1	1 to 31
2	00DD	B	1	1 to 12
3	00DE	B	1	0 to 99
4	00DF	B	1	0 to 23
5	00E0	B	1	0 to 59
6	0146	D	2	1st Word - MSB 2nd Word - LSB
7	0147	D	2	
8	0148	D	2	
9	0149	D	2	
10	014A	D	2	
11	014B	D	2	
12	014C	D	2	
13	014D	D	2	
14	0145	B	1	
15	0144	I	32	

```

*****
*SYSTEM OUTPUT MODE*
*
*-----*
*ENABLE            SCREEN COPIES*
*#1#IEEE          #2#Truth Table*
*##20mA           ###All Others*
*
*-----*
*RESULTS FORMAT:
*
*###Pass/Fail/Bin |Groups###*
*#3#Results Summary |###*
*###Parametric Results |#5#*
* |###*
*#4#Failures Only |###*
* |###*
* |*
*-----*
*HANDLER:          #8#
*###Off
*#6#Stop on#7# Consecutive Fails*
*###Continue
*****

```

Figure 5-11. Output-mode screen.

Table 5-11
OUTPUT-MODE SCREEN ENTRIES (Refer to Figure 5-11.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0096	B	1	Output enable: Bit 0 = IEEE Bit 1 = 20 mA. If the bit = 0 then do not send; if it = 1 then send to the device. (Do not use.)
2	0097	—	—	
3	0098	B	1	Results format: 0 = ON, 1 = OFF. Bit 0: Pass/fail/bin, Bit 1: Results summary, Bit 2: Parametric results
4	0099	B	1	Failures only flag: 0 = OFF; 1 = ON BIT 0: Failures-only flag
5	009A	B	1	Output-test group flag: Bit = 0, don't send; Bit = 1, send Bit number: 0 1 2 3 4 5 Group: 1 2 3 4 5 6
6	009B	B	1	Handler flag: 1 = OFF, 2 = Stop on a number of failures, 3 = Continuous
7	009C	B	1	Number of consecutive failures Maximum number = 99.
8	0150	B	1	(Not used.)

```

*****
*SERIAL INTERFACE OPTIONS*
*-----*
*
*LINE TERMINATION:###CR/LF/Pad*
*      #1#CR/Pad*
*
*
*
*PAD CHARACTER:###NUL (00)*
*      #2#ETX (03)*
*      ###EOT (04)*
*      Number Transmitted = #3#*
*
*
*START CHARACTER:###CR/LF*
*      #4#keyboard:#5#*
*PARITY #6# ODD*
*      EVEN*
*      NO PARITY*
*
*
*****

```

Figure 5-12. Serial interface options screen.

Table 5-12
SERIAL INTERFACE OPTIONS ENTRIES (Refer to Figure 5-12.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	009D	B	1	Line termination character. 1 = CR/LF/pad, 2 = CR/pad
2	009E	B	1	Pad character: 1 = NUL (00) 2 = ETX (03), 3 = EOT (04)
3	009F	D	1	Number of padding characters to be sent, values from 0 to 256
4	00A0	B	1	Start character: 1 = CR/LF 2 = Special character (KEYCHAR)
5	00A1	B	1	Special character (binary ASCII)
6	0151	B	1	1 = Odd, 2 = Even, 3 = No parity

Programming Function Screens and Tables

```

*****
*DESCRIBE      Name:      #1#      *
*Comment:      #2#      *
* of Pins = #3# of Groups =#4#*
*
*-----*
*Pin IDs | # ID S | # ID S | # ID S*
*I In |-----|-----|-----*
*O Out | 1 #7# | 17 #23# | 33 #39#*
*B Bidir | 2 #8# | 18 #24# | 34 #40#*
*T Trist | 3 #9# | 19 #25# | 35 #41#*
*G Gnd | 4 #10# | 20 #26# | 36 #42#*
*X Don't | 5 #11# | 21 #27# | 37 #43#*
*Vi Pwr.i | 6 #12# | 22 #28# | 38 #44#*
*Clocks | 7 #13# | 23 #29# | 39 #45#*
*C0 | 8 #14# | 24 #30# | 40 #46#*
* #5# | 9 #15# | 25 #31# | 41 #47#*
* | 10 #16# | 26 #32# | 42 #48#*
*Sync #6# | 11 #17# | 27 #33# | 43 #49#*
*C1=C0/1 | 12 #18# | 28 #34# | 44 #50#*
*C2=C0/2 | 13 #19# | 29 #35# | 45 #51#*
*C4=C0/4 | 14 #20# | 30 #36# | 46 #52#*
*C8=C0/8 | 15 #21# | 31 #37# | 47 #53#*
*CF=C0/16 | 16 #22# | 32 #38# | 48 #54#*
*****

```

Figure 5-13. Describe screen.

Table 5-13
DESCRIBE SCREEN ENTRIES (Refer to Figure 5-13.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	00A8	I	12	
2	00A9	I	32	
3	00AA	B	1	Binary 1-48
4	00A2	B	1	Binary 1-6 (See also Table 5-30.)
5	00A3	B	1	Binary 1 - 1 MHz Binary 2 - 1.07 MHz " 3 - 1.14 MHz " 4 - 1.23 MHz " 5 - 1.33 MHz " 6 - 1.45 MHz " 7 - 1.60 MHz " 8 - 1.78 MHz " 9 - 2.00 MHz " 10 - 2.29 MHz " 11 - 2.66 MHz " 12 - 3.2 MHz " 13 - 4.0 MHz " 14 - 5.33 MHz " 15 - 8.00 MHz
6	00A4	B	1	Binary 1 - C1 " 2 - C2 " 3 - C4 " 4 - C8 " 5 - CF " 6 - EXT

Table 5-13 (Continued)
DESCRIBE SCREEN ENTRIES

###	Index Address	Data Type	No. of Entries or Characters	Entry Options
7	00AB	I	6	ABCDEF A - Continuity pass/fail indicator: (20H - space key) is a pass, (AOH) is a fail. B - Pin types 'I' - Input 'O' - Output 'B' - Bidirectional 'T' - Tristate 'G' - Ground 'X' - Don't care 'Vi' - Power 'Ci' - Clock C - If Vi or Ci chosen then enter 1,2,3 for the voltage group of 0,1,2,4,8,F for the clock. D - Function pass/fail indicator (20H - space) - Pass (AOH) - Fail E - Parametric pass/fail indicator (Same entries as A and D) F - Pin group 1 or 2
8-54 (See below.)				Same as #7#

###	Index Address	###	Index Address
8	00AC	32	00C4
9	00AD	33	00C5
10	00AE	34	00C6
11	00AF	35	00C7
12	00B0	36	00C8
13	00B1	37	00C9
14	00B2	38	00CA
15	00B3	39	00CB
16	00B4	40	00CC
17	00B5	41	00CD
18	00B6	42	00CE
19	00B7	43	00CF
20	00B8	44	00D0
21	00B9	45	00D1
22	00BA	46	00D2
23	00BB	47	00D3
24	00BC	48	00D4
25	00BD	49	00D5
26	00BE	50	00D6
27	00BF	51	00D7
28	00C0	52	00D8
29	00C1	53	00D9
30	00C2	54	00DA
31	00C3		

Table 5-14
PARAMETERS SCREEN ENTRIES (Compare Figure 5-14.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0004	D	1	
2	0000	N	3	1st Word, V1
3				2nd Word, V2
4				3rd Word, V3
5	0001	N	3	1st Word, I1
6				2nd Word, I2
7				3rd Word, I3
8	0002	N	3	1st Word, IMAX V1
9				2nd Word, IMAX V2
10				3rd Word, IMAX V3
11	0003	N	7	1st Word
12				2nd Word
13				3rd Word
14				4th Word
15				5th Word
16				6th Word
17				7th Word
18	000A	N	6	1st Word
19				2nd Word
20				3rd Word
21				4th Word
22				5th Word
23				6th Word
24	000C	N	4	1st Word
25				2nd Word
26				3rd Word
27				4th Word
28	0012	N	1	
29	000F	N	1	
30	0007	N	7	1st Word
31				2nd Word
32				3rd Word
33				4th Word
34				5th Word
35				6th Word
36				7th Word
37	000B	N	6	1st Word
38				2nd Word
39				3rd Word
40				4th Word
41				5th Word
42				6th Word
43	0010	N	4	1st Word
44				2nd Word
45				3rd Word
46				4th Word
47	0013	N	1	
48	0011	N	1	

```

*****
*PARAMETERS Group 1 xxxxxxxxxxxxx*
*SUPPLIES Step #1#
* Voltage Test Limit I-max *
*V1= #2# I1= #5# #8# *
*V2= #3# I2= #6# #9# *
*V3= #4# I3= #7# #10# *
*--- S1 -----Parm-----Func---*
*IIL #11# @VIL #18# #24# *
*IIH #12# @VIH #19# #25# *
*VOL #13# @IOL #20# #26# *
*VOH #14# @IOH #21# #27# *
*IZL #15# @VZL #22# *
*IZH #16# @VZH #23# *
*IOS #17# #28# @VOS #29# *
*--- S2 -----Parm-----Func---*
*IIL #30# @VIL #37# #43# *
*IIH #31# @VIH #38# #44# *
*VOL #32# @IOL #39# #45# *
*VOH #33# @IOH #40# #46# *
*IZL #34# @VZL #41# *
*IZH #35# @VZH #42# *
*IOS #36# #47# @VOS #48# *
*****

```

Figure 5-14. Parameters screen.

```

*****
*ALT PARAM Group 1 xxxxxxxxxxxx*
*Parm Step #1# to #2# Parm Func *
* Voltage Test Limit ### ***
*V1=+x.xx V I1= x.xxmA #3# #4#
*V2=+x.xx V I2= x.xxmA ### ***
*V3=-x.xx V I3= x.xxmA ### ***
*--- S1 -----Parm-----Func---*
*IIL # 5# @VIL+X.XX V +X.XX V*
*IIH # 6# @VIH+X.XX V +X.XX V*
*VOL # 7# @IOL X.XXmA X.XXmA*
*VOH # 8# @IOH X.XXmA X.XXmA*
*IZL # 9# @VZL+X.XX V *
*IZH #10# @VZH+X.XX V *
*IOS #11# X.XXmA @VOS+X.XX V*
*--- S2 -----Parm-----Func---*
*IIL #12# @VIL+X.XX V +X.XX V*
*IIH #13# @VIH+X.XX V +X.XX V*
*VOL #14# @IOL X.XXmA X.XXmA*
*VOH #15# @IOH X.XXmA X.XXmA*
*IZL #16# @VZL+X.XX V *
*IZH #17# @VZH+X.XX V *
*IOS #18# X.XXmA @VOS+X.XX V*
*****

```

Figure 5-15. Alternate parameters screen, group 1.

Table 5-15
ALTERNATE PARAMETERS SCREEN ENTRIES, GROUP 1 (Refer to Figure 5-15.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	000D	D	1	
2	000E	D	1	
3	0006	B	1	Parametric relays Bit 1,2,3,4 imply relays 1,2,3,4. If the bit = 0, then the relay is not activated. If the bit = 1, then the relay is activated.
4	0005	B	1	Functional relays
5	0008	N	7	1st Word
6				2nd Word
7				3rd Word
8				4th Word
9				5th Word
10				6th Word
11				7th Word
12	0009	N	7	1st Word
13				2nd Word
14				3rd Word
15				4th Word
16				5th Word
17				6th Word
18				7th Word

Table 5-16
PARAMETERS SCREEN ENTRIES, GROUP 2 (Refer to Figure 5-16.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0018	D	1	
2	0014	N	3	1st Word, V1
3				2nd Word, V2
4				3rd Word, V3
5	0015	N	3	1st Word, I1
6				2nd Word, I2
7				3rd Word, I3
8	0016	N	3	1st Word, IMAX V1
9				2nd Word, IMAX V2
10				3rd Word, IMAX V3
11	0017	N	7	1st Word
12				2nd Word
13				3rd Word
14				4th Word
15				5th Word
16				6th Word
17				7th Word
18	001C	N	6	1st Word
19				2nd Word
20				3rd Word
21				4th Word
22				5th Word
23				6th Word
24	0020	N	4	1st Word
25				2nd Word
26				3rd Word
27				4th Word
28	0026	N	1	
29	0021	N	1	
30	001B	N	7	1st Word
31				2nd Word
32				3rd Word
33				4th Word
34				5th Word
35				6th Word
36				7th Word
37	001D	N	6	1st Word
38				2nd Word
39				3rd Word
40				4th Word
41				5th Word
42				6th Word
43	0024	N	4	1st Word
44				2nd Word
45				3rd Word
46				4th Word
47	0027	N	1	
48	0025	N	1	

```

*****
*PARAMETERS Group 2  xxxxxxxxxxxxxx*
*SUPPLIES Step #1#          *
* Voltage Test Limit I-max *
*v1= #2# I1= #5# #8# *
*v2= #3# I2= #6# #9# *
*v3= #4# I3= #7# #10# *
*--- S1 -----Parm-----Func---*
*IIL #11# @VIL #18# #24# *
*IIH #12# @VIH #19# #25# *
*VOL #13# @IOL #20# #26# *
*VOH #14# @IOH #21# #27# *
*IZL #15# @VZL #22#      *
*IZH #16# @VZH #23#      *
*IOS #17# #28# @VOS #29# *
*--- S2 -----Parm-----Func---*
*IIL #30# @VIL #37# #43# *
*IIH #31# @VIH #38# #44# *
*VOL #32# @IOL #39# #45# *
*VOH #33# @IOH #40# #46# *
*IZL #34# @VZL #41#      *
*IZH #35# @VZH #42#      *
*IOS #36# #47# @VOS #48# *
*****

```

Figure 5-16. Parameters screen, group 2.

```

*****
*ALT PARAM Group 2 xxxxxxxxxxxx*
*Parm Step #1# to #2# Parm Func *
* Voltage Test Limit ### ###*
*V1=+x.xx V I1= x.xxmA #3# #4#*
*V2=+x.xx V I2= x.xxmA ### ###*
*V3=-x.xx V I3= x.xxmA ### ###*
*--- S1 -----Parm----Func--*
*IIL # 5# @VIL+X.XX V +X.XX V*
*IIH # 6# @VIH+X.XX V +X.XX V*
*VOL # 7# @IOL X.XXmA X.XXmA*
*VOH # 8# @IOH X.XXmA X.XXmA*
*IZL # 9# @VZL+X.XX V *
*IZH #10# @VZH+X.XX V *
*IOS #11# X.XXmA @VOS+X.XX V*
*--- S2 -----Parm----Func--*
*IIL #12# @VIL+X.XX V +X.XX V*
*IIH #13# @VIH+X.XX V +X.XX V*
*VOL #14# @IOL X.XXmA X.XXmA*
*VOH #15# @IOH X.XXmA X.XXmA*
*IZL #16# @VZL+X.XX V *
*IZH #17# @VZH+X.XX V *
*IOS #18# X.XXmA @VOS+X.XX V*
*****

```

Figure 5-17. Alternate parameters screen, group 2.

Table 5-17
ALTERNATE PARAMETERS SCREEN ENTRIES, GROUP 2 (Refer to Figure 5-17.)

##	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0022	D	1	
2	0023	D	1	
3	001A	B	1	Parametric relays Bit 1,2,3,4 imply relays 1,2,3,4. If the bit = 0, then the relay is not activated. If the bit = 1, the relay is activated.
4	0019	B	1	Functional relays
5	001E	N	7	1st Word
6				2nd Word
7				3rd Word
8				4th Word
9				5th Word
10				6th Word
11				7th Word
12	001F	N	7	1st Word
13				2nd Word
14				3rd Word
15				4th Word
16				5th Word
17				6th Word
18				7th Word

Table 5-18

PARAMETERS SCREEN ENTRIES GROUP 3 (Refer to Figure 5-18.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	002C	D	1	
2	0028	N	3	1st Word, V1
3				2nd Word, V2
4				3rd Word, V3
5	0029	N	3	1st Word, I1
6				2nd Word, I2
7				3rd Word, I3
8	002A	N	3	1st Word, IMAX V1
9				2nd Word, IMAX V2
10				3rd Word, IMAX V3
11	002B	N	7	1st Word
12				2nd Word
13				3rd Word
14				4th Word
15				5th Word
16				6th Word
17				7th Word
18	0030	N	6	1st Word
19				2nd Word
20				3rd Word
21				4th Word
22				5th Word
23				6th Word
24	0034	N	4	1st Word
25				2nd Word
26				3rd Word
27				4th Word
28	003A	N	1	
29	0035	N	1	
30	002F	N	7	1st Word
31				2nd Word
32				3rd Word
33				4th Word
34				5th Word
35				6th Word
36				7th Word
37	0031	N	6	1st Word
38				2nd Word
39				3rd Word
40				4th Word
41				5th Word
42				6th Word
43	0038	N	4	1st Word
44				2nd Word
45				3rd Word
46				4th Word
47	003B	N	1	
48	0039	N	1	

```

*****
*PARAMETERS Group 3 xxxxxxxxxxxxxx*
*SUPPLIES Step #1# *
* Voltage Test Limit I-max *
*V1= #2# I1= #5# #8# *
*V2= #3# I2= #6# #9# *
*V3= #4# I3= #7# #10# *
*--- S1 -----Parm-----Func---*
*IIL #11# @VIL #18# #24# *
*IIH #12# @VIH #19# #25# *
*VOL #13# @IOL #20# #26# *
*VOH #14# @IOH #21# #27# *
*IZL #15# @VZL #22# *
*IZH #16# @VZH #23# *
*IOS #17# #28# @VOS #29# *
*--- S2 -----Parm-----Func---*
*IIL #30# @VIL #37# #43# *
*IIH #31# @VIH #38# #44# *
*VOL #32# @IOL #39# #45# *
*VOH #33# @IOH #40# #46# *
*IZL #34# @VZL #41# *
*IZH #35# @VZH #42# *
*IOS #36# #47# @VOS #48# *
*****

```

Figure 5-18. Parameters screen, group 3.

```

*****
*ALT PARAM Group 3 xxxxxxxxxxxx*
*Parm Step #1# to #2# Parm Func *
* Voltage Test Limit ### ###*
*V1=+x.xx V I1= x.xxmA #3# #4#*
*V2=+x.xx V I2= x.xxmA ### ###*
*V3=-x.xx V I3= x.xxmA ### ###*
*--- S1 -----Parm-----Func---*
*IIL # 5# @VIL+X.XX V +X.XX V*
*IIH # 6# @VIH+X.XX V +X.XX V*
*VOL # 7# @IOL X.XXmA X.XXmA*
*VOH # 8# @IOH X.XXmA X.XXmA*
*IZL # 9# @VZL+X.XX V *
*IZH #10# @VZH+X.XX V *
*IOS #11# X.XXmA @VOS+X.XX V*
*--- S2 -----Parm-----Func---*
*IIL #12# @VIL+X.XX V +X.XX V*
*IIH #13# @VIH+X.XX V +X.XX V*
*VOL #14# @IOL X.XXmA X.XXmA*
*VOH #15# @IOH X.XXmA X.XXmA*
*IZL #16# @VZL+X.XX V *
*IZH #17# @VZH+X.XX V *
*IOS #18# X.XXmA @VOS+X.XX V*
*****

```

Figure 5-19. Alternate parameters screen, group 3.

Table 5-19
ALTERNATE PARAMETERS SCREEN ENTRIES, GROUP 3 (Refer to Figure 5-19.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0036	D	1	
2	0037	D	1	
3	002E	B	1	Parametric relays. Bit 1,2,3,4 imply relays 1,2,3,4. If the bit = 0, then the relay is not activated. If the bit = 1, then the relay is activated.
4	002D	B	1	Functional relays
5	0032	N	7	1st Word
6				2nd Word
7				3rd Word
8				4th Word
9	0033	N	7	5th Word
10				6th Word
11				7th Word
12				1st Word
13				2nd Word
14				3rd Word
15				4th Word
16				5th Word
17				6th Word
18				7th Word

Table 5-20
PARAMETERS SCREEN ENTRIES, GROUP 4 (Refer to Figure 5-20.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0040	D	1	
2	003C	N	3	1st Word, V1
3				2nd Word, V2
4				3rd Word, V3
5	003D	N	3	1st Word, I1
6				2nd Word, I2
7				3rd Word, I3
8	003E	N	3	1st Word, IMAX V1
9				2nd Word, IMAX V2
10				3rd Word, IMAX V3
11	003F	N	7	1st Word
12				2nd Word
13				3rd Word
14				4th Word
15				5th Word
16				6th Word
17	0044	N	6	7th Word
18				1st Word
19				2nd Word
20				3rd Word
21				4th Word
22				5th Word
23	0048	N	4	6th Word
24				1st Word
25				2nd Word
26				3rd Word
27				4th Word
28	004E	N	1	
29	0049	N	1	
30	0043	N	7	1st Word
31				2nd Word
32				3rd Word
33				4th Word
34				5th Word
35				6th Word
36				7th Word
37				1st Word
38				2nd Word
39	0045	N	6	3rd Word
40				4th Word
41				5th Word
42				6th Word
43				1st Word
44				2nd Word
45				3rd Word
46				4th Word
47	004F	N	1	
48	004D	N	1	

```

*****
*PARAMETERS Group 4 xxxxxxxxxxxx*
*SUPPLIES Step #1# *
* Voltage Test Limit I-max *
*v1= #2# I1= #5# #8# *
*v2= #3# I2= #6# #9# *
*v3= #4# I3= #7# #10# *
*--- S1 -----Parm-----Func---*
*IIL #11# @VIL #18# #24# *
*IIH #12# @VIH #19# #25# *
*VOL #13# @IOL #20# #26# *
*VOH #14# @IOH #21# #27# *
*IZL #15# @VZL #22# *
*IZH #16# @VZH #23# *
*IOS #17# #28# @VOS #29# *
*--- S2 -----Parm-----Func---*
*IIL #30# @VIL #37# #43# *
*IIH #31# @VIH #38# #44# *
*VOL #32# @IOL #39# #45# *
*VOH #33# @IOH #40# #46# *
*IZL #34# @VZL #41# *
*IZH #35# @VZH #42# *
*IOS #36# #47# @VOS #48# *
*****

```

Figure 5-20. Parameters screen, group 4.

```

*****
*ALT PARAM Group 4 xxxxxxxxxxxx*
*Parm Step #1# to #2# Parm Func *
* Voltage Test Limit ### ***
*V1=+x.xx V I1= x.xxmA #3# #4#*
*V2=+x.xx V I2= x.xxmA ### ***
*V3=-x.xx V I3= x.xxmA ### ***
*--- S1 -----Parm-----Func--*
*IIL # 5# @VIL+X.XX V +X.XX V*
*IIH # 6# @VIH+X.XX V +X.XX V*
*VOL # 7# @IOL X.XXmA X.XXmA*
*VOH # 8# @IOH X.XXmA X.XXmA*
*IZL # 9# @VZL+X.XX V *
*IZH #10# @VZH+X.XX V *
*IOS #11# X.XXmA @VOS+X.XX V*
*--- S2 -----Parm-----Func--*
*IIL #12# @VIL+X.XX V +X.XX V*
*IIH #13# @VIH+X.XX V +X.XX V*
*VOL #14# @IOL X.XXmA X.XXmA*
*VOH #15# @IOH X.XXmA X.XXmA*
*IZL #16# @VZL+X.XX V *
*IZH #17# @VZH+X.XX V *
*IOS #18# X.XXmA @VOS+X.XX V*
*****

```

Figure 5-21. Alternate parameters screen, group 4.

Table 5-21
ALTERNATE PARAMETERS SCREEN ENTRIES, GROUP 4 (Refer to Figure 5-21.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	004A	D	1	
2	004B	D	1	
3	0042	B	1	Parametric relays. Bit 1,2,3,4 imply relays 1,2,3,4. If the bit = 0, then the relay is not activated. If the bit = 1, then the relay is activated.
4	0041	B	1	Functional relays.
5	0046	N	7	1st Word
6				2nd Word
7				3rd Word
8				4th Word
9				5th Word
10				6th Word
11				7th Word
12	0047	N	7	1st Word
13				2nd Word
14				3rd Word
15				4th Word
16				5th Word
17				6th Word
18				7th Word

Table 5-22

PARAMETERS SCREEN ENTRIES, GROUP 5 (Refer to Figure 5-22.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0054	D	1	
2	0050	N	3	1st Word, V1
3				2nd Word, V2
4				3rd Word, V3
5	0051	N	3	1st Word, I1
6				2nd Word, I2
7				3rd Word, I3
8	0052	N	3	1st Word, IMAX V1
9				2nd Word, IMAX V2
10				3rd Word, IMAX V3
11	0053	N	7	1st Word
12				2nd Word
13				3rd Word
14				4th Word
15				5th Word
16				6th Word
17				7th Word
18	0058	N	6	1st Word
19				2nd Word
20				3rd Word
21				4th Word
22				5th Word
23				6th Word
24	005C	N	4	1st Word
25				2nd Word
26				3rd Word
27				4th Word
28	0062	N	1	
29	005D	N	1	
30	0057	N	7	1st Word
31				2nd Word
32				3rd Word
33				4th Word
34				5th Word
35				6th Word
36				7th Word
37	0059	N	6	1st Word
38				2nd Word
39				3rd Word
40				4th Word
41				5th Word
42				6th Word
43	0060	N	4	1st Word
44				2nd Word
45				3rd Word
46				4th Word
47	0063	N	1	
48	0061	N	1	

```

*****
*PARAMETERS Group 5  xxxxxxxxxxxxxx*
*SUPPLIES Step #1#
* Voltage Test Limit I-max *
*V1= #2# I1= #5# #8# *
*V2= #3# I2= #6# #9# *
*V3= #4# I3= #7# #10# *
*--- S1 -----Parm-----Func---*
*IIL #11# @VIL #18# #24# *
*IIH #12# @VIH #19# #25# *
*VOL #13# @IOL #20# #26# *
*VOH #14# @IOH #21# #27# *
*IZL #15# @VZL #22# *
*IZH #16# @VZH #23# *
*IOS #17# #28# @VOS #29# *
*--- S2 -----Parm-----Func---*
*IIL #30# @VIL #37# #43# *
*IIH #31# @VIH #38# #44# *
*VOL #32# @IOL #39# #45# *
*VOH #33# @IOH #40# #46# *
*IZL #34# @VZL #41# *
*IZH #35# @VZH #42# *
*IOS #36# #47# @VOS #48# *
*****

```

Figure 5-22. Parameters screen, group 5.

```

*****
*ALT PARAM Group 5 xxxxxxxxxxxxx*
*Parm Step #1# to #2# Parm Func *
* Voltage Test Limit ### ###*
*V1=+x.xx V I1= x.xxmA #3# #4#*
*V2=+x.xx V I2= x.xxmA ### ###*
*V3=-x.xx V I3= x.xxmA ### ###*
*--- S1 -----Parm-----Func---*
*IIL # 5# @VIL+X.XX V +X.XX V*
*IIH # 6# @VIH+X.XX V +X.XX V*
*VOL # 7# @IOL X.XXmA X.XXmA*
*VOH # 8# @IOH X.XXmA X.XXmA*
*IZL # 9# @VZL+X.XX V *
*IZH #10# @VZH+X.XX V *
*IOS #11# X.XXmA @VOS+X.XX V*
*--- S2 -----Parm-----Func---*
*IIL #12# @VIL+X.XX V +X.XX V*
*IIH #13# @VIH+X.XX V +X.XX V*
*VOL #14# @IOL X.XXmA X.XXmA*
*VOH #15# @IOH X.XXmA X.XXmA*
*IZL #16# @VZL+X.XX V *
*IZH #17# @VZH+X.XX V *
*IOS #18# X.XXmA @VOS+X.XX V*
*****

```

Figure 5-23. Alternate parameters screen, group 5.

Table 5-23
ALTERNATE PARAMETERS SCREEN ENTRIES, GROUP 5 (Refer to Figure 5-23.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	005E	D	1	
2	005F	D	1	
3	0056	B	1	Parametric relays. Bit 1,2,3,4 imply relays 1,2,3,4. if the bit = 0, then the relay is activated. If the bit = 1, then the relay is not activated.
4	0055	B	1	Functional relays.
5	005A	N	7	1st Word
6				2nd Word
7				3rd Word
8				4th Word
9				5th Word
10				6th Word
11				7th Word
12	005B	N	7	1st Word
13				2nd Word
14				3rd Word
15				4th Word
16				5th Word
17				6th Word
18				7th Word

Table 5-24

PARAMETERS SCREEN ENTRIES, GROUP 6 (Refer to Figure 5-24.)

#/#	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0068	D	1	
2	0064	N	3	1st Word, V1
3				2nd Word, V2
4				3rd Word, V3
5	0065	N	3	1st Word, I1
6				2nd Word, I2
7				3rd Word, I3
8	0066	N	3	1st Word, IMAX V1
9				2nd Word, IMAX V2
10				3rd Word, IMAX V3
11	0067	N	7	1st Word
12				2nd Word
13				3rd Word
14				4th Word
15				5th Word
16				6th Word
17				7th Word
18	006C	N	6	1st Word
19				2nd Word
20				3rd Word
21				4th Word
22				5th Word
23				6th Word
24	0070	N	4	1st Word
25				2nd Word
26				3rd Word
27				4th Word
28	0076	N	1	
29	0071	N	1	
30	006B	N	7	1st Word
31				2nd Word
32				3rd Word
33				4th Word
34				5th Word
35				6th Word
36				7th Word
37	006D	N	6	1st Word
38				2nd Word
39				3rd Word
40				4th Word
41				5th Word
42				6th Word
43	0074	N	4	1st Word
44				2nd Word
45				3rd Word
46				4th Word
47	0077	N	1	
48	0075	N	1	

```

*****
*PARAMETERS Group 6 xxxxxxxxxxxxx*
*SUPPLIES Step #1# *
* Voltage Test Limit I-max *
*V1= #2# I1= #5# #8# *
*V2= #3# I2= #6# #9# *
*V3= #4# I3= #7# #10# *
*--- S1 -----Parm-----Func---*
*IIL #11# @VIL #18# #24# *
*IIH #12# @VIH #19# #25# *
*VOL #13# @IOL #20# #26# *
*VOH #14# @IOH #21# #27# *
*IZL #15# @VZL #22# *
*IZH #16# @VZH #23# *
*IOS #17# #28# @VOS #29# *
*--- S2 -----Parm-----Func---*
*IIL #30# @VIL #37# #43# *
*IIH #31# @VIH #38# #44# *
*VOL #32# @IOL #39# #45# *
*VOH #33# @IOH #40# #46# *
*IZL #34# @VZL #41# *
*IZH #35# @VZH #42# *
*IOS #36# #47# @VOS #48# *
*****

```

Figure 5-24. Parameters screen, group 6.

```

*****
*ALT PARAM  Group 6  xxxxxxxxxxxx*
*Parm Step  #1# to #2# Parm Func *
* Voltage   Test Limit  ###  ###*
*V1=+x.xx V  I1= x.xxmA  #3#  #4#*
*V2=+x.xx V  I2= x.xxmA  ###  ###*
*V3=-x.xx V  I3= x.xxmA  ###  ###*
*--- S1 -----Parm-----Func---*
*IIL # 5#    @VIL+X.XX V  +X.XX V*
*IIH # 6#    @VIH+X.XX V  +X.XX V*
*VOL # 7#    @IOL X.XXmA  X.XXmA*
*VOH # 8#    @IOH X.XXmA  X.XXmA*
*IZL # 9#    @VZL+X.XX V      *
*IZH #10#    @VZH+X.XX V      *
*IOS #11#    X.XXmA  @VOS+X.XX V*
*--- S2 -----Parm-----Func---*
*IIL #12#    @VIL+X.XX V  +X.XX V*
*IIH #13#    @VIH+X.XX V  +X.XX V*
*VOL #14#    @IOL X.XXmA  X.XXmA*
*VOH #15#    @IOH X.XXmA  X.XXmA*
*IZL #16#    @VZL+X.XX V      *
*IZH #17#    @VZH+X.XX V      *
*IOS #18#    X.XXmA  @VOS+X.XX V*
*****

```

Figure 5-25. Alternate parameters screen, group 6.

Table 5-25
ALTERNATE PARAMETERS SCREEN ENTRIES, GROUP 6 (Refer to Figure 5-25.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	0072	D	1	
2	0073	D	1	
3	006A	B	1	Parametric relays. Bit 1,2,3,4 imply relays 1,2,3,4. If the bit = 0, then the relay is activated. If the bit = 1, then the relay is not activated.
4	0069	B	1	Functional relays.
5	006E	N	7	1st Word
6				2nd Word
7				3rd Word
8				4th Word
9				5th Word
10				6th Word
11				7th Word
12	006F	N	7	1st Word
13				2nd Word
14				3rd Word
15				4th Word
16				5th Word
17				6th Word
18				7th Word

```
*****
*GATE/ STROBE      xxxxxxxxxxxxxxxxxxxxxx
*-----*
*          Sync Clock          TIMING
*          x.xxMHz             Unit   Sec
*
* |-----|-----| #1#   x.xxn
*
*   G/S Set A
*
*G: ---^----- #2#   x.xxn
*S: ---^----- #3#   x.xxn
*   G/S Set B
*
*G: ---^----- #4#   x.xxn
*S: ---^----- #5#   x.xxn
*-----*
*
* Pin #:
*       12345...
*GS Set: #6#...
*
* Pin #: 2222
*       5678...
*GS Set: BAABB...
*****
```

```

*****
*PROGRAM CALL*
*
*-----*
*
*
*
*
*Tape Program Name = #1#
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*****

```

Table 5-26
GATE/STROBE SCREEN ENTRIES (Refer to Figure 5-26.)

Table 5-27
PROGRAM CALL ENTRIES (Refer to Figure 5-27.)

5-30 EXTENDED SYSTEMS

```

*****
*TAPE OPERATION*
*-----*
*MODE: #1#General Tape Operation*
*   ###Results Call/Record*
*-----*
*###List Tape Directory*
*###Delete Prog/Res   #2#*
*#3#Restore Prog/Res  #4#*
*###Compress Tape*
*###Format Tape:*
*   Tape Name   #5#*
*   Comment     #6#*
*-----*
*###Call Result   #7#*
*#9#Record Result #8#*
*   Send All Result Files to*
*           System Output*
*-----*
*
*
*
*
*
*****

```

Other messages that can appear on the bottom two lines are:

```

Operation successful
Cartridge not in place
Tape error
Write protected
Bad tape in drive
No such file
File already deleted
File not found
File was not deleted
Not enough space for file
Directory is full
Operation completed with errors
File name already exists
File was deleted
Not a program file
Error while writing directory; tape may be lost
Extra tape not used
Bad directory on tape

```

Figure 5-28. Tape operation screen.

Table 5-28
TAPE OPERATION SCREEN ENTRIES (Refer to Figure 5-28.)

###	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	007D	B	1	1 - General operation mode 2 - Results mode
2	007B	I	12	File name (complete)
3	007E	B	1	General operation mode: 1 = list directory 2 = delete 3 = restore 4 = compress tape 5 = format tape
4	007B	I	12	File name (complete)
5	014E	I	12	Tape name
6	014F	I	16	Comment
7	0081	I	12	File name (with extension)
8	0081	I	12	File name (base only)
9	007F	B	1	Result mode: 1 = retrieve result file 2 = save result file 3 = output all result files.

```

*****
*PROGRAM RECORD*
*
*-----*
*
*
*
*
*Tape Program Name = #1#*
*
*Comment = #2#*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*****

```

Figure 5-29. Program record screen.

Table 5-29
PROGRAM RECORD SCREEN ENTRIES (Refer to Figure 5-29.)

#"	Index Address	Data Type	No. of Entries or Characters	Entry Options
1	007B	I	12	Program file name
2	007C	I	16	Comment

Table 5-30
GENERAL PROGRAMMING FLAGS NOT ON SCREENS

Index Address	Data Type	No. of Entries or	Entry Options																		
00E4	B	1	The general pass/fail flag 0 = Fail 1 = Pass																		
0117	B	48	Each pin has one set of fail flags; one set is one byte. If bit = 0, there is no failure. If bit = 1, there is a failure. <table><tr><td>Bit number</td><td>Parametric reference</td></tr><tr><td>7</td><td>IIL</td></tr><tr><td>6</td><td>IIH</td></tr><tr><td>5</td><td>VOL</td></tr><tr><td>4</td><td>VOH</td></tr><tr><td>3</td><td>IZL</td></tr><tr><td>2</td><td>IZH</td></tr><tr><td>1</td><td>IOS</td></tr><tr><td>0</td><td>I1, I2, or I3,</td></tr></table> for pin with ID of V1, V2, or V3.	Bit number	Parametric reference	7	IIL	6	IIH	5	VOL	4	VOH	3	IZL	2	IZH	1	IOS	0	I1, I2, or I3,
Bit number	Parametric reference																				
7	IIL																				
6	IIH																				
5	VOL																				
4	VOH																				
3	IZL																				
2	IZH																				
1	IOS																				
0	I1, I2, or I3,																				
0080	B	1	Indicates the tape operation <table><tr><td>Bit</td><td>Operation</td></tr><tr><td>0</td><td>Call program</td></tr><tr><td>1</td><td>Record program</td></tr><tr><td>2</td><td>Tape operation screen</td></tr></table>	Bit	Operation	0	Call program	1	Record program	2	Tape operation screen										
Bit	Operation																				
0	Call program																				
1	Record program																				
2	Tape operation screen																				
0079	B	1	Enable/disable screen output during remote control. Bit 0 = 1, Disable screens Bit 0 = 0, Enable screens																		
00DB	B	1	Power-supply shut-down flag: 0 = no shutdown Not 0 = there is a shutdown.																		
0152	B	1	Indicates the no. of groups; must be programmed in harmony with data in address 00A2 (describe screen). For groups: 1 2 3 4 5 6 Set bits: (none) 0 1 2 3 4, keeping bits 5, 6, and 7 at logic 0.																		
0118	P	32	1st Screen line, Characters 0 to 32																		
0119	P	32	2nd Screen line																		
011A	P	32	3rd Screen line																		
011B	P	32	4th Screen line																		
011C	P	32	5th Screen line																		
011D	P	32	6th Screen line																		
011E	P	32	7th Screen line																		
011F	P	32	8th Screen line																		
0120	P	32	9th Screen line																		
0121	P	32	10th Screen line																		
0122	P	32	11th Screen line																		
0123	P	32	12th Screen line																		
0124	P	32	13th Screen line																		
0125	P	32	14th Screen line																		
0126	P	32	15th Screen line																		
0127	P	32	16th Screen line																		

Table 5-30 (Continued)
GENERAL PROGRAMMING FLAGS NOT ON SCREENS

Index Address	Data Type	No. of Entries or Characters	Entry Options
0128	P	32	17th Screen line
0129	P	32	18th Screen line
012A	P	32	19th Screen line
012B	P	32	20th Screen line
012C	P	32	21st Screen line
012D	P	32	22nd Screen line
012E	P	32	1st Screen line, Characters 33 to 64
012F	P	32	2nd Screen line
0130	P	32	3rd Screen line
0131	P	32	4th Screen line
0132	P	32	5th Screen line
0133	P	32	6th Screen line
0134	P	32	7th Screen line
0135	P	32	8th Screen line
0136	P	32	9th Screen line
0137	P	32	10th Screen line
0138	P	32	11th Screen line
0139	P	32	12th Screen line
013A	P	32	13th Screen line
013B	P	32	14th Screen line
013C	P	32	15th Screen line
013D	P	32	16th Screen line
013E	P	32	17th Screen line
013F	P	32	18th Screen line
0140	P	32	19th Screen line
0141	P	32	20th Screen line
0142	P	32	21st Screen line
0143	P	32	22nd Screen line

Measurement Theory—Section 6

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6.1 GENERAL

The purpose of this section is to provide the user with an understanding of how the system performs each test and how the tests and screens are interrelated. The section will begin with a discussion of the screens, limited to those factors which affect how the system performs the various tests. The functional and parametric tests both use the functional pin electronics and truth table to set up the desired test state, so the theory behind the functional test will be discussed before the theory behind the parametric test. Since the continuity test uses the parametric measurement unit and can be considered a specialized form of the parametric test, it will be described after the parametric test.

Throughout the remainder of this section, it is assumed that power has been applied to the system, that the DUT has been inserted into an appropriate socket adaptor on the pin electronics module, and that both system software and a valid test program reside in system memory.

The system must have the proper data specified in the describe, parameters, alternate parameters, truth table, and run-mode screens in order to test a device. Information on how to enter data in these screens can be found in Sections 3 and 4.

6.1.1 Describe Screen

The describe screen defines the DUT for the test program. The clock frequency and sync values are entered, pins are labeled, and pin sets defined. The structure of the test program itself is set up by the value entered for the number of groups.

Pins. Pins are labeled as inputs, outputs, ground, voltage supply, bidirectional, tristate, clocks, or don't care. If a pin is defined as a don't care (X), all the VMOS switches between the DUT pin and the driver/sensor lines are turned off. The system will see only a 200-pF worst-case load at that pin. Tristate and bidirectional pins are further defined by the entries in the truth table. Pins labeled Vi (where i is 1, 2, or 3) enable selection of voltage and current limits for those power supplies in the parameters screens, but they must be hardwired to the voltage sources on the DUT socket adaptor board.

Pin Sets. There are two sets of 6 registers on the parametric board that are available to define the voltage and current levels for testing. By assigning a pin to one of the two pin sets, the system can identify which set of registers to enable when testing a given pin. The values in each register can change from group to group, but the pin set assignment remains fixed throughout the test pro-

gram. For simple devices, there is normally a need for only one pin set (one set of logic levels), so every pin can be in pin set 1. If some pins had different current limit specifications or required different voltages than others, then some pins would be assigned to pin set 1 and others to pin set 2.

Clock Frequency. The functional test rate is set by the frequency supplied to the sync. The 1732 can supply this specified frequency by using a software-programmable oscillator and hardware wiring of a divider output to the sync. The clock frequency specified here is converted into a 4-bit count which the system loads into a register on distribution board No. 2. This board also contains a 32-MHz oscillator that is used as the base frequency for the high-speed controller and DUT clocking. This oscillator frequency is divided by 2 to produce the 16-MHz clock for the high-speed controller and the gate/strobe circuitry.

Any one of 15 different counts can be loaded into the clock register by the system. The register increments by one each time it receives a pulse from the 32-MHz clock; when it reaches its maximum count, it reloads the starting count and toggles a flip-flop. If the free-run signal from the high-speed controller is also present at the flip-flop, a pulse is sent into the divider network. This network produces the 5 different submultiples of the clock frequency, but, in order to select one of the submultiples, a jumper must be installed on the DUT socket adaptor.

The selected submultiple of the clock frequency is shaped and sent to the high-speed controller board as a clock "tick." Two high-speed clock "ticks" produce one clock frequency pulse. On the first high-speed clock "tick," the DUT clock pulse goes from low to high, and on the second "tick" it goes from high to low. The sync flip-flop simultaneously triggers a one-shot multivibrator and the microsequencer that generates the next step of the truth table to be performed. This one-shot resets the sync flip-flop to the default condition, guaranteeing a minimum period of 30 nanoseconds for the pulses that are fed to the microsequencer and for those signal pulses which require clocking.

Sync. The clock frequency supplied by the system is divided by the sync to produce a submultiple of the clock frequency. The entry on the describe screen serves primarily as an aid to the operator, since the actual hardwired implementation of the sync takes place on the DUT socket adaptor. The sync signal on the socket adaptor is fed back to the high-speed controller, where it triggers the controller to generate the address of the next step of the

truth table. It should be noted that parametric testing exercises the truth table functionally until the step meeting the logic level requirements for that test is found; the clock is then stopped and the parametric test performed. If the DUT requires a negative-going clock edge to trigger an output state change, then the only value of sync which will provide the negative-going edge is C1. This is assuming that, first, the system is supplying the sync signal and, second, the clock input to the DUT is the same as the sync line. It is important to remember that the final test frequency cannot exceed 2 MHz in any case.

Number of Groups. The number entered on the describe screen causes the system to enable the entry of data into that number of parameters group screens. An attempt to call up a parameters group screen for a higher-numbered group than that number entered in the describe screen will not be recognized by the system.

6.1.2. Gate/Strobe Screen

Pins defined in the describe screen as input, bidirectional, or tristate and further defined as being inputs in the truth table for a given step require a gate signal. The system has stored the input pattern in the $4K \times 4$ RAM for that driver/sensor pin. As each step is executed, the data are latched into an internal register of the driver/sensor chip for that pin. The gate signal gates the data from the driver/sensor chip into the DUT. Pins defined in the describe screen as output, bidirectional, or tristate and further defined as being outputs in the truth table for a given step require a strobe signal. While each step of the truth table is being executed, the strobe signals strobe the data from the DUT into the driver/sensor chip, setting its internal latches and the internal error flip-flop.

The gate/strobe screen allows the user to specify two independent sets of gate/strobe timing values, A and B. Each driver/sensor pin can be set individually for strobe A or B, and the corresponding gate signal is automatically selected for that pin. The values of a strobe and its associated gate can be set independently within certain constraints. The unit of time that the gate/strobe circuitry deals with is 62 nanoseconds. The limits on the gate/strobe values are such that the gates cannot be earlier than 312 nanoseconds after the beginning of the truth-table step's execution (T0) and the strobes cannot be later than 62 nanoseconds before the next T0.

The gate and strobe signals originate in 4 ports on distribution board No. 2. These ports, which correspond to the gates and strobes, are loaded with values determined by the entries in the gate/strobe screen. At time T0, 4 counters are loaded with the data in the 4 ports and are clocked by a 16-MHz clock. At their maximum count, the counters go into a hold mode and trigger a pulse-forming network which generates a 62-nanosecond pulse. The gate and strobe signals go first to mother board No. 2 and then to the driver/sensor boards, where the gate signals are applied to those driver/sensor chips feeding pins defined as inputs and the strobe signals are applied to those driver/sensor chips sensing pins defined as outputs.

6.1.3 Parameters Screen

The parameters screen defines the voltage and current values that the system uses to test the DUT both functionally and parametrically in the test program. This screen

is organized in three sections, running from top to bottom. The first section defines the power-supply setup that will be used in that group's test. Values for voltage, test limit (li), and shutdown current limit (I-max) can be specified for each of the 3 power supplies. The second and third sections are identical in structure. The second section defines the values used for pin set 1 while the third section defines the values used for pin set 2. Each of these sections is divided into 3 columns, with the exception of the parameters for measuring IOS. The first column is used to enter the values the system compares to the test results when determining whether the DUT passes or fails either the parametric or functional tests. The second column is used to enter the value forced on each pin during parametric testing so that the parametric measurement unit can measure properly the values to be compared to the first column. The third column is used to enter the values forced on the pins during the functional test. During parametric testing, these values are also forced on all pins except the one under test.

Power Supply Voltages and Current Limits. The voltages specified for PS1, PS2, and PS3 in the parameters screen are supplied to the DUT via jumper wires on the socket adaptor. Unlike the sync (refer to para 6.1.1), the values for these voltages entered in the parameters screen are more than an aid for the operator. The system can't perform the power-supply tests without them. The values of "I" entered for (Vi) in the describe screen pin IDs dictate to the software which power supplies will be monitored for current conditions. The test limit (li) specified is the maximum steady-state-current value allowed for the pass or fail determination of the parametric test. It occurs at a specific step in the truth table which meets the test conditions required by the manufacturer's data sheets. If the test limit current value is exceeded, the power-supply test fails but other tests may be conducted.

The voltage and current information for each DUT power supply specified in the parameters screen is loaded into registers on the parametric board. Because all 3 supplies operate in a similar fashion, for the purpose of this explanation, PS1 will be used as an example. These registers in turn set up the PS1REF and PS1CL levels which control the amount of voltage and current the power supply will produce. The PS1REF level is fed through 2 op amps to produce the PS1V signal level. This voltage level is applied to the voltmeter analog multiplexer and the voltmeter itself, where it is checked under the program's direction. Current limiting is performed by 2 buffers sampling the voltage on both sides of the current sensing resistor. They produce a voltage, called PS1I, in a differential amplifier. This voltage is also routed to the voltmeter for possible checking, but its primary function, in combination with PS1CL, is to put the power supply in the current limiting mode. If PS1CL is more positive than PS1I, it indicates that the power supply has exceeded the current "max" specified in the parameters screen, and the LIMIT1 signal is driven low. The LIMIT1 signal shuts down the power supply, as explained below.

I-max Current Limit Operation. If the value specified for I-max is exceeded during a test, the test is aborted and all DUT power supplies are shut down to prevent damage to the DUT. The program supplies the parametric board with a

current limit reference level PS1CL. The digital-to-analog converter (DAC) provides an input current sense level (PS1REF) to the DUT power supply circuit. When the sense level exceeds the reference level, it turns on a transistor which toggles the LIMIT1 latch. This latch shuts down the 3 DUT power supplies. The PS1 source line is opened, thus removing it from the DUT. This prevents damage to the DUT. Simultaneously, the PS1 sense line is opened, preventing damage to the system. Each power supply is monitored and the program receives information as to which supply caused the shutdown.

The value of I-max is usually chosen as a "worst-case" current, calculated by adding all expected dynamic and static current loads, as explained for each device family in Section 4. That value of I-max may not be suitable for all the test groups throughout the entire program. (Refer to para 6.3.3)

Test Conditions and Limits. Test conditions and limits for functional and parametric tests can be specified in either one or both of two pin sets on the parameters screen. Each of the pin sets is identical in layout. The first column contains the entries for the test limits, the second column contains the entries for the parametric test conditions, and the third column contains the entries for the functional test conditions. The exception to this format, IOS, has first a minimum limit, then a maximum limit, and finally the test condition specified. This is the only parameter that can be specified with both minimum and maximum limits on a single screen.

Under the headings S1 (pin set 1) and S2 (pin set 2), current and voltage limit values are assigned for the parametric tests, e.g., IIL and IIH, which also require parametric forcing functions (in this case VIL and VIH) to be measured properly. Assume, for example, that a manufacturer specifies that, to measure properly an IIL test limit of 400 μ A, a VIL of 600 mV must be forced. This means that, with a forcing voltage of 600 mV at one input pin of the device, if the IIL is measured and it exceeds 400 μ A in magnitude, the DUT will fail the IIL test. The manufacturer's data sheets are the source for the logic levels entered into the test limit and condition columns.

The system interprets each of the first column entries except VOH and IOS as a maximum-allowable entry. VOH is the minimum-allowed value for a high, and IOS has both a minimum and a maximum value entered on the parameters screen. The logic levels for functional operation, as listed on a manufacturer's data sheet, are entered into the functional test condition column. (For TTL devices, the functional input voltage levels are normally specified by the Vout parametric test condition.)

The two pin sets operate in an identical manner. Each pin set has 6 registers and 6 D/A converters (DAC) assigned to it. Four of the register/DAC pairs receive the VIL, VIH, VZL, and VZH entries from a single parameters group screen. The remaining 2 register/DAC pairs receive the IOL and IOH entries from the same parameters group screen. These entries can be either functional or parametric test conditions, depending upon the test being performed.

The system converts the entries for each parametric or functional current and voltage condition into a 12-bit code. This code is routed to the register of the appropriate DAC and is transformed into the desired voltage level. The

resulting voltage is then placed on an analog bus. The current references are set up in the same fashion as the voltage references; a voltage is produced which is proportional to the current and that voltage is then placed on the analog bus. The analog bus routes these voltages to the DUT and to the voltmeter.

The values of the parametric test limits for IIL, IIH, VOL, VOH, IZL, and IZH are stored in memory on the 64K RAM board. Once the parametric measurement unit has converted the tested value back to a digital form and measured it, the result is sent back to the Z80 for comparison with the value stored in memory. If the test result does not fall within the range allowed for it by memory, the Z80 will mark the pin as faulty and store the result according to the option selected in the display screen. If the Pass/Fail/Bin mode is selected, the result will be stored in binary code. If any other display mode is selected, the result will be stored in floating-point code. The values for the functional test conditions are stored in the registers by the system prior to the execution of a functional test; when the system executes a functional test, it matches the test results against the values stored in the memory on the driver/sensor board. The values of the parametric and functional test conditions are not required to be the same. Each test condition is independent of the others.

Typically, more than one group of tests is required. (Be sure to enable the required number of groups by entry in the 3rd line in the describe screen.) As an example, for TTL devices, the typical manufacturer specifications normally require IIL and IIH to be measured at Vcc max (5.25 V) and IOL and IOH to be measured at Vcc min (4.75 V). Since the power supply for each group is fixed, 2 groups are required. The system will reload the registers with the new current and voltage references before the start of the new group's test and refer to the new test limits stored in memory when comparing the results.

If the forced test conditions and power-supply conditions are the same for both minimum and maximum values of parameters to be tested, the alternate parameters screen can be used as described below.

6.1.4 Alternate Parameters Screen

The alternate parameters screen for a group can be accessed only if enabled by entry of a sufficiently large digit for NUMBER OF GROUPS in the describe screen. The alternate parameters screen is used to define in which portion of the truth table the parametric tests for that group will be performed. This is accomplished by specifying start and stop steps for the parametric testing in the group. Thus, these tests can be delayed until after certain steps have been completed to set the DUT into a desired state. Entries in the alternate parameters screen also control the use of up to 4 relays in functional and parametric testing. Entries for each relay can be set independently for either or both tests, if desired. If these entries are selected, the system provides enabling signals only. The relays must be installed on the DUT socket adaptor.

A major use of the alternate parameters screen is to specify other test limits to test both minimum and maximum values for IIL, IIH, VOL, VOH, IZL, and IZH. On this screen, the maximum limit for the magnitude of VOH and the minimum limits for the magnitudes of the other parametric tests are listed in the same groups and pin sets

as on the parameters screens. The same test conditions for the functional and parametric tests that were used in the parameters screen are used automatically by the system in the alternate parameters screen, but additional tests limits can be input. Thus, the DUT must produce test results within a defined pair of limits in order to pass the tests. The system operates in the same manner as described above but, if the DUT is to pass, the additional limit must be met when the result is compared against the values stored in the main memory.

6.1.5 Truth Table Screen

The truth table provides the sequence of steps that each test will follow, including the logic pattern that the DUT input pins will be forced into at each step and the output logic pattern that must be recognized if the DUT is to pass the functional test. The truth table will execute one step each time a positive edge appears on the DUT sync line.

When the system encounters a "don't care" logic state in the truth table, its actions are determined by the definition of that pin in the describe screen and by the function it is performing at that step of the truth table. If a pin was defined in the describe screen as a don't care, the system only sees a load of approximately 200 pF at that pin throughout the test. If the pin was defined as a tristate, the active load is enabled and the current driver at the output of the driver/sensor chip goes to the high-impedance condition, disconnecting the driver/sensor line from the pin. Input pins and bidirectional pins acting as inputs for that step of the truth table are disconnected from the driver/sensor lines when the driver disconnect signal goes into the high-impedance state and the active load is disabled. Output pins and bidirectional pin acting as outputs for that step of the truth table are disconnected from the driver/sensor lines when the driver disconnect goes into the high-impedance condition. The pins aren't loaded by the active load.

6.1.6 Run-Mode Screen

The run-mode screen enables continuity, Kelvin, functional, and parametric testing. It also controls the sequence of functional and parametric tests, what the functional test start and stop steps will be, whether or not the parametric and functional tests will be performed on a particular bin for a particular group, when the procedure will halt, and whether or not the keyboard is locked.

Test Sequence. Although the continuity, Kelvin, functional, and parametric tests can be specified in any order, the continuity and/or Kelvin test will always be performed first (if enabled). The functional and parametric tests are performed in the order selected.

Bin Assignment Field. The system is instructed by the bin assignment field to run tests in only those groups that have been assigned to at least one bin. Test execution will begin with the lowest numbered group that has either a functional or a parametric test enabled in any bin. If both functional and parametric testing are enabled for the same group, the order of execution of the tests within that group will be the order specified in the test sequence entry.

At the beginning of each test, the Z80 will load the registers and DACs on the parametric board with the test conditions specified for the group and test being performed.

Functional Start and Stop Step. The functional start and stop step specifications can be used to set where the functional test will begin in the truth table and where it will end. Steps prior to the functional-test start are NOT available for establishing an initial logic condition for the functional test, because the high-speed controller's starting address is actually set by the system to the value entered for the functional start step in the run-mode screen. (However, for each parametric test, the steps from step zero to the parametric start step for that group are executed at the functional-test rate to set up a desired logic condition for the test.)

Testing Mode. The option selected in this field will determine what the system will do when it encounters a fault or completes the test. Note that the RUN CONTINUOUSLY option is used with the Z command when debugging a test program (Refer to para 4.7.)

6.2 FUNCTIONAL TESTING

6.2.1 Functional Test Sequence

Figure 6-1

The system software provides all the necessary programming to perform a functional test except for certain options (such as which run mode is selected) and data (such as the test limits and conditions and the truth table) that are provided by the device test program. In addition to the conditions assumed at the beginning of this section, it is further assumed that a functional test is to be executed and that the START/ABORT button has been depressed. Table 6-1 briefly outlines the procedure performed by the system when it makes a functional test. A more detailed discussion of the same procedure follows.

Table 6-1
FUNCTIONAL TEST PROCEDURE PERFORMED
BY THE SYSTEM

- a. Set up the DUT power supply voltages and the functional drive/sense levels for the functional driver/sensors.
- b. Apply power to the DUT.
- c. Start clock and check for the absence of sync (time out). Reset H/S/C.
- d. Cycle the DUT through the truth table, starting at the functional-test start step.
- e. Make the functional tests.
- f. Compare the sensed output to the expected result stored in the truth table.
- g. Display the results.

a. *Set up the DUT power supply voltages and the functional drive/sense levels for the functional driver/sensors.* From the parameters screens stored in memory on the 64K RAM board, the system will enter the values of voltage and I-max for the power supplies and the force and sense levels of voltage and current for the functional test conditions required to test the DUT. The sync clock frequency derived from the clock frequency and sync values on the describe screen is entered into registers on the distribution board No. 2, along with the gate and strobe information from the gate/strobe screen.

The Z80 calls out data from memory to set up the functional test conditions; this information is transmitted to the parametric board. The parametric board then sets up the voltage and current drive and sense levels that will be

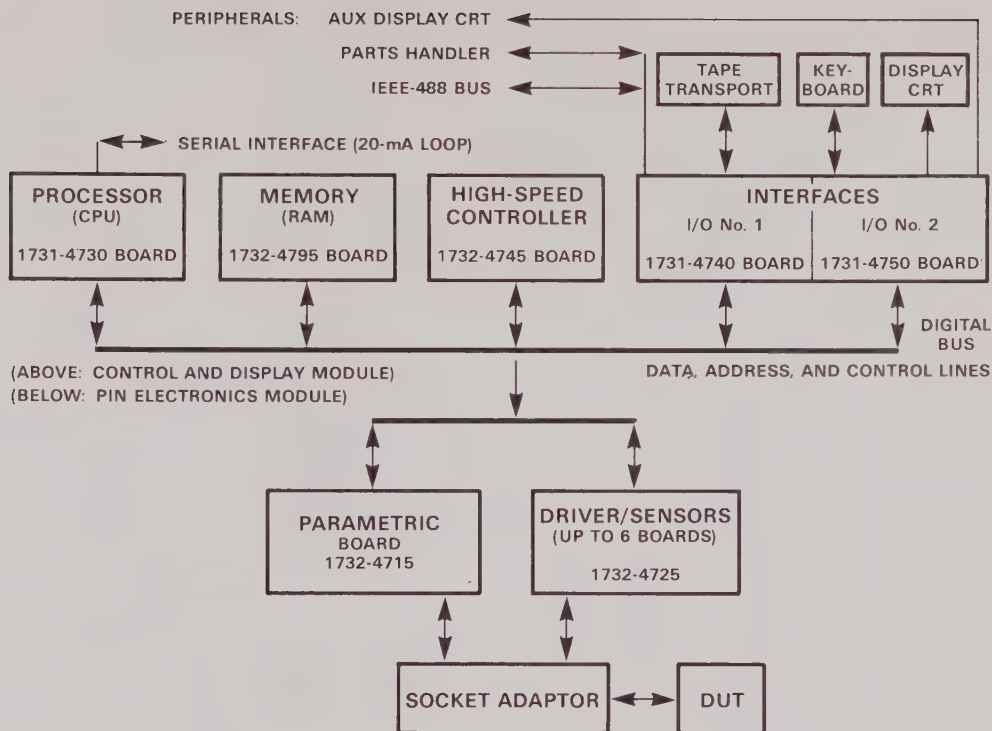


Figure 6-1. The 1732 system block diagram, simplified.

needed to conduct the test. These levels are routed to the driver/sensor boards. The parametric board sets up the device power-supply voltages (V_1 , V_2 , V_3) and corresponding shutdown current values (I_{MAX}) and supplies dc power to the socket adaptor.

If the program resides in a tape cartridge, the Z80 transferred the truth table from the tape cartridge through the high-speed controller to the driver/sensor boards when the program was called up. If the program was entered from the keyboard, a line of the truth table was transferred whenever the [ENTER] switch was depressed. The truth table is stored in the $4K \times 4$ RAM behind each driver/sensor pin. The Z80 transmits the functional-test start and stop addresses to the high-speed controller, which starts the functional test.

b. *Apply power to the DUT.* The test cycle begins with the DUT pins disconnected from the driver/sensor and parametric measurement unit lines. The device power supplies are turned on and allowed to stabilize at the values of voltage and current specified for functional testing. Once the voltage and current levels have settled, the system connects the driver/sensor lines to the DUT pins.

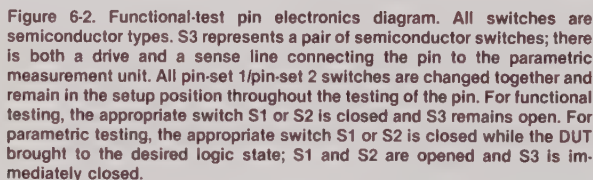
c. *Cycle the DUT through the truth table*, starting at the functional-test start step. Testing proceeds at the rate of 1 step per positive sync edge except where a wait command appears in the truth table. If a wait command is encountered, the system will execute the step associated with the wait command for the number of clock cycles defined in the wait command. At each step, the system forces the specified functional high-level (V_{IH}) or low-level

(V_{IL}) voltage at each input and sinks or sources a current (functional IOH or functional IOL) at each output pin, in accordance with the actual DUT output logic state with respect to V_{mid} .

d. *Make the functional tests*, during which the system forces the logic states of input pins as defined in the truth table and provides current loading for output pins. The functional test logic circuitry remains connected to all pins of interest. V_{OH} and V_{OL} , as specified in the functional test conditions column of the parameters screen, are used as reference values. (Refer to para 6.2.2.) If the output voltage equals or exceeds V_{OH} , a logic high (1) is sensed. If the output voltage is less than or equal to V_{OL} , a logic low (0) is sensed. However, if the voltage is less than V_{OH} and greater than V_{OL} and tristate sensing is enabled, the high-impedance state is sensed.

e. *Compare the sensed output to the expected result stored in the truth table.* If the response does not match the truth table, the functional test is aborted, and an error message is generated. The system stores the identity of the pin that failed and the step at which it failed. If there is a functional failure and ALL GROUPS FIRST FAILURE or TEST CONTINUOUSLY TO FAILURE were selected on the run-mode screen, all testing is terminated. Otherwise, the next group available will be tested.

f. *Display the results.* If all testing is terminated, the parametric-results screen, result-summary screen, or a pass/fail screen will be displayed. The option that was selected in the display-mode screen will determine which of the screens will be used.



The DUT pin shown in the functional-test pin electronics diagram is connected to either a voltage driver (input pin, S1 closed) or a current load and functional sensor (output pin, S2 closed) during the functional test. Only one of the three switches (S1, S2, or S3) can be closed at a given instant. The switches represent semiconductor VMOS switches. If the pin of interest has been designated an input pin by its definition in the describe screen, S1 will be closed. If it is a member of pin set 1, the VIH and VIL values from pin set 1 will be fed into the input drive circuit. The truth table will control which logic level is passed through the drive circuit to the DUT pin for each step. These levels are forced onto the pin when the gate signal is received at the driver/sensor chip in the driver/sensor circuit. No measurements are made on an input pin during a functional test, thus no error sensing is performed on input pins during this test.

The voltage at the loaded output pin is sensed in the functional error logic when the strobe signal is applied to the driver/sensor circuit. If the gate/strobe timing is set in-

The functional-test electronics are also used during the parametric testing to exercise the DUT by forcing inputs and loading outputs functionally, as defined in the truth table. The elementary functional procedure (without monitoring outputs for functional-test results) advances from step zero until the pin of interest reaches the desired logic state within the portion of the truth table bounded by the parametric start and stop steps. Then S1 or S2, whichever was connected, is opened and S3 is closed, enabling the parametric measurement unit to force the voltage or current and make its measurement. (References are made to S1, S2, S3 of the simplified diagram, not to mechanical switches. S3 represents a pair of semiconductor switches.) The parametric lines are Kelvin, and have both a sense and a drive line to the parametric measure-

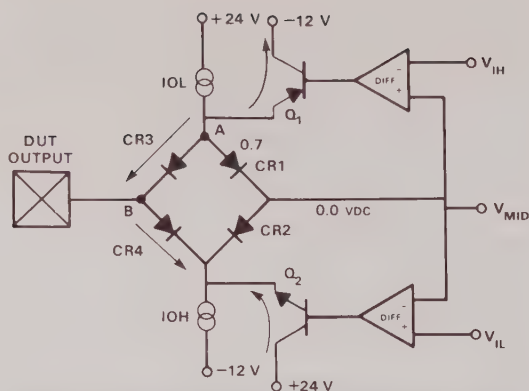


Figure 6-3. Functional active load, simplified schematic diagram.

ment unit. These lines join at a Kelvin junction, close to the DUT pin, i.e., on mother board No. 2 of systems 1732-9700 through -9704, and in the socket adaptor circuitry of systems 1732-9720 through -9724.

6.2.3 Theory of the Active Load

Figure 6-3

The functional active load, as shown in the figure, consists of a reference voltage ($V_{mid} = [V_{OH} + V_{OL}] / 2$), a current source (IOL), and a current sink (IOH). If the differential amplifiers are on, the bypass transistors Q1 and Q2 are on. This causes the current loads, as seen by the diode bridge, to be off. All the current to or from the current generators is bypassed to -12 V and +24 V, respectively. (This is only a rough approximation of how the current generator works.)

For proper operation of the active load, V_{IL} and V_{IH} must be set at values which will enable the two current generators. As an example, consider an imaginary device operating under the following conditions:

$$V_{IL} = -1 \text{ V}$$

$$V_{IH} = +1 \text{ V}$$

$$V_{OL} = -2 \text{ V, IOL} = 1 \text{ mA}$$

$$V_{OH} = +2 \text{ V, IOH} = 2 \text{ mA}$$

First, compute V_{mid} .

$$V_{mid} = (V_{OH} + V_{OL}) / 2$$

$$V_{mid} = (-2 + 2) / 2 = 0 \text{ V}$$

Next, the current sources are examined. (Refer to the simplified diagram of the functional active load.) To enable the generator for IOH, for example, V_{IL} must be about 250 mV less than V_{mid} . If V_{mid} is 0 V and V_{IL} is -1 V, bypass transistor Q2 is turned off and IOH is enabled. IOL is enabled in a similar fashion.

At this point, assume that the current generators are enabled, V_{mid} is applied, and no device output is connected. In the diode bridge, V_{mid} is applied at the junction of the cathode of CR1 and the anode of CR2. Assuming ideal silicon diodes, approximately 0.7 V will be dropped across any one diode junction. Point A on the diagram will be at 0.7 V (or $V_{mid} + 0.7 \text{ V}$) due to the rise across CR1. Point B will be at 0.0 V (or V_{mid}) due to the 0.7 V voltage drop across CR3. This means that the bridge is in balance. Some portion of IOL will flow through CR1 to V_{mid} , while the remainder will flow through CR3 and CR4 to IOH. In a similar fashion, a portion of IOH will flow through CR2 from V_{mid} and the rest will come from IOL.

Now assume that a DUT output has been placed on the bridge at point B. If the DUT output (logic high) is initially +2.1 V (no load), CR3 will be reverse-biased and CR4 will be forward-biased. The total current IOH will be drawn from the DUT through CR4 (not from V_{mid} through CR2). If the DUT can source the 2-mA IOH while maintaining 2.1 V, the functional-error logic circuit will sense $V_{out} > V_{OH}$, thus recognizing a logic high.

However, if the DUT is unable to source the 2-mA IOH at a voltage above V_{OH} , the system cannot recognize a logic high. The DUT output voltage will drop, for example, down to 0.6 V while sourcing 2 mA. The comparators in the functional error logic circuit will then sense that V_{out} is between V_{OL} and V_{OH} . If this pin is designated "tristate", the system will recognize that it is in the high-impedance state.

Similarly, if the DUT output is logic low (for example -2.1 V open circuit) and able to sink the 1-mA IOL while maintaining a voltage below -2 V, the system will recognize the low state. However, if the current load forces the DUT output pin to a voltage nearer zero, the system will not recognize a low state; it will recognize a high-impedance state if the pin is classified tristate.

The DUT will fail the functional test if the expected output at a step of the truth table is a logic high and the output of a DUT is unable to source the amount of IOH or if the expected output at a step of the truth table is a logic low and the output of a DUT is unable to sink the amount of IOL specified in the functional test conditions of the group under test.

In summary, the output of the DUT steers the diode bridge with reference to V_{mid} . The current generators are enabled for a given pin set by disabling the bypass transistors. To disable the bypass transistors, V_{IL} must be less than or equal to V_{mid} minus 250 mV, while the V_{IH} must be greater than or equal to V_{mid} plus 250 mV.

6.2.4 Example of Functional Test

Figure 6-4

The accompanying figure shows a hypothetical device and the truth table used to test it. There are only three pins to be concerned with; it is assumed that the V_{cc} and ground pins are wired properly to the socket adaptor and that all pins are assigned to pin set 1. Each pin is connected to a functional-test pin electronics circuit. The program stored in memory is called up and the correct voltage and current levels are set.

The test begins at the start step. Unless a start step is defined, the system defaults the functional-test start to step 0. In step 0000, V_{IL} is forced by the input drive circuits for both pins 1 and 2, as defined by the truth table. Switches S1 for both pins are closed. Switch S2 is closed for the output, pin 3. (See functional-test pin electronic diagram.) When the gate signal is received at the driver/sensor chip, the V_{IL} level is connected to the DUT pins. The period between the gate and strobe signals should equal or slightly exceed the time it takes for the logic level to propagate through the DUT. The strobe signal causes the logic level on the DUT output pin to be loaded into and sensed by the functional-test pin electronics. Since the output is higher than V_{mid} , the IOH value of current is sunk from the DUT. A logic high (1) is sensed. When this state is compared to the expected result stored in the truth table and there is a match, the DUT functionally

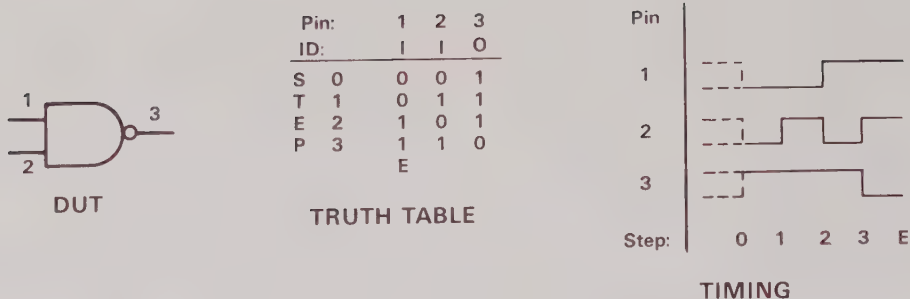


Figure 6-4. Functional test procedure, example for a simple gate.

passes this step of the truth table. The system advances to the next step of the truth table with the next positive-going edge of the sync signal, and the test continues.

6.3 PARAMETRIC TESTING

6.3.1 Parametric Test Sequence

The sequence of the parametric test procedure is described below. It is briefly recapitulated in Table 6-2. This sequence broadly parallels the functional test sequence except as follows. Only one pin (input or output) is tested parametrically for a single parameter at a time. The parametric start step and stop step are defined in the alternate parameters screen for the group being tested. For each parametric measurement, the system always starts at step 0 of the truth table and advances at full speed with functional-logic error reporting disabled, driving all inputs and loading outputs as in the functional test procedure. Parametric testing does not begin until the parametric start step is reached.

The system stops at the first step after the parametric start step where the pin being tested has been driven to the appropriate logic state for measuring the parameter being tested. If the correct logic state is not encountered for that pin before the stop step defined in the alternate parameters screen or an End command is reached, the system will ignore the pin being tested. The system will store a blank (not a failure) for the test result and continue the test procedure. If the correct logic state is encountered, the system performs the measurement. After the measurement, the system restarts the truth table at step 0 and proceeds to make another parametric test on the next pin of interest, as described in detail below.

Table 6-2
PARAMETRIC TEST PROCEDURE EXECUTED
BY THE SYSTEM

- Set up the DUT power-supply voltages and the functional drive/sense levels for the functional driver/sensors.
- Apply power to the DUT.
- Test the power supply.
- Cycle the DUT through the truth table, starting at step 0000.
- Disconnect the functional levels and then connect the parametric measurement unit to the pin under test.
- Make the parametric measurement.
- Compare the measured value with the parametric limit and determine whether the parametric test passes.
- Display the results.

a. *Set up the functional drive/sense levels.* The system calls the appropriate data from memory into certain registers, data such as values of power-supply voltage, test limit, and I-max, as well as functional forcing voltage and current levels (VIL, VIH, IOL, and IOH). These values set the device power supplies on the parametric board and the program-specified voltages for the driver/sensors to their proper levels. Test condition (drive) and measuring limit (sense) values for the parametric test being performed are also called up from memory and set up in the parametric measurement unit.

When a parametric test is selected, the following events occur. The Z80 calls out the data from the 64K memory to set up the test conditions; this information is transmitted on mother board No. 1 to the high-speed controller board, which routes it to the parametric board via the two distribution boards and mother board No. 2. The parametric board then sets up the voltage and current drive and sense levels that will be needed to conduct the test and routes them to the parametric switches (S3) on the driver/sensor boards for the pin to be tested. The parametric board also supplies dc power for the DUT and sets up the device power-supply voltages and shutdown current values.

b. *Apply power to the DUT.* The test cycle begins with the DUT pins disconnected from the driver/sensor and parametric measurement unit lines. The device power supplies are turned on and allowed to stabilize at the values of voltage and current specified for functional testing. Once the voltage and current levels have settled, the system connects the driver/sensor lines to the DUT pins.

c. *Test the power supply.* The actual start of parametric testing is the power supply test. The system checks to see if an entry is specified in the TEST LIMIT (li) field of the parameters screen. If there is, the system runs through the truth table, starting at step 0, until it reaches the step specified in the SUPPLIES STEP field of the parameters screen. If no value was entered for the TEST LIMIT, the power supply won't be tested in that group. This is done independently of the parametric test start and stop steps entered in the alternate parameters screen.

Assuming that there was a value entered for the TEST LIMIT and a step specified for power supply testing, and that the system has stepped through the truth table to that step, the following procedure is performed. The DUT pins are set to the levels specified in the functional test conditions column of the parameters screen for the group where the power supply test is being performed. However, all out-

put pins that are assigned "X" (don't care) are temporarily unloaded. (See **Truth Table Screen** above.)

d. *Cycle the DUT through the truth table.* The system resets the truth table step to 0000 and steps forward at the functional test rate until the parametric test start step for the group being tested is reached. The system will then begin to search for the appropriate logic state on the pin to be tested, cycling through as many more steps as necessary until the pin of interest is in the appropriate state for the test that is to be performed. Any functional errors are ignored. The truth-table data stored in the RAM on the driver/sensor board are used to place the appropriate functional logic level at each pin of the DUT.

The sequence in which parametric measurements are performed is the same as the order of their appearance on the parameters screen (IIL, IIH, VOL, VOH, IZL, IZH, and finally IOS). One parameter is measured at all appropriate pins, beginning with the lowest numbered pin having the function being tested (input or output) and continuing through to the highest numbered pin. After each pin is tested, the system resets the truth table step to 0000. This resetting is done in order to insure that devices with bidirectional pins and devices requiring initialization are in the proper states when tested.

A specific parametric test will not be performed if either the test limit or parametric test condition is not entered in the parameters screen of the test group being performed. Also, parametric testing in any group will be performed only if enabled under at least one bin in the run-mode screen. If the pin state to be tested does not appear within the section of the truth table where parametric testing is enabled, the parametric test for that logic state will not be performed on the pin. In such a case, the system will reset the truth table step to 0000 and attempt to perform the same parametric test on the next pin with the same function. If the pin that was unsuccessfully tested was the last pin to be tested for that parameter, the system will start testing for the next parameter.

e. *Disconnect the functional levels and then connect the parametric measurement unit to the pin under test.* Once the device has been cycled to the correct logic state as defined in the truth table, the parametric measurement unit is connected to the pin under test, replacing the functional drive/sense circuitry for that pin on the appropriate driver/sensor board. The functional levels remain at the other input and output pins in order to prevent the device from changing state.

f. *Make the parametric measurement.* The parametric measurement unit forces a voltage or current and measures the resulting current or voltage, whichever is required by the particular parameter being measured. The parametric board uses its digital voltmeter to measure the voltage of the desired parameter and returns the result along the same path that the inputs to the parametric board followed. The Z80 makes the appropriate calculations and comparisons, converts the data to floating-point format (usually), and stores the results in memory. If the selected display mode option is Pass/Fail/Bin, the Z80 will not perform floating-point conversion but will compare the binary result to the binary value stored in memory. It then searches for the next pin to be measured for the same parameter and restarts testing at the beginning of the truth table.

g. *Compare the measured value with the parametric limit and determine whether the parametric test passes.* The system will compare the result of each test on each pin with the values stored in memory. If there is a parametric failure on any pin, a flag is set. Testing will continue until all tests specified for the group being tested have been performed. Once all testing for the group has been completed, if the test program includes the selection of ALL GROUPS FIRST FAILURE or TEST CONTINUOUSLY TO FAILURE in the run-mode screen, the flag set by the parametric failure causes the system to terminate the test program.

If no failure was detected, the system continues the parametric test until it is completed. Once all pins have been measured for a parameter, the parameters screen is searched for the next listed parametric test condition and parametric test limit and the system repeats the parametric test procedure. When all parameters listed on both parameters screens have been tested for each group that has parametric tests enabled in one or more bins on the run-mode screen, the parametric test is complete.

h. *Display the results.* Once all testing is terminated, the parametric-results screen, results-summary screen, or a pass/fail screen will be displayed.

6.3.2 Parametric Measurement Unit Functions Figures 6-5 through 6-7

The parametric measurement unit (sometimes referred to as the parametric head) performs two basic operations as it makes parametric tests. It either forces voltage and measures current (V-FORCE mode) or forces current and measures voltage (I-FORCE mode). These operations will be described below. The parametric measurement unit is connected to the DUT pin of interest through PARACUR and PARASENSE lines, as shown in the simplified schematic diagram. These lines are bused to all of the driver/sensor boards. Each driver/sensor board has 8 drive/sense circuits and the DUT interface to each of them takes place at a Kelvin junction close to a DUT pin. This junction includes both drive and sense lines.

To put the operation of the parametric measurement unit into context, consider what happens when the system performs first a functional test and then a parametric test. If the test to be performed was a functional test, the drive and sense lines would remain connected to the driver/sensor throughout the test, and the parametric measurement unit would not be used. During a parametric test, however, the pin of interest is first driven to the correct step in the truth table by the driver/sensor lines. Once the pin of interest is at the proper logic state for the test to be made, it is switched to the PARACUR and PARASENSE lines. At this point, the parametric head makes the measurement called for, either forcing voltage and measuring current or forcing current and measuring voltage, whichever is required by the particular test. After the measurement, the pin is switched back to the driver/sensor lines, and the test program continues.

V-FORCE mode. V-FORCE (voltage force) produces an I-MEAS output (a signal voltage that is proportional to current). The 12-bit D/A converter receives data from the CPU bus and translates this information into a voltage, which is fed into the V RANGE SELECTOR. This selector has three ranges, in decreasing order of sensitivity: -1 to +1 V, -4 to

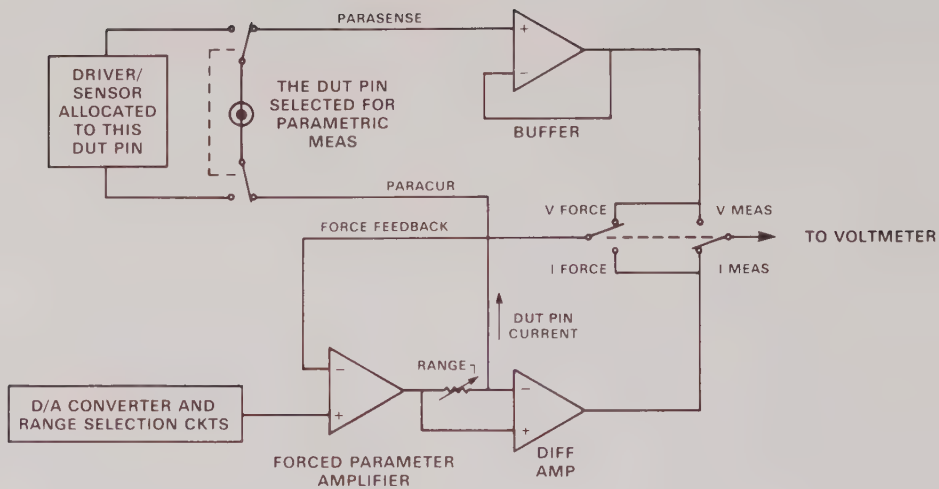


Figure 6-5. Parametric measurement unit, simplified schematic diagram.

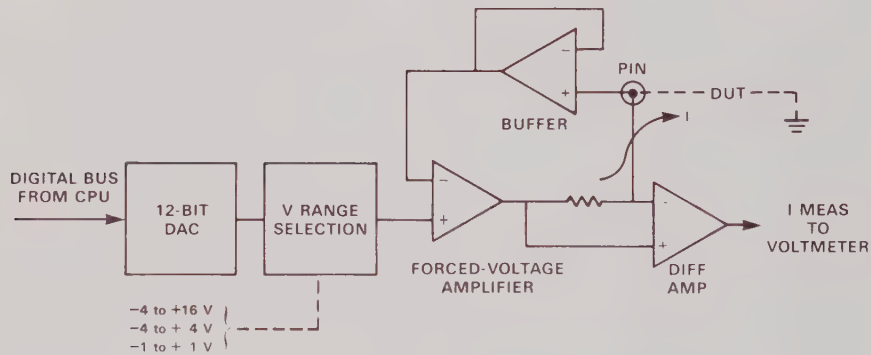


Figure 6-6. Parametric measurement unit, simplified to show voltage-force current-measure functions.

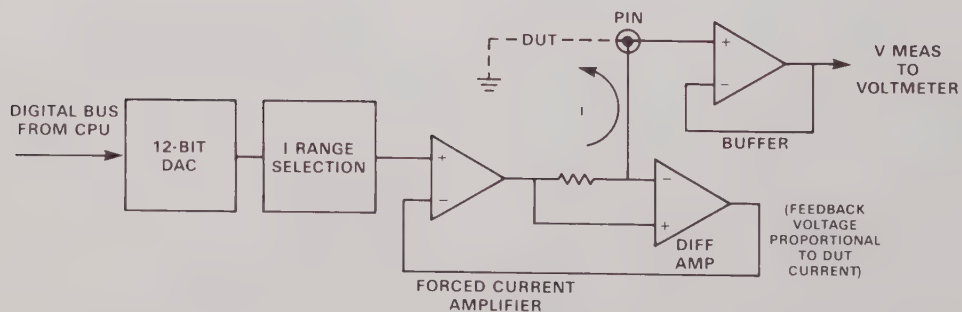


Figure 6-7. Parametric measurement unit, simplified to show current-force voltage-measure functions.

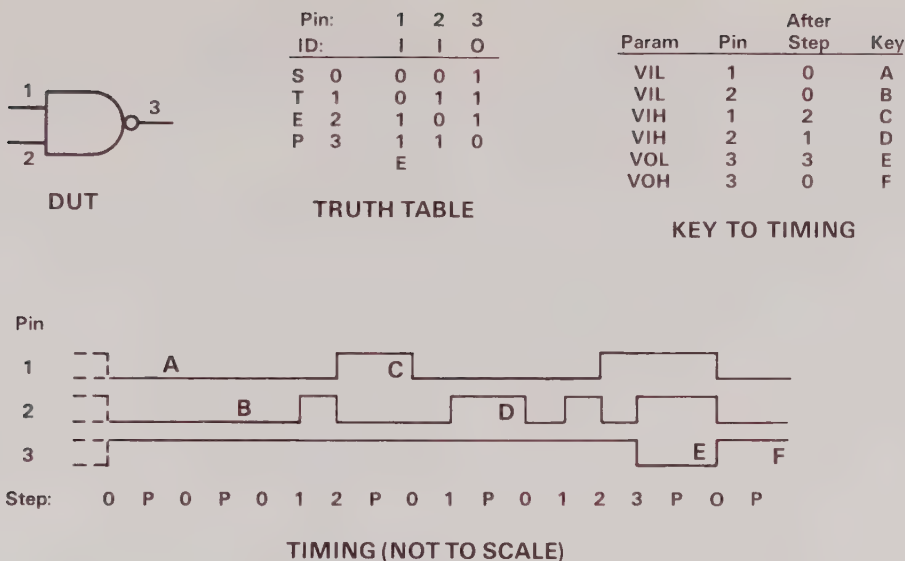


Figure 6-8. Parametric test procedure, example for a single gate.

+4 V, and -4 to +16 V. In V-FORCE mode, the parametric head acts like a big op-amp feedback loop. The current flowing in the circuit to the DUT pin is sensed by a differential amplifier as it flows through the R SENSE resistor. The current flow through R SENSE develops voltage V SENSE, which is applied to the inputs of the differential amplifier; the output of the differential amplifier is called I MEAS and is sent to the voltmeter. From I MEAS and the value of resistance, RSENSE, the CPU calculates the current value.

I-FORCE mode. I-FORCE (current force) produces a V-MEAS output, which is a signal voltage. The D/A converter and V-RANGE SELECTOR perform in the same manner as they would for the V-FORCE Mode. The difference here is that the current, rather than the voltage, is forced to agree with the prescribed condition. The output voltage from the V-RANGE SELECTOR is maintained across R SENSE, using the feedback loop. The voltage at the DUT pin is sensed by the buffer and sent to the voltmeter as V MEAS and then, in digital form, to the CPU.

6.3.3 I-max Interaction with Range Selection

There is an interaction between the value of I-max and the accuracy of the corresponding current test limit measurement. It is possible to achieve even greater accuracy for power-supply current test measurement by the use of a separate group and the specification of a lower value of I-max than that used during the parametric and functional testing. The I-max shutdown circuitry and the current test limit measurement circuitry share a common range measurement impedance. This impedance is set by the system software according to the value entered for I-max in the parameters screen of the group being tested. Each power supply has three ranges; the lower ranges have greater resolution than the higher ranges. The system automatically uses the lowest range that contains I-max. Therefore, for the test group in which the power-supply current limit is to be tested and in which the output current

loads are kept suitably small, select a value for I-max that falls within a range that has acceptable resolution.

The ranges for the supplies can be found in the DUT Power Supply tables of the system specifications.

6.3.4 Example of Parametric Test

Figure 6-8

The figure shows a device and the test steps used to perform the parametric test. The parameters screen is set up so that the test will begin with the IIL test. The truth table indicates that pin 1 is an input, so the truth table is searched for the first instance where pin 1 goes low — in this case, step 0. This is done, as mentioned before, so that the device will be in the proper state when the measurement is taken. The low level (VIL) indicated in the truth table is set up in the parametric measurement unit, which is connected to pin 1 to make an IIL measurement.

The next pin indicated by the describe screen as an input is pin 2. The test will return to step 0 and begin again from there in order to insure the device is in the proper state when the test has cycled to step 0, where the IIL measurement on pin 2 will be taken.

The system finds no other pins listed on the describe screen to be tested for IIL, so the next test will be for IIH. The system returns to step 0 of the truth table and begins the test from the start of the truth table, cycling at the functional-test rate past the parametric-test start step to the first step where pin 1 goes high. The parametric head will be connected, a VIH will be forced parametrically, and the IIH measurement will be made. The system will restart at step 0, test IIH at pin 2, and continue on.

Once all the input pins have been tested, the system will begin to check the output pins for VOL and VOH. Pin 3 is the first output; when the test reaches step 3, the system will force IOL parametrically and measure VOL. After the system has verified that there are no other output pins to check for VOL, it will begin to check for VOH. Pin 3 will be checked at step 0, the first step where a high output occurs.

6.4 CONTINUITY TESTING

Continuity tests are performed by the parametric unit once each time a program is executed (unless they are omitted from the test program in the run-mode screen). The continuity test is performed, prior to any other testing, in the first group that has either a parametric or functional test enabled, without regard to the truth table, and is the only test that can run without a valid truth table residing in memory. It automatically checks all power-supply, input, output, tristate, and bidirectional pins. Only one pin is checked for continuity at a time; all other DUT pins are disconnected from both the parametric measurement unit and the driver/sensor lines. A pin is checked by sinking from or sourcing to it a current of 100 μA and checking whether the voltage is 2.5 V dc or less, indicating conti-

nuity. If the voltage is not greater than 2.5 V dc, the pin passes the continuity test.

Each power-supply pin is checked with 1.6 mA in the appropriate direction; all other active pins are checked with 0.1 mA in each direction (either direction is sufficient for a "pass").

For the power-supply continuity test, the current is forced in the direction defined by the power supply selected for that pin. During the test, the system acts as current source and sink; the test normally feeds current through an inherent semiconductor junction (the protection circuitry) in the DUT. If there are no such current paths at certain device pins, continuity testing should be omitted. If continuity testing must be performed, "protection" diodes should be provided in the socket adaptor. The diodes should be installed with the cathode connected to the DUT pin and the anode connected to the socket adaptor driver/sensor connector. This will allow valid continuity tests to be performed.

6.5 KELVIN TESTING

Basically, the Kelvin connection at every pin is checked by activating both drive and sense (functional test) circuits associated with that pin. Schematically (see Figure 6-2), the test is performed with both "S1" and "S2" closed. The Kelvin check passes if the circuit is complete from "S1" through the Kelvin connection at or near the pin to "S2".

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Index to Device Programs and Adaptors for GR 1732 Digital IC Test System

Form 1732-0124-04

NOTE

Due to the dynamic nature of the 1732 program library, this index will be revised periodically. Contact your local GenRad office for updates.

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NOTE

References to K and non-K socket adaptors refer to Kelvin and non-Kelvin models, respectively. Kelvin systems include those numbered 1732-9720 through 1732-9724, 1732-9730 through 1732-9734, and 1732-9740 through 1732-9744. Non-Kelvin systems are those numbered 1732-9700 through 1732-9704. The number is located on the rear panel.

Revision Date: 06 September 1983

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INTRODUCTION

In Lists A through F, the information is arranged as follows:

Device Type/Device Description.

The first column lists the type number or name of the device to be tested (DUT). The second column provides a brief description of the device.

Program Tape Number/Order Number.

The third column lists the name of the tape cassette(s) containing the test program for the device listed in column 1. The fourth column contains the suffix (the prefix is 1732-) of the order number for the tape.

Socket Adaptor (K/non-K).

The fifth column contains the suffix (again, the prefix is 1732-) of the part number for the manual-test adaptors (i.e. no automatic device handler in use). The first number in this column is the Kelvin adaptor - the second is the non-Kelvin adaptor. Refer to the adaptor wiring manual (Form 1732-1820) for assembly instructions for the adaptors listed in lists A through D. Instructions for LSI adaptors (lists E and F) are included as part of the order number in column 4.

2-Cable Handler Contactor Board.

The sixth column lists the 2-cable handler contactor board for Kelvin and non-Kelvin systems. This information applies only if the test system is set up with an automatic parts handler and uses two ribbon cables from the handler adaptor (at the test head) to the contactor (at the handler).

5-Cable Handler Adaptor.

The seventh column lists the 5-cable handler adaptors for EMS and MCT (the first of the two numbers) and Trigon handlers (the second number). This information applies only to Kelvin test systems interfaced via five ribbon cables to those handlers. For a complete description of this interface, refer to the handler interface manual (Form 1732-1819). For assembly instructions for the adaptors listed in this column, refer to the handler adaptor library manual (Form 1732-1823).

NOTE 1

Where a single number appears followed by (NOTE1) in the seventh column, the number refers to a jumper board which must be installed on adaptor board 1732-9604 (MCT/EMS) or 1732-9619 (Trigon).

NOTE 2

Where a single number appears followed by (NOTE2) in the "MCT/Trigon" column, the number refers to a jumper board which must be installed on adaptor board 1732-4717 (MCT/EMS) or 1732-4619 (Trigon) and used with the RAM adaptor (1732-9645) and static RAM adaptor (1732-9616).

NOTE 3

Where a single number appears followed by (NOTE3) in the seventh column, the number refers to a jumper board which must be installed on adaptor board 1732-4717 (MCT/EMS) or 1732-4619 (Trigon) and used with the RAM adaptor (1732-9645) and dynamic RAM adaptor (1732-9617).

LIST A. 7400-SERIES TTL DEVICES.

Cartridge Designations: T1, T2, LST1, LST2, ST1, ST2, etc.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
7400	QUAD 2-INPUT POSITIVE NAND	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS00	QUAD 2-INPUT NAND GATE	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S00	QUAD 2-INPUT NAND GATE	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7401	QUAD 2-INPUT POS NAND (O-C)	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS01	QUAD 2-INPUT NAND GATE (O-C)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
7402	QUAD 2-INPUT POSITIVE NOR	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS02	QUAD 2-INPUT NOR GATE	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S02	QUAD 2-INPUT POSITIVE NOR	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7403	QUAD 2-INPUT POS NAND (O-C)	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS03	QUAD 2-INPUT NAND GATE (O-C)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S03	QUAD 2-INPUT POS NAND (O-C)	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7404	HEX INVERTER	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS04	HEX INVERTER	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S04	HEX INVERTER	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7405	HEX INVERTER (O-C)	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS05	HEX INVERTER (O-C)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S05	HEX INVERTER (O-C)	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7408	QUAD 2-INPUT POSITIVE AND	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS08	QUAD 2-INPUT AND GATE	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S08	QUAD 2-INPUT POSITIVE AND	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7409	QUAD 2-INPUT POSITIVE AND (O-C)	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS09	QUAD 2-INPUT AND GATE (O-C)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S09	QUAD 2-INPUT POSITIVE AND (O-C)	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7410	TRIPLE 3-INPUT POSITIVE NAND	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS10	TRIPLE 3-INPUT NAND GATE	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S10	TRIPLE 3-INPUT POSITIVE NAND	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
74H11	TRIPLE 3-INPUT POSITIVE AND	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS11	TRIPLE 3-INPUT AND GATE	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S11	TRIPLE 3-INPUT POSITIVE AND	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7412	TRIPLE 3-INPUT POS NAND (O-C)	T1	9400	5938/5900	5837/5838	4634(NOTE1)

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
74LS12	TRIPLE 3-INPUT NAND GATE (O-C)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
7413	DUAL 4-INPUT POS NAND (SCHMITT)	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS13	DUAL 4-INPUT NAND (SCHMITT)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
7414	HEX INVERTER (SCHMITT)	T1	9400	5938/5900	5937/5838	4634(NOTE1)
74LS14	HEX INVERTER (SCHMITT)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74H15	TRIPLE 3-INPUT POS AND (O-C)	T1	9400	5938/5900	5837/5838	4634(NOTE1)
74LS15	TRIPLE 3-INPUT AND GATE (O-C)	LST1	9473	5938/5900	5837/5838	4634(NOTE1)
74S15	TRIPLE 3-INPUT POS AND (O-C)	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7416	HEX INVERTER	T1	9400	5938/5900	5837/5838	4634(NOTE1)
7417	HEX BUFFER (O-C)	T2	9401	5938/5900	5837/5838	4634(NOTE1)
7420	DUAL 4-INPUT POSITIVE NAND	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS20	DUAL 4-INPUT NAND GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
74S20	DUAL 4-INPUT POSITIVE NAND	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
74H21	DUAL 4-INPUT POSITIVE AND	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS21	DUAL 4-INPUT AND GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
7422	DUAL 4-INPUT POS NAND (O-C)	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS22	DUAL NAND GATE (O-C)	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
74S22	DUAL 4-INPUT POS NAND (O-C)	ST1	9484	5938/5900	5837/5838	4634(NOTE1)
7423	EXP DUAL 4-INPUT POSITIVE NOR	T2	9401	5962/5901	5822/5821	4635(NOTE1)
7425	DUAL 4-INPUT POSITIVE NOR W/STR	T2	9401	5938/5900	5837/5838	4634(NOTE1)
7426	QUAD 2-INPUT POS NAND (O-C)	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS26	QUAD 2-INPUT NAND GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
7427	TRIPLE 3-INPUT POSITIVE NOR	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS27	TRIPLE 3-INPUT NOR GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
7428	QUAD 2-INPUT POSITIVE NOR	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS28	QUAD 2-INPUT NOR GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
7430	8-INPUT POSITIVE NAND	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS30	8-INPUT NAND GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
74S30	8-INPUT POSITIVE NAND	ST2	9485	5938/5900	5837/5838	4634(NOTE1)
7432	QUAD 2-INPUT POSITIVE OR	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS32	QUAD 2-INPUT OR GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
74S32	QUAD 2-INPUT POSITIVE OR	ST2	9485	5938/5900	5837/5838	4634(NOTE1)
7433	QUAD 2-INPUT POSITIVE NOR (O-C)	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS33	QUAD 2-INPUT NOR GATE (O-C)	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
7437	QUAD 2-INPUT NAND	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS37	QUAD 2-INPUT NAND GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
74S37	QUAD 2-INPUT POSITIVE NAND	ST2	9485	5938/5900	5837/5838	4634(NOTE1)
7438A	QUAD 2-INPUT POS NAND (O-C)	T2	9401	5938/5900	5837/5838	4634(NOTE1)
74LS38	QUAD NAND GATE (O-C)	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
74S38	QUAD NAND BUFFER (O-C)	ST2	9485	5938/5900	5837/5838	4634(NOTE1)
74LS40	DUAL 4-INPUT NAND GATE	LST2	9474	5938/5900	5837/5838	4634(NOTE1)
74S40	DUAL 4-INPUT NAND GATE	ST2	9484	5938/5900	5837/5838	4634(NOTE1)
7442A	BCD TO DEC CONVERTER	T3	9402	5962/5901	5822/5821	4635(NOTE1)
74LS42	BCD TO DEC CONVERTER	LST3	9475	5962/5901	5822/5821	4635(NOTE1)
7445	BCD TO DEC DECODER/DRIVER (O-C)	T3	9402	5962/5901	5822/5821	4635(NOTE1)

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
7446A	BCD-7-SEG DECODER/DRVR (O-C)	T3	9402	5962/5901	5822/5821	4635(NOTE 1)
7447A	BCD-7-SEG DECODER/DRVR (O-C)	T3	9402	5962/5901	5822/5821	4635(NOTE 1)
74LS47	BCD TO 7-SEGMENT DRIVER (O-C)	LST3	9475	5962/5901	5822/5821	4635(NOTE 1)
7448	BCD TO 7-SEGMENT DECODER/DRVR	T3	9402	5962/5901	5822/5821	4635(NOTE 1)
74LS48	BCD TO 7-SEGMENT DRIVER	LST3	9475	5962/5901	5822/5821	4635(NOTE 1)
7450	DUAL 2X2 AND-OR-INVERTER	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
7451	3X3, 2X2 AND-OR-INVERTER	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
74LS51	DUAL 2X2 AND-OR-INVERT	LST3	9475	5938/5900	5837/5838	4634(NOTE 1)
74S51	DUAL 2X2 AND-OR-INVERT	ST2	9485	5938/5900	5837/5838	4634(NOTE 1)
74H52	AND-OR-INVERTER	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
7453	AND-OR-INVERTER EXPANDABLE	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
74H53	AND-OR-INVERTER EXPANDABLE	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
7454	AND-OR-INVERTER	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
74LS54	AND-OR-INVERTER	LST3	9475	5938/5900	5837/5838	4634(NOTE 1)
74H55	AND-OR-INVERTER	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
74LS55	AND-OR-INVERTER EXPANDABLE	LST3	9475	5938/5900	5837/5838	4634(NOTE 1)
7460	DUAL EXPANDER	T3	9402	5951/5910	N.A.	5785/5786
74H61	TRIPLE EXPANDER	T3	9402	5938/5900	5837/5838	4634(NOTE 1)
74H62	AND-OR EXPANDER	T3	9402	5945/5909	N.A.	5773/5774
74S64	4-2-3-2 AND-OR-INVERTER	ST2	9485	5938/5900	5837/5838	4634(NOTE 1)
7470	GATED J-K FLIP/FLOP	T4	9403	5938/5900	5837/5838	4634(NOTE 1)
74H71	GATED J-K FLIP/FLOP	T4	9403	5938/5900	5837/5838	4634(NOTE 1)
7472	GATED J-K FLIP/FLOP	T4	9403	5938/5900	5837/5838	4634(NOTE 1)
74LS73A	DUAL J-K FLIP/FLOP	LST3	9475	5952/5906	5825/5826	5502(NOTE 1)
* 7474	DUAL D-TYPE FLIP/FLOP	T4	9403	5938/5900	5837/5838	4634(NOTE 1)
* 74LS74A	DUAL D-TYPE FLIP-FLOP	LST3	9475	5938/5900	5837/5838	4634(NOTE 1)
74S74	DUAL D-TYPE FLIP-FLOP	ST2	9485	5881/5882	5837/5884	5745/5746
7475	4-BIT LATCH	T4	9403	5936/5907	5823/5824	5503(NOTE 1)
74LS75	4-BIT BISTABLE LATCH	LST3	9475	5936/5907	5823/5824	5503(NOTE 1)
7476	DUAL J-K FLIP/FLOP	T4	9403	5939/5908	5829/5830	5504(NOTE 1)
74LS76A	DUAL J-K FLIP-FLOP	LST3	9475	5939/5908	5829/5830	5504(NOTE 1)
74LS78A	DUAL J-K FLIP/FLOP	LST3	9475	5952/5906	5825/5826	5502(NOTE 1)
7480	GATED FULL ADDER	T4	9403	5938/5900	5837/5838	4634(NOTE 1)
7483A	4-BIT FULL ADDER	T4	9403	5936/5907	5823/5824	5503(NOTE 1)
74LS83A	4-BIT FULL ADDER	LST3	9475	5936/5907	5823/5824	5503(NOTE 1)
7485	4-BIT MAGNITUDE COMP	T5	9404	5962/5901	5822/5821	4635(NOTE 1)
74LS85	4-BIT MAGNITUDE COMPARATOR	LST4	9476	5962/5901	5822/5821	4635(NOTE 1)
74S85	4-BIT MAGNITUDE COMPARATOR	ST2	9485	5962/5901	5822/5821	4635(NOTE 1)
7486	QUAD 2-INPUT EXCLUSIVE OR	T5	9404	5938/5900	5837/5838	4634(NOTE 1)
74LS86	QUAD 2-INPUT EXCLUSIVE OR	LST4	9476	5938/5900	5837/5838	4634(NOTE 1)
74S86	QUAD 2-INPUT EXCLUSIVE OR	ST2	9485	5938/5900	5837/5838	4634(NOTE 1)
74H87	4-BIT TRUE/COMP 0/1 ELEMENT	T5	9404	5938/5900	5837/5838	4634(NOTE 1)
7490A	DECADE COUNTER	T5	9404	5946/5912	5841/5842	5503(NOTE 1)
74LS90	DECADE COUNTER	LST4	9476	5946/5912	5841/5842	5503(NOTE 1)
7491A	8-BIT SHIFT REGISTER	T5	9404	5946/5912	5841/5842	5503(NOTE 1)

* This device may also be tested on adaptors listed for its "S" series counterpart.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
74LS91	8-BIT SHIFT REGISTER	LST4	9476	5946/5912	5841/5842	5503 (NOTE 1)
7492A	DIVIDE BY 12	T5	9404	5946/5912	5841/5842	5503 (NOTE 1)
74LS92	DIVIDE BY 12	LST4	9476	5946/5912	5841/5842	5503 (NOTE 1)
7493A	4-BIT BINARY COUNTER	T5	9404	5946/5912	5841/5842	5503 (NOTE 1)
74LS93	4-BIT BINARY COUNTER	LST4	9476	5946/5912	5841/5842	5503 (NOTE 1)
7494	4-BIT SHIFT REGISTER	T5	9404	5936/5907	5823/5824	5503 (NOTE 1)
7495A	4-BIT SHIFT REGISTER	T5	9404	5938/5900	5837/5838	4634 (NOTE 1)
74LS95B	4-BIT SHIFT REGISTER	LST4	9476	5938/5900	5837/5838	4634 (NOTE 1)
7496	5-BIT SHIFT REGISTER	T5	9404	5936/5907	5823/5824	5503 (NOTE 1)
74LS96	5-BIT SHIFT REGISTER	LST4	9476	5936/5907	5823/5824	5503 (NOTE 1)
7497	6-BIT RATE MULT	T6	9405	5962/5901	5822/5821	4635 (NOTE 1)
74L98	4-BIT SELECTOR/STORAGE REG	T6	9405	5962/5901	5822/5821	4635 (NOTE 1)
74100	DUAL 4-BIT LATCH	T6	9405	5942/5920	N.A.	5767/5768
74H103	DUAL J-K FLIP/FLOP	T6	9405	5952/5906	5825/5826	5502 (NOTE 1)
74H106	DUAL J-K FLIP/FLOP	T6	9405	5939/5908	5829/5830	5504 (NOTE 1)
74107	DUAL J-K M-S FLIP/FLOP	T6	9405	5938/5900	5837/5838	4634 (NOTE 1)
74LS107ADUAL	J-K FLIP-FLOP MASTER/SLAVE	LST4	9476	5938/5900	5837/5838	4634 (NOTE 1)
74109	DUAL J-K FLIP/FLOP	T6	9405	5962/5901	5822/5821	4635 (NOTE 1)
74LS109ADUAL	J-K FLIP-FLOP EDGE-TRIG	LST4	9476	5962/5901	5822/5821	4635 (NOTE 1)
74110	GATED M-S FLIP/FLOP	T6	9405	5938/5900	5837/5838	4634 (NOTE 1)
74111	DUAL J-K M-S FLIP/FLOP	T6	9405	5962/5901	5822/5821	4635 (NOTE 1)
* 74LS112ADUAL	J-K FLIP-FLOP	LST5	9477	5962/5901	5822/5821	4635 (NOTE 1)
74S112	DUAL J-K FLIP-FLOP	ST3	9486	5843/5844	5822/5846	5729/5730
74LS113ADUAL	J-K FLIP-FLOP	LST5	9477	5938/5900	5837/5838	4634 (NOTE 1)
* 74LS114ADUAL	J-K FLIP-FLOP	LST5	9477	5938/5900	5837/5838	4634 (NOTE 1)
74S114	DUAL J-K FLIP-FLOP	ST3	9486	5851/5852	5837/5854	5733/5734
74116	DUAL 4-BIT LATCH	T7	9406	5953/5902	5879/5880	5789/5790
74120	DUAL PULSE SYNCHRONIZER/DRIVER	T7	9406	5962/5901	5822/5821	4635 (NOTE 1)
74121	MONOSTABLE MULTIVIBRATOR	T7	9406	5935/5915	N.A.	5753/5754
74122	MONOSTABLE MULTIVIBRATOR	T7	9406	5943/5914	N.A.	5769/5770
74LS122	RETRIG. MONOSTABLE MULTIV.	LST5	9477	5863/5864	5865/5866	5739/5740
74123	DUAL MONOSTABLE MULTIVIBRATOR	T7	9406	5934/5916	5893/5894	5751/5752
74LS123	DUAL RETRIG. MONOSTABLE MULTIV.	LST5	9477	5859/5860	5861/5862	5737/5738
74125	QUAD BUS BUFFER (TRI-S)	T7	9406	5938/5900	5837/5838	4634 (NOTE 1)
74126	QUAD BUS BUFFER (TRI-S)	T7	9406	5938/5900	5837/5838	4634 (NOTE 1)
74132	QUAD NAND (SCHMITT)	T7	9406	5938/5900	5837/5838	4634 (NOTE 1)
74S132	QUAD NAND (SCHMITT)	ST3	9486	5938/5900	5837/5838	4634 (NOTE 1)
74S133	13-INPUT POSITIVE NAND	ST3	9486	5962/5901	5822/5821	4635 (NOTE 1)
74S134	12-INPUT POSITIVE NAND	ST3	9486	5962/5901	5822/5821	4635 (NOTE 1)
74S135	QUAD EXCLUSIVE-OR/NOR	ST3	9486	5962/5901	5822/5821	4635 (NOTE 1)
74136	QUAD 2-INPUT EXCLUSIVE OR	T7	9406	5938/5900	5837/5838	4634 (NOTE 1)
74LS136	QUAD EXCLUSIVE OR GATE	LST6	9478	5938/5900	5837/5838	4634 (NOTE 1)
74LS138	3-TO-8-LINE DECODER	LST6	9478	5962/5901	5822/5821	4635 (NOTE 1)
74S138	3-TO-8 LINE DECODER	ST3	9486	5962/5901	5822/5821	4635 (NOTE 1)
74LS139	DUAL 2-TO-4-LINE DECODER	LST6	9478	5962/5901	5822/5821	4635 (NOTE 1)

* This device may also be tested on adaptors listed for its "S" series counterpart.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
74S139	DUAL 2-TO-4 LINE DECODER	ST3	9486	5962/5901	5822/5821	4635(NOTE1)
74S140	4-INPUT NAND LINE DRIVER	ST3	9486	5938/5900	5837/5838	4634(NOTE1)
74145	BCD TO DEC DECODER/DRIVER	T8	9407	5962/5901	5822/5821	4635(NOTE1)
74LS145	BCD TO DEC DECODER/DRIVER	LST6	9478	5962/5901	5822/5821	4635(NOTE1)
74148	8-TO-3-LINE PRIORITY ENCODER	T8	9407	5962/5901	5822/5821	4635(NOTE1)
74LS148	8-TO-3 LINE PRIORITY ENCODER	LST6	9478	5962/5901	5822/5821	4635(NOTE1)
74150	1 OF 16 MUX	T8	9407	5953/5902	5879/5880	5789/5790
74151	1 OF 8 MUX	T8	9407	5962/5901	5822/5821	4635(NOTE1)
74LS151	1-OF-8 MULTIPLEXER	LST6	9478	5962/5901	5822/5821	4635(NOTE1)
74S151	1-OF-8 MULTIPLEXER	ST3	9486	5962/5901	5822/5821	4635(NOTE1)
74152	1 OF 8 MUX	T8	9407	5938/5900	5837/5838	4634(NOTE1)
74153	DUAL 1 OF 4 MULTIPLEXER	T8	9407	5962/5901	5822/5821	4635(NOTE1)
74LS153	DUAL 1-OF-4 MULTIPLEXER	LST6	9478	5962/5901	5822/5821	4635(NOTE1)
74S153	DUAL 1-OF-4 MULTIPLEXER	ST4	9487	5962/5901	5822/5821	4635(NOTE1)
74154	4-TO-16-LINE DECODER	T8	9407	5953/5902	5879/5880	5789/5790
74155	DUAL 2-TO-4-LINE DECODER	T8	9407	5962/5901	5822/5821	4635(NOTE1)
74LS155	DUAL 2-TO-4 LINE DECODER	LST6	9478	5962/5901	5822/5821	4635(NOTE1)
74156	DUAL 2-TO-4-LINE DECODER (O-C)	T8	9407	5962/5901	5822/5821	4635(NOTE1)
74LS156	DUAL 2-TO-4 LINE DECODER (O-C)	LST6	9478	5962/5901	5822/5821	4635(NOTE1)
74157	QUAD 2 TO 1 MULTIPLEXER	T9	9408	5962/5901	5822/5821	4635(NOTE1)
74LS157	QUAD 2-TO-1 MULTIPLEXER	LST6	9478	5962/5901	5822/5821	4635(NOTE1)
74S157	QUAD 2-TO-1 MULTIPLEXER	ST4	9487	5962/5901	5822/5821	4635(NOTE1)
74LS158	QUAD 2 TO 1 MULTIPLEXER	LST7	9479	5962/5901	5822/5821	4635(NOTE1)
74S158	QUAD 2-TO-1 MULTIPLEXER	ST4	9487	5962/5901	5822/5821	4635(NOTE1)
74159	4 TO 16 DECODER	T9	9408	5953/5902	5879/5880	5789/5790
74160	DECADE COUNTER	T9	9408	5962/5901	5822/5821	4635(NOTE1)
74LS160A	4-BIT SYNCH. DECADE COUNTER	LST7	9479	5869/5870	5871/5872	5741/5742
74161A	BINARY COUNTER	T9	9408	5962/5901	5822/5821	4635(NOTE1)
74LS161A	4-BIT SYNCH. BINARY COUNTER	LST7	9479	5869/5870	5871/5872	5741/5742
74S161	4-BIT SYNCH. BINARY COUNTER	ST4	9487	5869/5870	5871/5872	5741/5742
74162	DECADE COUNTER	T9	9408	5962/5901	5822/5821	4635(NOTE1)
74LS162A	4-BIT SYNCH. DECADE COUNTER	LST7	9479	5869/5870	5871/5872	5741/5742
74S162	4-BIT SYNCH. DECADE COUNTER	ST4	9487	5869/5870	5871/5872	5741/5742
74163	BINARY COUNTER	T9	9408	5962/5901	5822/5821	4635(NOTE1)
74LS163A	4-BIT SYNCH. BINARY COUNTER	LST7	9479	5869/5870	5871/5872	5741/5742
74S163	4-BIT SYNCH. BINARY COUNTER	ST4	9487	5869/5870	5871/5872	5741/5742
74164	8-BIT SHIFT REG PARALLEL OUT	T9	9408	5938/5900	5837/5838	4634(NOTE1)
74LS164	8-BIT SHIFT REG PARALLEL OUT	LST7	9479	5938/5900	5837/5838	4634(NOTE1)
74165	8-BIT SHIFT REG PARALLEL IN	T9	9408	5962/5901	5822/5821	4635(NOTE1)
74LS165	8-BIT SHIFT REG PARALLEL IN	LST7	9479	5962/5901	5822/5821	4635(NOTE1)
74166	8-BIT SHIFT REG PARALLEL IN	T9	9408	5962/5901	5822/5821	4635(NOTE1)
74LS166	8-BIT SHIFT REG PARALLEL I/O	LST7	9479	5962/5901	5822/5821	4635(NOTE1)
74S169	BINARY COUNTER	ST4	9487	5869/5870	5871/5872	5741/5742
74170	4X4 REGISTER FILE	T10	9409	5962/5901	5822/5821	4635(NOTE1)
74LS170	4X4 REGISTER FILE (O-C)	LST7	9479	5962/5901	5822/5821	4635(NOTE1)

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/ Trigon
74172	16-BIT REGISTER FILE	T10	9409	5953/5902	5879/5880	5789/5790
74173	4-BIT D-TYPE FLIP/FLOP (TRI-S)	T10	9409	5962/5901	5822/5821	4635 (NOTE 1)
74LS173	4-BIT D-TYPE REGISTER (TRI-S)	LST7	9479	5962/5901	5822/5821	4635 (NOTE 1)
* 74174	HEX D-TYPE FLIP-FLOP	T10	9409	5962/5901	5822/5821	4635 (NOTE 1)
* 74LS174	HEX D-TYPE FLIP-FLOP	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
74S174	HEX D-TYPE FLIP-FLOP	ST4	9487	5833/5834	5822/5836	5727/5728
* 74175	QUAD D-TYPE FLIP-FLOP	T10	9409	5962/5901	5822/5821	4635 (NOTE 1)
* 74LS175	QUAD D-TYPE FLIP-FLOP	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
74S175	QUAD D-TYPE FLIP-FLOP	ST4	9487	5833/5834	5822/5836	5727/5728
74176	DECADE COUNTER	T10	9409	5938/5900	5837/5838	4634 (NOTE 1)
74177	BINARY COUNTER	T10	9409	5938/5900	5837/5838	4634 (NOTE 1)
74180	PARITY GENERATOR	T10	9409	5938/5900	5837/5838	4634 (NOTE 1)
74181	ARITHMETIC LOGIC UNIT	T10	9409	5953/5902	5879/5880	5789/5790
74LS181	ARITHMETIC LOGIC UNIT	LST8	9480	5953/5902	5879/5880	5789/5790
74S181	ARITHMETIC LOGIC UNIT	ST4	9487	5953/5902	5879/5880	5789/5790
74182	LOOK-AHEAD CARRY GENERATOR	T10	9409	5962/5901	5822/5821	4635 (NOTE 1)
74S182	LOOK-AHEAD CARRY GENERATOR	ST4	9487	5962/5901	5822/5821	4635 (NOTE 1)
74H183	DUAL FULL ADDER	T11	9410	5938/5900	5837/5838	4634 (NOTE 1)
74LS183	DUAL FULL ADDER	LST8	9480	5938/5900	5837/5838	4634 (NOTE 1)
74184	BCD TO BINARY CODE CONVERTER	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
74185	BINARY TO BCD CODE CONVERTER	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
74190	BCD UP/DOWN COUNTER	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
74LS190	BCD UP/DOWN COUNTER	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
74191	BINARY UP/DOWN COUNTER	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
74LS191	BINARY UP/DOWN COUNTER	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
74192	BCD UP/DOWN COUNTER	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
74LS192	BCD UP/DOWN COUNTER	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
74193	BINARY UP/DOWN COUNTER	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
74LS193	BINARY UP/DOWN COUNTER	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
* 74194	4-BIT BI-DIREC SHIFT REGISTER	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
* 74LS194	4-BIT BI-DIREC SHIFT REGISTER	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
74S194	4-BIT BI-DIREC SHIFT REGISTER	ST5	9488	5847/5848	5822/5850	5731/5732
* 74195	4-BIT PARALLEL ACCESS SHIFT REG	T11	9410	5962/5901	5822/5821	4635 (NOTE 1)
* 74LS195	4-BIT PARALLEL ACCESS SHIFT REG	LST8	9480	5962/5901	5822/5821	4635 (NOTE 1)
74S195	4-BIT PARALLEL ACCESS SHIFT REG	ST5	9488	5827/5828	5822/5840	5725/5726
* 74196	DECADE COUNTER	T12	9411	5938/5900	5837/5838	4634 (NOTE 1)
* 74LS196	DECADE COUNTER	LST9	9481	5938/5900	5837/5838	4634 (NOTE 1)
74S196	DECADE COUNTER/LATCH	ST5	9488	5873/5874	5837/5876	5743/5744
* 74197	BINARY COUNTER	T12	9411	5938/5900	5837/5838	4634 (NOTE 1)
* 74LS197	BINARY COUNTER/LATCH	LST9	9481	5938/5900	5837/5838	4634 (NOTE 1)
74S197	BINARY COUNTER/LATCH	ST5	9488	5873/5874	5837/5876	5743/5744
74198	8-BIT BI-DIREC SHIFT REGISTER	T12	9411	5953/5902	5879/5880	5789/5790
74199	8-BIT BI-DIRECTIONAL SHIFT REG	T12	9411	5953/5902	5879/5880	5789/5790
74221	DUAL MONOSTABLE MULTIVIBRATOR	T12	9411	5934/5916	5893/5894	5751/5752
74LS221	DUAL MONOSTABLE MULTIVIBRATOR	LST9	9481	5855/5856	5857/5858	5735/5736

* This device may also be tested on adaptors listed for its "S" series counterpart.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
74LS240	OCTAL BUFFER (TRI-S)	LST9	9481	5950/5911	5867/5868	5507(NOTE1)
74S240	OCTAL BUFFER DRVR/RCVR (TRI-S)	ST5	9488	5950/5911	5867/5868	5507(NOTE1)
74LS241	OCTAL BUFFER DRVR/RCVR (TRI-S)	LST9	9481	5950/5911	5867/5868	5507(NOTE1)
74S241	OCTAL BUFFER DRVR/RCVR (TRI-S)	ST5	9488	5950/5911	5867/5868	5507(NOTE1)
74LS244	OCTAL BUFFER DRVR/RCVR (TRI-S)	LST9	9481	5950/5911	5867/5868	5507(NOTE1)
74S244	OCTAL BUFFER (TRI-S)	ST5	9488	5950/5911	5867/5868	5507(NOTE1)
74LS245	OCTAL BUS TRANSCEIVER	LST9	9481	5950/5911	5867/5868	5507(NOTE1)
74251	1-OF-8 MULTIPLEXER (TRI-S)	T12	9411	5962/5901	5822/5821	4635(NOTE1)
74LS251	1-OF-8 MULTIPLEXER (TRI-S)	LST9	9481	5962/5901	5822/5821	4635(NOTE1)
74S251	1-OF-8 MULTIPLEXER (TRI-S)	ST5	9488	5962/5901	5822/5821	4635(NOTE1)
74LS253	DUAL 1-OF-4 MULTIPLEXER (TRI-S)	LST9	9481	5962/5901	5822/5821	4635(NOTE1)
74LS257A	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	LST9	9481	5962/5901	5822/5821	4635(NOTE1)
74LS258	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	LST10	9482	5962/5901	5822/5821	4635(NOTE1)
74S258	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	ST5	9488	5962/5901	5822/5821	4635(NOTE1)
74LS259	8-BIT ADDRESSABLE LATCH	LST10	9482	5962/5901	5822/5821	4635(NOTE1)
74S260	DUAL 5-INPUT POSITIVE NOR	ST5	9488	5938/5900	5837/5838	4634(NOTE1)
74265	QUAD COMPLEMENTARY-OUTPUT ELT.	T13	9412	5962/5901	5822/5821	4635(NOTE1)
74LS266	QUAD EXCLUSIVE OR	LST10	9482	5938/5900	5837/5838	4634(NOTE1)
74273	OCTAL D-TYPE FLIP/FLOP	T13	9412	5950/5911	5867/5868	5507(NOTE1)
74LS273	OCTAL D-TYPE FLIP-FLOP	LST10	9482	5950/5911	5867/5868	5507(NOTE1)
74276	QUAD J-K FLIP/FLOP	T13	9412	5950/5911	5867/5868	5507(NOTE1)
74278	4-BIT CASCADE PRIORITY REGISTER	T13	9412	5938/5900	5837/5838	4634(NOTE1)
74279	QUAD R-S LATCH	T13	9412	5962/5901	5822/5821	4635(NOTE1)
74LS279	QUAD S-R LATCH	LST10	9482	5962/5901	5822/5821	4635(NOTE1)
74LS280	9-BIT PARITY GENERATOR/CHECKER	LST10	9482	5938/5900	5837/5838	4634(NOTE1)
74S280	9-BIT PARITY GENERATOR	ST6	9489	5938/5900	5837/5838	4634(NOTE1)
74283	4-BIT FULL ADDER	T13	9412	5962/5901	5822/5821	4635(NOTE1)
74LS283	4-BIT BINARY FULL ADDER	LST10	9482	5962/5901	5822/5821	4635(NOTE1)
74S283	4-BIT FULL ADDER	ST6	9489	5962/5901	5822/5821	4635(NOTE1)
74293	4-BIT BINARY COUNTER	T13	9412	5938/5900	5837/5838	4634(NOTE1)
74LS293	4-BIT BINARY COUNTER	LST10	9482	5938/5900	5837/5838	4634(NOTE1)
74298	QUAD 1 OF 2 MUX/LATCH	T14	9413	5962/5901	5822/5821	4635(NOTE1)
* 74LS299	8-BIT BI-D SHIFT REGISTER	LST10	9482	5950/5911	5867/5868	5507(NOTE1)
74S299	8-BIT L/R SHIFT REGISTER	ST6	9489	5885/5886	5867/5888	5747/5748
74LS365	HEX BUS DRIVER	LST11	9483	5962/5901	5822/5821	4635(NOTE1)
74366	HEX BUS DRIVER (TRI-S)	T14	9413	5962/5901	5822/5821	4635(NOTE1)
74LS366	HEX BUS DRIVER (TRI-S)	LST11	9483	5962/5901	5822/5821	4635(NOTE1)
74367	HEX BUS DRIVER (TRI-S)	T14	9413	5962/5901	5822/5821	4635(NOTE1)
74LS367	HEX BUS DRIVER (TRI-S)	LST11	9483	5962/5901	5822/5821	4635(NOTE1)
74368	HEX BUS DRIVER (TRI-S)	T14	9413	5962/5901	5822/5821	4635(NOTE1)
74LS368	HEX BUS DRIVER (TRI-S)	LST11	9483	5962/5901	5822/5821	4635(NOTE1)
74LS373	OCTAL D-TYPE LATCH (TRI-S)	LST11	9483	5947/5922	5877/5878	5777/5778
74S373	OCTAL D-TYPE LATCH (TRI-S)	ST6	9489	5947/5922	5877/5878	5777/5778
74LS374	OCTAL D-TYPE FLIP/FLOP (TRI-S)	LST11	9483	5947/5922	5877/5878	5777/5778
74S374	OCTAL D-TYPE FLIP-FLOP (TRI-S)	ST6	9489	5947/5922	5877/5878	5777/5778

* This device may also be tested on adaptors listed for its "S" series counterpart.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
74LS375	4-BIT BISTABLE LATCH	LST11	9483	5962/5901	5822/5821	4635(NOTE1)
74390	DUAL DECADE COUNTER	T14	9413	5962/5901	5822/5821	4635(NOTE1)
74LS390	DUAL DECADE COUNTER	LST11	9483	5962/5901	5822/5821	4635(NOTE1)
74393	DUAL 4-BIT BINARY COUNTER	T14	9413	5938/5900	5837/5838	4634(NOTE1)
74LS393	DUAL 4-BIT BINARY COUNTER	LST11	9483	5938/5900	5837/5838	4634(NOTE1)

LIST B. 5400-SERIES TTL DEVICES.

Cartridge Designations: T1, T2, etc.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
5400	QUAD 2-INPUT POSITIVE NAND	T15	9309	5938/5900	5837/5838	4634(NOTE1)
54LS00	QUAD 2-INPUT NAND GATE	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54S00	QUAD 2-INPUT NAND GATE	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
5401	QUAD 2-INPUT POS NAND (O-C)	T15	9309	5938/5900	5837/5838	4634(NOTE1)
5402	QUAD 2-INPUT POSITIVE NOR	T15	9309	5938/5900	5837/5838	4634(NOTE1)
54LS02	QUAD 2-INPUT NOR GATE	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54S02	QUAD 2-INPUT POSITIVE NOR	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
5404	HEX INVERTER	T15	9309	5938/5900	5837/5838	4634(NOTE1)
54L04	HEX INVERTER	T15	9309	5938/5900	5837/5838	4634(NOTE1)
54LS04	HEX INVERTER	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54S04	HEX INVERTER	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
54LS05	HEX INVERTER (O-C)	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
5407	HEX BUFFER/DRIVER	T15	9309			
54LS08	QUAD 2-INPUT AND GATE	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54S08	QUAD 2-INPUT POSITIVE AND	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
54LS09	QUAD 2-INPUT AND GATE (O-C)	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
5410	TRIPLE 3-INPUT POSITIVE NAND	T15	9309	5938/5900	5837/5838	4634(NOTE1)
54LS10	TRIPLE 3-INPUT NAND GATE	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54S10	TRIPLE 3-INPUT POSITIVE NAND	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
54LS11	TRIPLE 3-INPUT AND GATE	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54S11	TRIPLE 3-INPUT POSITIVE AND	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
5420	DUAL 4-INPUT POSITIVE NAND	T15	9309	5938/5900	5837/5838	4634(NOTE1)
54H20	DUAL 4-INPUT POSITIVE NAND	T15	9309			
54LS20	DUAL 4-INPUT NAND GATE	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54S20	DUAL 4-INPUT POSITIVE NAND	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
54LS21	DUAL 4-INPUT AND GATE	LST12	9300	5938/5900	5837/5838	4634(NOTE1)
54L26	QUAD 2-INPUT POS NAND (O-C)	T15	9309	5938/5900	5837/5838	4634(NOTE1)
54LS26	QUAD 2-INPUT NAND GATE	LST13	9301	5938/5900	5837/5838	4634(NOTE1)
54LS27	TRIPLE 3-INPUT NOR GATE	LST13	9301	5938/5900	5837/5838	4634(NOTE1)
5430	8-INPUT POSITIVE NAND	T16	9310	5938/5900	5837/5838	4634(NOTE1)
54LS30	8-INPUT NAND GATE	LST13	9301	5938/5900	5837/5838	4634(NOTE1)
54S30	8-INPUT POSITIVE NAND	ST7	9307	5938/5900	5837/5838	4634(NOTE1)
54LS32	QUAD 2-INPUT OR GATE	LST13	9301	5938/5900	5837/5838	4634(NOTE1)

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand-ler Adaptor MCT/Trigon
54S32	QUAD 2-INPUT POSITIVE OR	ST7	9307	5938/5900	5837/5838	4634(NOTE 1)
5438	QUAD 2-INPUT POS NAND (O-C)	T16	9310	5938/5900	5837/5838	4634(NOTE 1)
54S40	DUAL 4-INPUT NAND GATE	ST7	9307	5938/5900	5837/5838	4634(NOTE 1)
54LS51	DUAL 2X2 AND-OR-INVERT	LST13	9301	5938/5900	5837/5838	4634(NOTE 1)
54S51	DUAL 2X2 AND-OR-INVERT	ST7	9307	5938/5900	5837/5838	4634(NOTE 1)
5473	DUAL J-K FLIP-FLOP	T16	9310	5952/5906	5825/5826	5502(NOTE 1)
54H73	DUAL J-K FLIP-FLOP	T16	9310	5952/5906	5825/5826	5502(NOTE 1)
54LS73	DUAL J-K FLIP/FLOP	LST13	9301	5952/5906	5825/5826	5502(NOTE 1)
*54LS74	DUAL D-TYPE FLIP-FLOP	LST13	9301	5938/5900	5837/5838	4634(NOTE 1)
54S74	DUAL D-TYPE FLIP-FLOP	ST7	9307	5881/5882	5837/5884	5545/5546
5476	DUAL J-K FLIP/FLOP	T16	9310	5939/5908	5829/5830	5504(NOTE 1)
54LS76	DUAL J-K FLIP-FLOP	LST13	9301	5939/5908	5829/5830	5504(NOTE 1)
54LS78	DUAL J-K FLIP-FLOP	LST13	9301	5952/5906	5825/5826	5502(NOTE 1)
54LS83	4-BIT FULL ADDER	LST13	9301	5936/5907	5823/5824	5503(NOTE 1)
54LS85	4-BIT MAGNITUDE COMPARATOR	LST14	9302	5962/5901	5822/5821	4635(NOTE 1)
54LS86	QUAD 2-INPUT EXCLUSIVE OR	LST14	9302	5938/5900	5837/5838	4634(NOTE 1)
54S86	QUAD 2-INPUT EXCLUSIVE OR	ST8	9308	5938/5900	5837/5838	4634(NOTE 1)
54LS90	DECADE COUNTER	LST14	9302	5946/5912	5841/5842	5503(NOTE 1)
54LS92	DIVIDE BY 12	LST14	9302	5946/5912	5841/5842	5503(NOTE 1)
54LS93	4-BIT BINARY COUNTER	LST14	9302	5946/5912	5841/5842	5503(NOTE 1)
54LS109	DUAL J-K FLIP-FLOP (EDGE-TRIG)	LST14	9302	5962/5901	5822/5821	4635(NOTE 1)
54S109	DUAL J-K FLIP-FLOP (EDGE-TRIG)	ST8	9308	5962/5901	5822/5821	4635(NOTE 1)
*54LS112	DUAL J-K FLIP-FLOP	LST14	9302	5962/5901	5822/5821	4635(NOTE 1)
54S112	DUAL J-K FLIP-FLOP	ST8	9308	5843/5844	5822/5846	5729/5730
54LS113	DUAL J-K FLIP-FLOP	LST14	9302	5938/5900	5837/5838	4634(NOTE 1)
54S113	DUAL J-K FLIP-FLOP	ST8	9308	5938/5900	5837/5838	4634(NOTE 1)
54LS123	DUAL RETRIG. MONOSTABLE MULTIV.	LST14	9302	5859/5860	5861/5862	5737/5738
54LS125	QUAD BUS BUFFER (TRI-STATE)	LST14	9302	5938/5900	5837/5838	4634(NOTE 1)
54LS138	3-TO-8-LINE DECODER	LST15	9303	5962/5901	5822/5821	4635(NOTE 1)
54S138	3-TO-8 LINE DECODER	ST8	9308	5962/5901	5822/5821	4635(NOTE 1)
54LS139	DUAL 2-TO-4-LINE DECODER	LST15	9303	5962/5901	5822/5821	4635(NOTE 1)
54LS151	1-OF-8 MULTIPLEXER	LST15	9303	5962/5901	5822/5821	4635(NOTE 1)
54S151	1-OF-8 MULTIPLEXER	ST8	9308	5962/5901	5822/5821	4635(NOTE 1)
54154	4-TO-16-LINE DECODER	T16	9310	5953/5902	5879/5880	5789/5790
54LS157	QUAD 2-TO-1 MULTIPLEXER	LST15	9303	5962/5901	5822/5821	4635(NOTE 1)
54LS158	QUAD 2 TO 1 MULTIPLEXER	LST15	9303	5962/5901	5822/5821	4635(NOTE 1)
54LS160	4-BIT SYNCH. DECADE COUNTER	LST15	9303	5869/5870	5871/5872	5541/5542
54LS161	4-BIT SYNCH. BINARY COUNTER	LST15	9303	5869/5870	5871/5872	5541/5542
54LS163	4-BIT SYNCH. BINARY COUNTER	LST15	9303	5869/5870	5871/5872	5541/5542
54LS164	8-BIT SHIFT REG PARALLEL OUT	LST15	9303	5938/5900	5837/5838	4634(NOTE 1)
54165	8-BIT SHIFT REG PARALLEL IN	T16	9310	5962/5901	5822/5821	4635(NOTE 1)
54LS165	8-BIT SHIFT REG PARALLEL IN	LST15	9303	5962/5901	5822/5821	4635(NOTE 1)
54166	8-BIT SHIFT REG. (PARALLEL IN)	T16	9310	5962/5901	5822/5821	4635(NOTE 1)
54LS169	4-BIT BINARY COUNTER	LST16	9304	5869/5870	5871/5872	5741/5742
54LS173	4-BIT D-TYPE REGISTER (TRI-S)	LST16	9304	5962/5901	5822/5821	4635(NOTE 1)

* This device may also be tested on adaptors listed for its "S" series counterpart.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
* 54174	HEX D-TYPE FLIP-FLOP	T16	9310	5962/5901	5822/5821	4635(NOTE1)
* 54LS174	HEX D-TYPE FLIP-FLOP	LST16	9304	5962/5901	5822/5821	4635(NOTE1)
54S174	HEX D-TYPE FLIP-FLOP	ST8	9308	5833/5834	5822/5836	5727/5728
* 54LS175	QUAD D-TYPE FLIP-FLOP	LST16	9304	5962/5901	5822/5821	4635(NOTE1)
54S175	QUAD D-TYPE FLIP-FLOP	ST8	9308	5833/5834	5822/5836	5727/5728
54LS181	ARITHMETIC LOGIC UNIT	LST16	9304	5953/5902	5879/5880	5789/5790
54S182	LOOK-AHEAD CARRY GENERATOR	ST8	9308	5962/5901	5822/5821	4635(NOTE1)
54LS189	64-BIT RAM (TRI-STATE)	LST16	9304			
54S189	64-BIT RAM (TRI-STATE)	ST8	9308			
54LS191	BINARY UP/DOWN COUNTER	LST16	9304	5962/5901	5822/5821	4635(NOTE1)
54LS193	BINARY UP/DOWN COUNTER	LST16	9304	5962/5901	5822/5821	4635(NOTE1)
54LS194	4-BIT BI-DIRECTIONAL SHIFT REG.	LST16	9304	5962/5901	5822/5821	4635(NOTE1)
54LS195	4-BIT PARALLEL ACCESS SHIFT REG.	LST16	9304	5962/5901	5822/5821	4635(NOTE1)
54LS196	DECADE COUNTER	LST17	9305	5938/5900	5837/5838	4634(NOTE1)
54LS244	OCTAL BUFFER DRVR/RCVR (TRI-S)	LST17	9305	5950/5911	5867/5868	5507(NOTE1)
54LS245	OCTAL BUS TRANSCEIVER	LST17	9305	5950/5911	5867/5868	5507(NOTE1)
54LS251	1-OF-8 MULTIPLEXER (TRI-STATE)	LST17	9305	5962/5901	5822/5821	4635(NOTE1)
54LS253	DUAL 1-OF-4 MULTIPLEXER (TRI-S)	LST17	9305	5962/5901	5822/5821	4635(NOTE1)
54S253	DUAL 1-OF-4 MULTIPLEXER (TRI-S)	ST8	9308	5962/5901	5822/5821	4635(NOTE1)
54LS257	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	LST17	9305	5962/5901	5822/5821	4635(NOTE1)
54S257	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	ST8	9308	5962/5901	5822/5821	4635(NOTE1)
54LS258	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	LST17	9305	5962/5901	5822/5821	4635(NOTE1)
54LS259	8-BIT ADDRESSABLE LATCH	LST17	9305	5962/5901	5822/5821	4635(NOTE1)
54LS273	OCTAL D-TYPE FLIP-FLOP	LST17	9305	5950/5911	5867/5868	5507(NOTE1)
54LS279	QUAD S-R LATCH	LST18	9306	5962/5901	5822/5821	4635(NOTE1)
54LS289	64-BIT RAM	LST18	9306			
54LS299	8-BIT BI-DIRECTIONAL SHIFT REG.	LST18	9306	5950/5911	5867/5868	5507(NOTE1)
54LS365	HEX BUS DRIVER	LST18	9306	5962/5901	5822/5821	4635(NOTE1)
54LS366	HEX BUS DRIVER (TRI-STATE)	LST18	9306	5962/5901	5822/5821	4635(NOTE1)
54LS367	HEX BUS DRIVER (TRI-STATE)	LST18	9306	5962/5901	5822/5821	4635(NOTE1)
54LS374	OCTAL D-TYPE FLIP/FLOP (TRI-S)	LST18	9306	5947/5922	5877/5878	5777/5778
54LS393	DUAL 4-BIT BINARY COUNTER	LST18	9306	5938/5900	5837/5838	4634(NOTE1)
54LS395	4-BIT SHIFT REGISTER (TRI-S)	LST18	9306			

* This device may also be tested on adaptors listed for its "S" series counterpart.

LIST C. CMOS DEVICES.
Cartridge Designations: C1, C2, etc.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
4000	DUAL 3-INPUT NOR PLUS INVERTER	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4001	QUAD 2-INPUT NOR	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4002	DUAL 4-INPUT NOR	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4006	18-STAGE STATIC SHIFT REGISTER	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4007UB	DUAL COMPLEMENTARY PAIR, INVRTG	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4008	4-BIT FULL ADDER	C1	9414	5940/5904	N.A.	5509(NOTE 1)
4009UB	HEX INVERTING BUFFER	C1	9414	5940/5904	N.A.	5509(NOTE 1)
4010	NON-INVERTING HEX BUF/CONVERTER	C1	9414	5940/5904	N.A.	5509(NOTE 1)
4011	QUAD 2-INPUT NAND GATE	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4012	DUAL 4-INPUT NAND GATE	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4013	DUAL D-TYPE FLIP/FLOP	C1	9414	5937/5903	N.A.	5508(NOTE 1)
4014	8-BIT SHIFT REGISTER	C1	9414	5940/5904	N.A.	5509(NOTE 1)
4015	DUAL 4-BIT STATIC SHIFT REG	C1	9414	5940/5904	N.A.	5509(NOTE 1)
4016	QUAD ANALOG SWITCH	C2	9415	5937/5903	N.A.	5508(NOTE 1)
4017	DECADE COUNTER/DIVIDER	C2	9415	5940/5904	N.A.	5509(NOTE 1)
4018	DIVIDE-BY-N COUNTER	C2	9415	5940/5904	N.A.	5509(NOTE 1)
4019	QUAD AND/OR SELECT (RCA)	C2	9415	5940/5904	N.A.	5509(NOTE 1)
4020	14-BIT BINARY COUNTER	C2	9415	5944/5921	N.A.	5510(NOTE 1)
4021	8-STAGE STATIC SHIFT REGISTER	C2	9415	5940/5904	N.A.	5509(NOTE 1)
4022	DIVIDE-BY-8 COUNTER	C2	9415	5940/5904	N.A.	5509(NOTE 1)
4023	TRIPLE 3-INPUT NAND GATE	C2	9415	5937/5903	N.A.	5508(NOTE 1)
4024	7-STAGE BINARY COUNTER	C2	9415	5937/5903	N.A.	5508(NOTE 1)
4025	TRIPLE 3-INPUT NOR	C2	9415	5937/5903	N.A.	5508(NOTE 1)
4026	DECADE COUNTER WITH 7-SEGMENTS	C2	9415	5940/5904	N.A.	5509(NOTE 1)
4027	DUAL J-K FLIP FLOP	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4028	BCD TO DECIMAL DECODER	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4029	UP/DOWN COUNTER	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4030	QUAD EXCLUSIVE OR	C3	9416	5937/5903	N.A.	5508(NOTE 1)
4031	64-STAGE SHIFT REGISTER	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4032	TRIPLE SERIAL ADDER	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4033	DECADE COUNTER	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4035	4-BIT PARALLEL/SERIAL SHIFT REG	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4040	12-BIT BINARY COUNTER	C3	9416	5940/5904	N.A.	5509(NOTE 1)
4041UB	QUAD BUFFER	C3	9416	5937/5903	N.A.	5508(NOTE 1)
4042	QUAD LATCH	C4	9417	5940/5904	N.A.	5509(NOTE 1)
4043	QUAD NOR - RS LATCH	C4	9417	5940/5904	N.A.	5509(NOTE 1)
4044	QUAD NAND - RS LATCH	C4	9417	5940/5904	N.A.	5509(NOTE 1)
4047UB	MONO/ASTABLE MULTIVIBRATOR	C4	9417	5949/5917	N.A.	5781/5782
4048	8-INPUT GATE	C4	9417	5940/5904	N.A.	5509(NOTE 1)
4049UB	HEX BUFFER (SEE 4009)	C4	9417	5948/5913	N.A.	5511(NOTE 1)

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
4050	HEX BUFFER (SEE 4010)	C4	9417	5948/5913	N.A.	5511(NOTE1)
4060	14-STAGE RIPPLE COUNTER	C4	9417	5400/5401	N.A.	5506(NOTE1)
4063	4-BIT MAGNITUDE COMPARATOR	C4	9417	5940/5904	N.A.	5509(NOTE1)
4066	QUAD ANALOG SWITCH	C4	9417	5937/5903	N.A.	5508(NOTE1)
4068	8-INPUT NAND	C5	9418	5937/5903	N.A.	5508(NOTE1)
4069	HEX INVERTER	C5	9418	5937/5903	N.A.	5508(NOTE1)
4070	QUAD EXCLUSIVE OR	C5	9418	5937/5903	N.A.	5508(NOTE1)
4071	2-INPUT OR	C5	9418	5937/5903	N.A.	5508(NOTE1)
4072	DUAL 4-INPUT OR	C5	9418	5937/5903	N.A.	5508(NOTE1)
4073	TRIPLE 3-INPUT AND	C5	9418	5937/5903	N.A.	5508(NOTE1)
4075	TRIPLE 3-INPUT OR	C5	9418	5937/5903	N.A.	5508(NOTE1)
4076	QUAD D-TYPE REGISTER	C5	9418	5940/5904	N.A.	5509(NOTE1)
4077	QUAD EXCLUSIVE NOR	C5	9418	5937/5903	N.A.	5508(NOTE1)
4078	8-INPUT NOR	C5	9418	5937/5903	N.A.	5508(NOTE1)
4081	QUAD 2-INPUT AND	C5	9418	5937/5903	N.A.	5508(NOTE1)
4082	DUAL 4-INPUT AND	C5	9418	5937/5903	N.A.	5508(NOTE1)
4085	DUAL 2-2 AND/OR GATE	C5	9418	5937/5903	N.A.	5508(NOTE1)
4086	8-INPUT NAND	C5	9418	5937/5903	N.A.	5508(NOTE1)
4093	QUAD 2-INPUT NAND (SCHMITT)	C5	9418	5937/5903	N.A.	5508(NOTE1)
40103	8-STAGE COUNTER	C5	9418	5940/5904	N.A.	5509(NOTE1)

LIST D. ECL DEVICES.

Cartridge Designations: E1, E2, etc.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand- ler Adaptor MCT/Trigon
10100	QUAD 2-INPUT NOR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10101	QUAD OR/NOR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10102	QUAD 2-INPUT NOR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10103	QUAD 2-INPUT OR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10104	QUAD 2-INPUT AND	E1	9419	5955/5930	N.A.	5512(NOTE1)
10105	TRIPLE 2-3-2 INPUT OR/NOR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10106	TRIPLE 4-3-3 INPUT NOR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10107	TRIPLE 2-INPUT EX/OR, EX/NOR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10109	DUAL 4-5-INPUT OR/NOR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10110	DUAL 3-INPUT 3-OUTPUT OR	E1	9419	5956/5929	N.A.	5513(NOTE1)
10111	DUAL 3-INPUT 3-OUTPUT NOR	E1	9419	5956/5929	N.A.	5513(NOTE1)
10113	QUAD EXCLUSIVE OR	E1	9419	5955/5930	N.A.	5512(NOTE1)
10114	TRIPLE LINE RECEIVER	E1	9419	5955/5930	N.A.	5512(NOTE1)
10115	QUAD LINE RECEIVER	E1	9419	5955/5930	N.A.	5512(NOTE1)
10116	TRIPLE LINE RECEIVER	E1	9419	5955/5930	N.A.	5512(NOTE1)
10117	DUAL 2-WIDE 2-3-INPUT OR-AND	E2	9420	5955/5930	N.A.	5512(NOTE1)
10118	DUAL 2-WIDE 3-INPUT OR-AND GATE	E2	9420	5955/5930	N.A.	5512(NOTE1)
10119	4-WIDE 4-3-3-3 INPUT OR-AND	E2	9420	5955/5930	N.A.	5512(NOTE1)

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand-ler Adaptor MCT/Trigon
10121	4-WIDE OR (AND/OR) AND INVERTER	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10123	TRIPLE 4-3-3-INPUT BUS DRIVER	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10124	QUAD TTL-TO-MECL TRANSLATOR	E2	9420	5941/5923	N.A.	5514(NOTE 1)
10125	QUAD MECL-TO-TTL TRANSLATOR	E2	9420	5957/5928	N.A.	5797/5798
10130	DUAL LATCH	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10131	DUAL D-TYPE FLIP/FLOP	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10132	DUAL MUX WITH LATCH	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10133	QUAD LATCH	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10134	DUAL MUX WITH LATCH	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10135	DUAL J-K MASTER-SLAVE FLIP/FLOP	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10136	UNIVERSAL HEX COUNTER	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10138	BI-QUINARY COUNTER	E2	9420	5955/5930	N.A.	5512(NOTE 1)
10141	4-BIT UNIVERSAL SHIFT REGISTER	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10153	QUAD LATCH	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10160	12-BIT PARITY CHECKER	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10161	BINARY 1-8 DECODER (LOW)	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10162	BINARY 1-8 DECODER (HIGH)	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10164	8-LINE MUX	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10173	QUAD 2-INPUT MUX/LATCH	E3	9421	5933/5932	N.A.	5515(NOTE 1)
10174	DUAL 4 TO 1 MUX	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10175	QUINT LATCH	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10176	HEX D-TYPE FLIP/FLOP	E3	9421	5955/5930	N.A.	5512(NOTE 1)
10178	BINARY COUNTER	E4	9422	5955/5930	N.A.	5512(NOTE 1)
10181	4-BIT ARITHMETIC LOGIC UNIT	E4	9422	5954/5931	N.A.	5791/5792
10184	2-BIT ALU	E4	9422	5955/5930	N.A.	5512(NOTE 1)
10195	HEX INVERTER/BUFFER	E4	9422	5955/5930	N.A.	5512(NOTE 1)
10197	HEX AND	E4	9422	5955/5930	N.A.	5512(NOTE 1)
10211	DUAL 3-INPUT 3-OUTPUT NOR	E4	9422	5956/5929	N.A.	5513(NOTE 1)
10216	TRIPLE LINE RECEIVER	E4	9422	5955/5930	N.A.	5512(NOTE 1)
10231	DUAL D-TYPE FLIP/FLOP	E4	9422	5955/5930	N.A.	5512(NOTE 1)

LIST E. MEMORY DEVICES.

Cartridge Designations: R1, R2, etc.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand-ler Adaptor MCT/Trigon
2102*	1KX1 RAM - STATIC MOS	R1	9423	9616/N.A.	N.A.	5516(NOTE 2)
2112*	256X4 RAM - STATIC MOS	R1	9423	9616/N.A.	N.A.	4635(NOTE 2)
2114*	1KX4 RAM - STATIC MOS	R1	9423	9616/N.A.	N.A.	5517(NOTE 2)
2147*	4KX1 STATIC RAM	R8	9452	9616/N.A.	N.A.	5517(NOTE 2)
2708	1KX8 STATIC EPROM	R6	9443	5971/5972	N.A.	5645/5646
2716*	2KX8 STATIC EPROM	R7	9444	5973/5974	N.A.	5613/5614
4096	4KX1 RAM - DYNAMIC MOS	R3	9425	9617/N.A.	N.A.	5518(NOTE 3)

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand-ler Adaptor MCT/Trigon
4116	16KX1 RAM - DYNAMIC MOS	R4	9426	9617/N.A.	N.A.	5518(NOTE3)
4164	64KX1 RAM - DYNAMIC SMOS	R10	9495	9617/N.A.	N.A.	N.A.
5101L	256X4 CMOS RAM	R9	9453	5813/5814	N.A.	4635(NOTE2)
93415*	1KX1 RAM - STATIC BIPOLAR	R5	9427	9616/N.A.	N.A.	4635(NOTE2)
93470*	4KX1 RAM - STATIC BIPOLAR	R5	9427	9616/N.A.	N.A.	5517(NOTE2)

* NOTE: Static RAM devices must be tested on systems with at least 32 D/S pins.

LIST F. MICROPROCESSORS AND SUPPORT CHIPS.

Cartridge Designations: M1, M2, etc.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand-ler Adaptor MCT/Trigon
Z-80	8-BIT MICROPROCESSOR (See M13)	M1	9428	5995/5918	N.A.	N.A.
Z80-PIO	2 X 8-BIT PARALLEL I/O (See M1)	M13	9440	5961/5958	N.A.	N.A.
CDP1802	COSMAC MICROPROCESSOR	M22	9451	5815/5816	N.A.	N.A.
CDP1802CC	COSMAC MICROPROCESSOR	M41	9472	5815/5816	N.A.	N.A.
AM2901	4-BIT MICROPROCESSOR	M20	9449	5998/5800	5835/5839	N.A.
AM2910	4-BIT MICROPROCESSOR	M21	9450	5998/5800	5835/5839	N.A.
6502	8-BIT MICROPROCESSOR	M35	9466	5817/5818	5889/5890	N.A.
6800	8-BIT MICROPROCESSOR	M7	9434	5966/5965	5895/5896	N.A.
6802	8-BIT MICROPROCESSOR	M8	9435	5986/5987	N.A.	N.A.
6809*	8-BIT MICROPROCESSOR	M27	9458	5819/5820	5891/5892	N.A.
6821	PERIPHERAL INTERFACE ADAPTOR	M9	9436	5989/5988	N.A.	N.A.
6828	PRIORITY INTERRUPT CONTROLLER	M10	9437	5964/5963	N.A.	N.A.
6850	ASYNCHRONOUS INTERFACE ADAPTOR	M11	9438	5990/5991	N.A.	N.A.
6852	SYNC SERIAL DATA ADAPTOR	M12	9439	5959/5960	N.A.	N.A.
8022	SINGLE-CHIP MICROPROCESSOR	M16	9445	5801/5802	N.A.	N.A.
8035	8-BIT MICROPROCESSOR	M17	9446	5985/5984	N.A.	N.A.
8039	8-BIT MICROPROCESSOR	M19	9448	5985/5984	N.A.	N.A.
8048	8-BIT MICROPROCESSOR	M14	9441	5985/5984	N.A.	N.A.
8048H	8-BIT MICROPROCESSOR	M23	9454	5985/5984	N.A.	N.A.
8049	8-BIT MICROPROCESSOR	M18	9447	5985/5984	N.A.	N.A.
8080	8-BIT MICROPROCESSOR	M2	9429	5967/5968	5897/5898	N.A.
8085	8-BIT MICROPROCESSOR	M6	9433	5977/5978	N.A.	N.A.
8086	16-BIT MICROPROCESSOR	M24	9125	5849/N.A.	N.A.	N.A.
8205	1-OF-8 BINARY DECODER	M15	9442	5962/5901	5822/5821	N.A.
8212	INPUT/OUTPUT PORT	M15	9442	5953/5902	5879/5880	N.A.
8214	PRIORITY INTERRUPT CONTROLLER	M3	9430	5982/5981	N.A.	N.A.
8216	BI-DIRECTIONAL BUS DRIVER	M15	9442	5962/5901	5822/5821	N.A.
8224	CLOCK DRIVER	M3	9430	5983/5979	5831/5832	N.A.
8226	BI-DIRECTIONAL BUS DRIVER	M15	9442	5962/5901	5822/5821	N.A.
8228	BUS CONTROLLER	M3	9430	5996/5997	N.A.	N.A.
8238	BUS CONTROLLER	M3	9430	5996/5997	N.A.	N.A.

Device Type	Device Description	Test Prog Tape	Order Number 1732-	Socket Adaptor K/non-K	2-Cbl Hdlr Contctr Bd K/non-K	5-Cbl Hand-ler Adaptor MCT/ Trigon
8255A	PARALLEL I/O	M4	9431	5993/5992	N.A.	N.A.
8259	INTERRUPT CONTROLLER	M5	9432	5975/5976	N.A.	N.A.
8253	PROGRAMMABLE INTERVAL TIMER	M26	9457	5953/5902	5879/5880	N.A.
8282	OCTAL LATCH	M43	9491	5950/5911	5867/5868	N.A.
8283	OCTAL LATCH - INVERTED	M43	9491	5950/5911	5867/5868	N.A.
8284	CLOCK GENERATOR/DRIVER	M44	9492	5845/N.A.	N.A.	N.A.
8284A	CLOCK GENERATOR/DRIVER	M44	9492	5845/N.A.	N.A.	N.A.
8286	OCTAL BUS TRANSCEIVER	M45	9493	5950/5911	5867/5868	N.A.
8287	OCTAL BUS TRANSCEIVER	M45	9493	5950/5911	5867/5868	N.A.
8288	BUS CONTROLLER	M46	9494	5950/5911	5867/5868	N.A.

* NOTE: The 6809 must be tested on a system with at least 48 D/S pins.

LIST G. CROSS-REFERENCE TO DEVICES TESTABLE ON GenRad SOCKET ADAPTORS

Adaptor.	Device Description	Pins	Tape Number	Kit Number (1732-)
1732-5400	(Kelvin) see also 1732-5401 (non-Kelvin)			
	4060 14-STAGE RIPPLE COUNTER	16	C4	9417
1732-5401	(non-Kelvin) see also 1732-5400 (Kelvin)			
	4060 14-STAGE RIPPLE COUNTER	16	C4	9417
1732-5800	(non-Kelvin) see also 1732-5998 (Kelvin)			
	AM2901 4-BIT MICROPROCESSOR	40	M20	9449
	AM2910 4-BIT MICROPROCESSOR	40	M21	9450
1732-5801	(Kelvin) see also 1732-5802 (non-Kelvin)			
	8022 SINGLE-CHIP MICROPROCESSOR	40	M16	9445
1732-5802	(non-Kelvin) see also 1732-5801 (Kelvin)			
	8022 SINGLE-CHIP MICROPROCESSOR	40	M16	9445
1732-5813	(Kelvin) see also 1732-5814 (non-Kelvin)			
	5101L 256X4 CMOS RAM	22	R9	9453
1732-5814	(non-Kelvin) see also 1732-5813 (Kelvin)			
	5101L 256X4 CMOS RAM	22	R9	9453
1732-5815	(Kelvin) see also 1732-5816 (non-Kelvin)			
	CDP1802 COSMAC MICROPROCESSOR	40	M22	9451
	CDP1802CCOSMAC MICROPROCESSOR	40	M41	9472
1732-5816	(non-Kelvin) see also 1732-5815 (Kelvin)			
	CDP1802 COSMAC MICROPROCESSOR	40	M22	9451
	CDP1802CCOSMAC MICROPROCESSOR	40	M41	9472
1732-5817	(Kelvin) see also 1732-5818 (non-Kelvin)			
	6502 MICROPROCESSOR	40	M35	9466
1732-5818	(non-Kelvin) see also 1732-5817 (Kelvin)			
	6502 MICROPROCESSOR	40	M35	9466
1732-5819	(Kelvin) see also 1732-5820 (non-Kelvin)			
	6809 8-BIT MICROPROCESSOR	40	M27	9458
1732-5820	(non-Kelvin) see also 1732-5819 (Kelvin)			
	6809 8-BIT MICROPROCESSOR	40	M27	9458
1732-5827	(Kelvin) see also 1732-5828 (non-Kelvin)			
	74S195 4-BIT PARALLEL ACCESS SHIFT REG	16	ST5	9488
1732-5828	(non-Kelvin) see also 1732-5827 (Kelvin)			
	74S195 4-BIT PARALLEL ACCESS SHIFT REG	16	ST5	9488
1732-5833	(Kelvin) see also 1732-5834 (non-Kelvin)			

Adaptor	Device	Description	Pins	Number	(1732-)
	54S174	HEX D-TYPE FLIP-FLOP	16	ST8	9308
	54S175	QUAD D-TYPE FLIP-FLOP	16	ST8	9308
	74S174	HEX D-TYPE FLIP-FLOP	16	ST4	9487
	74S175	QUAD D-TYPE FLIP-FLOP	16	ST4	9487
1732-5834	(non-Kelvin) see also 1732-5833 (Kelvin)				
	54S174	HEX D-TYPE FLIP-FLOP	16	ST8	9308
	54S175	QUAD D-TYPE FLIP-FLOP	16	ST8	9308
	74S174	HEX D-TYPE FLIP-FLOP	16	ST4	9487
	74S175	QUAD D-TYPE FLIP-FLOP	16	ST4	9487
1732-5843	(Kelvin) see also 1732-5844 (non-Kelvin)				
	54S112	DUAL J-K FLIP-FLOP	16	ST8	9308
	74S112A	DUAL J-K FLIP-FLOP	16	ST3	9486
1732-5844	(non-Kelvin) see also 1732-5843 (Kelvin)				
	54S112	DUAL J-K FLIP-FLOP	16	ST8	9308
	74S112A	DUAL J-K FLIP-FLOP	16	ST3	9486
1732-5845	(Kelvin) no non-Kelvin counterpart				
	8284	CLOCK GENERATOR/DRIVER	18	M44	9492
	8284A	CLOCK GENERATOR/DRIVER	18	M44	9492
1732-5847	(Kelvin) see also 1732-5848 (non-Kelvin)				
	74S194	4-BIT BI-DIREC SHIFT REGISTER	16	ST5	9488
1732-5848	(non-Kelvin) see also 1732-5847 (Kelvin)				
	74S194	4-BIT BI-DIREC SHIFT REGISTER	16	ST5	9488
1732-5849	(Kelvin) no non-Kelvin counterpart				
	8086	16-BIT MICROPROCESSOR	40	M24	9125
1732-5851	(Kelvin) see also 1732-5852 (non-Kelvin)				
	74S114A	DUAL J-K FLIP-FLOP	14	ST3	9486
1732-5852	(non-Kelvin) see also 1732-5851 (Kelvin)				
	74S114A	DUAL J-K FLIP-FLOP	14	ST3	9486
1732-5855	(Kelvin) see also 1732-5856 (non-Kelvin)				
	74LS221	DUAL MONOSTABLE MULTIVIBRATOR	16	LST9	9481
1732-5856	(non-Kelvin) see also 1732-5855 (Kelvin)				
	74LS221	DUAL MONOSTABLE MULTIVIBRATOR	16	LST9	9481
1732-5859	(Kelvin) see also 1732-5860 (non-Kelvin)				
	54LS123	DUAL RETRIG. MONOSTABLE MULTIV.	16	LST14	9302
	74LS123	DUAL RETRIG MULTISTABLE MULTIV.	16	LST5	9477
1732-5860	(non-Kelvin) see also 1732-5859 (Kelvin)				
	54LS123	DUAL RETRIG. MONOSTABLE MULTIV.	16	LST14	9302
	74LS123	DUAL RETRIG MULTISTABLE MULTIV.	16	LST5	9477
1732-5863	(Kelvin) see also 1732-5864 (non-Kelvin)				
	74LS122	RETRIG MULTISTABLE MULTIV	16	LST5	9477
1732-5864	(non-Kelvin) see also 1732-5863 (Kelvin)				
	74LS122	RETRIG MULTISTABLE MULTIV	16	LST5	9477
1732-5869	(Kelvin) see also 1732-5870 (non-Kelvin)				
	54LS160	4-BIT SYNCH. DECADE COUNTER	16	LST15	9303
	54LS161	4-BIT SYNCH. BINARY COUNTER	16	LST15	9303
	54LS163	4-BIT SYNCH. BINARY COUNTER	16	LST15	9303
	54LS169	4-BIT BINARY COUNTER	16	LST16	9304
	74LS160A	4-BIT SYNCH. DECADE COUNTER	16	LST7	9479
	74LS161A	4-BIT SYNCH. BINARY COUNTER	16	LST7	9479
	74S161	4-BIT SYNCH. BINARY COUNTER	16	ST4	9487
	74LS162A	4-BIT SYNCH. DECADE COUNTER	16	LST7	9479
	74S162	4-BIT SYNCH. DECADE COUNTER	16	ST4	9487
	74LS163A	4-BIT SYNCH. BINARY COUNTER	16	LST7	9479
	74S169	BINARY COUNTER	16	ST4	9487

Adaptor	Device	Description	Pins	Number	(1732-)
1732-5870	(non-Kelvin)	see also 1732-5869 (Kelvin)			
	54LS160	4-BIT SYNCH. DECADE COUNTER	16	LST15	9303
	54LS161	4-BIT SYNCH. BINARY COUNTER	16	LST15	9303
	54LS163	4-BIT SYNCH. BINARY COUNTER	16	LST15	9303
	54LS169	4-BIT BINARY COUNTER	16	LST16	9304
	74LS160A	4-BIT SYNCH. DECADE COUNTER	16	LST7	9479
	74LS161A	4-BIT SYNCH. BINARY COUNTER	16	LST7	9479
	74S161	4-BIT SYNCH. BINARY COUNTER	16	ST4	9487
	74LS162A	4-BIT SYNCH. DECADE COUNTER	16	LST7	9479
	74S162	4-BIT SYNCH. DECADE COUNTER	16	ST4	9487
	74LS163A	4-BIT SYNCH. BINARY COUNTER	16	LST7	9479
	74S169	BINARY COUNTER	16	ST4	9487
1732-5873	(Kelvin)	see also 1732-5874 (non-Kelvin)			
	74S196	DECADE COUNTER/LATCH	14	ST5	9488
	74S197	BINARY COUNTER/LATCH	14	ST5	9488
1732-5874	(non-Kelvin)	see also 1732-5873 (Kelvin)			
	74S196	DECADE COUNTER/LATCH	14	ST5	9488
	74S197	BINARY COUNTER/LATCH	14	ST5	9488
1732-5881	(Kelvin)	see also 1732-5882 (non-Kelvin)			
	54S74	DUAL D-TYPE FLIP-FLOP	14	ST7	9307
	74S74A	DUAL D-TYPE FLIP-FLOP	14	ST2	9485
1732-5882	(non-Kelvin)	see also 1732-5881 (Kelvin)			
	54S74	DUAL D-TYPE FLIP-FLOP	14	ST7	9307
	74S74A	DUAL D-TYPE FLIP-FLOP	14	ST2	9485
1732-5885	(Kelvin)	see also 1732-5886 (non-Kelvin)			
	74S299	8-BIT L-R SHIFT REGISTER	16	ST6	9489
1732-5886	(non-Kelvin)	see also 1732-5885 (Kelvin)			
	74S299	8-BIT L-R SHIFT REGISTER	16	ST6	9489
1732-5900	(non-Kelvin)	see also 1732-5938 (Kelvin)			
	5400	QUAD 2-INPUT POSITIVE NAND	14	T15	9309
	54LS00	QUAD 2-INPUT NAND GATE	14	LST12	9300
	54S00	QUAD 2-INPUT NAND GATE	14	ST7	9307
	5401	QUAD 2-INPUT POS NAND (O-C)	14	T15	9309
	5402	QUAD 2-INPUT POSITIVE NOR	14	T15	9309
	54LS02	QUAD 2-INPUT NOR GATE	14	LST12	9300
	54S02	QUAD 2-INPUT POSITIVE NOR	14	ST7	9307
	5404	HEX INVERTER	14	T15	9309
	54L04	HEX INVERTER	14	T15	9309
	54LS04	HEX INVERTER	14	LST12	9300
	54S04	HEX INVERTER	14	ST7	9307
	54LS05	HEX INVERTER (O-C)	14	LST12	9300
	5407	HEX BUFFER/DRIVER	14	T15	9309
	54LS08	QUAD 2-INPUT AND GATE	14	LST12	9300
	54S08	QUAD 2-INPUT POSITIVE AND	14	ST7	9307
	54LS09	QUAD 2-INPUT AND GATE (O-C)	14	LST12	9300
	5410	TRIPLE 3-INPUT POSITIVE NAND	14	T15	9309
	54LS10	TRIPLE 3-INPUT NAND GATE	14	LST12	9300
	54S10	TRIPLE 3-INPUT POSITIVE NAND	14	ST7	9307
	54LS11	TRIPLE 3-INPUT AND GATE	14	LST12	9300
	54S11	TRIPLE 3-INPUT POSITIVE AND	14	ST7	9307
	5420	DUAL 4-INPUT POSITIVE NAND	14	T15	9309
	54H20	DUAL 4-INPUT POSITIVE NAND	14	T15	9309
	54LS20	DUAL 4-INPUT NAND GATE	14	LST12	9300
	54S20	DUAL 4-INPUT POSITIVE NAND	14	ST7	9307

Adaptor	Device	Description	Pins	Number	(1732-)
	54LS21	DUAL 4-INPUT AND GATE	14	LST12	9300
	54L26	QUAD 2-INPUT POS NAND (O-C)	14	T15	9309
	54LS26	QUAD 2-INPUT NAND GATE	14	LST13	9301
	54LS27	TRIPLE 3-INPUT NOR GATE	14	LST13	9301
	5430	8-INPUT POSITIVE NAND	14	T16	9310
	54LS30	8-INPUT NAND GATE	14	LST13	9301
	54S30	8-INPUT POSITIVE NAND	14	ST7	9307
	54LS32	QUAD 2-INPUT OR GATE	14	LST13	9301
	54S32	QUAD 2-INPUT POSITIVE OR	14	ST7	9307
	5438	QUAD 2-INPUT POS NAND (O-C)	14	T16	9310
	54S40	DUAL 4-INPUT NAND GATE	14	ST7	9307
	54LS51	DUAL 2X2 AND-OR-INVERT	14	LST13	9301
	54S51	DUAL 2X2 AND-OR-INVERT	14	ST7	9307
	54LS74	DUAL D-TYPE FLIP-FLOP	14	LST13	9301
	54LS86	QUAD 2-INPUT EXCLUSIVE OR	14	LST14	9302
	54S86	QUAD 2-INPUT EXCLUSIVE OR	14	ST8	9308
	54LS113	DUAL J-K FLIP-FLOP	14	LST14	9302
	54S113	DUAL J-K FLIP-FLOP	14	ST8	9308
	54LS125	QUAD BUS BUFFER (TRI-STATE)	14	LST14	9302
	54LS164	8-BIT SHIFT REG PARALLEL OUT	14	LST15	9303
	54LS196	DECADE COUNTER	14	LST17	9305
	54LS393	DUAL 4-BIT BINARY COUNTER	14	LST18	9306
	7400	QUAD 2-INPUT POSITIVE NAND	14	T1	9400
	74LS00	QUAD 2-INPUT NAND GATE	14	LST1	9473
	74S00	QUAD 2-INPUT POSITIVE NAND	14	ST1	9484
	7401	QUAD 2-INPUT POSITIVE NAND(O-C)	14	T1	9400
	74LS01	QUAD 2-INPUT NAND GATE (O-C)	14	LST1	9473
	7402	QUAD 2-INPUT POSITIVE NOR	14	T1	9400
	74LS02	QUAD 2-INPUT NOR GATE	14	LST1	9473
	74S02	QUAD 2-INPUT POSITIVE NOR	14	ST1	9484
	7403	QUAD 2-INPUT POSITIVE NAND(O-C)	14	T1	9400
	74LS03	QUAD 2-INPUT NAND GATE (O-C)	14	LST1	9473
	74S03	QUAD 2-INPUT POSITIVE NAND(O-C)	14	ST1	9484
	7404	HEX INVERTER	14	T1	9400
	74LS04	HEX INVERTER	14	LST1	9473
	74S04	HEX INVERTER	14	ST1	9484
	7405	HEX INVERTER (O-C)	14	T1	9400
	74LS05	HEX INVERTER (O-C)	14	LST1	9473
	74S05	HEX INVERTER (O-C)	14	ST1	9484
	7408	QUAD 2-INPUT POSITIVE AND	14	T1	9400
	74LS08	QUAD 2-INPUT AND GATE	14	LST1	9473
	74S08	QUAD 2-INPUT POSITIVE AND	14	ST1	9484
	7409	QUAD 2-INPUT POSITIVE AND (O-C)	14	T1	9400
	74LS09	QUAD 2-INPUT AND GATE (O-C)	14	LST1	9473
	74S09	QUAD 2-INPUT POSITIVE AND (O-C)	14	ST1	9484
	7410	TRIPLE 3-INPUT POSITIVE NAND	14	T1	9400
	74LS10	TRIPLE 3-INPUT NAND GATE	14	LST1	9473
	74S10	TRIPLE 3-INPUT NAND GATE	14	ST1	9484
	74H11	TRIPLE 3-INPUT POSITIVE AND	14	T1	9400
	74LS11	TRIPLE 3-INPUT AND GATE	14	LST1	9473
	74S11	TRIPLE 3-INPUT POSITIVE AND	14	ST1	9484
	7412	TRIPLE 3-INPUT POS NAND (O-C)	14	T1	9400
	74LS12	TRIPLE 3-INPUT NAND GATE (O-C)	14	LST1	9473
	7413	DUAL 4-INPUT POS NAND (SCHMITT)	14	T1	9400

Adaptor	Device	Description	Pins	Number	(1732-)
	74LS13	DUAL 4-INPUT NAND (SCHMITT)	14	LST1	9473
	7414	HEX INVERTER (SCHMITT)	14	T1	9400
	74LS14	HEX INVERTER (SCHMITT)	14	LST1	9473
	74H15	TRIPLE 3-INPUT POS. AND (O-C)	14	T1	9400
	74LS15	TRIPLE 3-INPUT AND GATE (O-C)	14	LST1	9473
	74S15	TRIPLE 3-INPUT POS. AND (O-C)	14	ST1	9484
	7416	HEX INVERTER	14	T1	9400
	7417	HEX BUFFER (O-C)	14	T2	9401
	7420	DUAL 4-INPUT POSITIVE NAND	14	T2	9401
	74LS20	DUAL 4-INPUT NAND GATE	14	LST2	9474
	74S20	DUAL 4-INPUT POSITIVE NAND	14	ST1	9484
	74H21	DUAL 4-INPUT POSITIVE AND	14	T2	9401
	74LS21	DUAL 4-INPUT AND GATE	14	LST2	9474
	7422	DUAL 4-INPUT POS. NAND (O-C)	14	T2	9401
	74LS22	DUAL NAND GATE (O-C)	14	LST2	9474
	74S22	DUAL 4-INPUT POSITIVE NAND	14	ST1	9484
	7425	DUAL 4-INPUT POSITIVE NOR W/STR	14	T2	9401
	7426	QUAD HI V 2-INPUT POS NAND	14	T2	9401
	74LS26	QUAD 2-INPUT NAND GATE	14	LST2	9474
	7427	TRIPLE 3-INPUT POSITIVE NOR	14	T2	9401
	74LS27	TRIPLE 3-INPUT NOR GATE	14	LST2	9474
	7428	QUAD 2-INPUT POSITIVE NOR	14	T2	9401
	74LS28	QUAD 2-INPUT NOR	14	LST2	9474
	7430	8-INPUT POSITIVE NAND	14	T2	9401
	74LS30	8-INPUT NAND GATE	14	LST2	9474
	74S30	8-INPUT POSITIVE NAND	14	ST2	9485
	7432	QUAD 2-INPUT POSITIVE OR	14	T2	9401
	74LS32	QUAD 2-INPUT OR GATE	14	LST2	9474
	74S32	QUAD 2-INPUT POSITIVE OR	14	ST2	9485
	7433	QUAD 2-INPUT POSITIVE OR (O-C)	14	T2	9401
	73LS33	QUAD 2-INPUT NOR GATE (O-C)	14	LST2	9474
	7437	QUAD 2-INPUT NAND	14	T2	9401
	74LS37	QUAD 2-INPUT NAND GATE	14	LST2	9474
	74S37	QUAD 2-INPUT POSITIVE NAND	14	ST2	9485
	7438A	QUAD 2-INPUT POSITIVE NAND(O-C)	14	T2	9401
	74LS38	QUAD NAND GATE (O-C)	14	LST2	9474
	74S38	QUAD NAND BUFFER (O-C)	14	ST2	9485
	74LS40	DUAL 4-INPUT NAND GATE	14	LST2	9474
	7450	DUAL 2X2 AND-OR-INVERTER	14	T3	9402
	7451	3X3, 2X2 AND-OR-INVERTER	14	T3	9402
	74LS51	DUAL 2X2 AND-OR-INVERT	14	LST3	9475
	74S51	DUAL 2X2 AND-OR-INVERT	14	ST2	9485
	74H52	AND-OR-INVERTER	14	T3	9402
	7453	AND-OR-INVERTER EXPANDABLE	14	T3	9402
	74H53	AND-OR-INVERTER EXPANDABLE	14	T3	9402
	7454	AND-OR-INVERTER	14	T3	9402
	74LS54	AND-OR-INVERTER	14	LST3	9475
	74H55	AND-OR-INVERTER	14	T3	9402
	74LS55	AND-OR-INVERTER EXPANDABLE	14	LST3	9475
	74H61	TRIPLE EXPANDER	14	T3	9402
	74S64	4-2-3-2 AND-OR-INVERTER	14	ST2	9485
	7470	GATED J-K FLIP/FLOP	14	T4	9403
	74H71	GATED J-K FLIP/FLOP	14	T4	9403
	7472	GATED J-K FLIP/FLOP	14	T4	9403

Adaptor	Device	Description	Pins	Number	(1732-)
	7474	DUAL D-TYPE FLIP/FLOP	14	T4	9403
	74LS74A	DUAL D-TYPE FLIP-FLOP	14	LST3	9475
	7480	GATED FULL ADDER	14	T4	9403
	7486	QUAD 2-INPUT EXCLUSIVE OR	14	T5	9404
	74LS86	QUAD 2-INPUT EXCLUSIVE OR	14	LST4	9476
	74S86	QUAD 2-INPUT EXCLUSIVE OR	14	ST2	9485
	74H87	4-BIT TRUE/COMP 0/1 ELEMENT	14	T5	9404
	7495A	4-BIT SHIFT REGISTER	14	T5	9404
	74LS95B	4-BIT SHIFT REGISTER	14	LST4	9476
	74107	DUAL J-K M-S FLIP/FLOP	14	T6	9405
	74LS107ADUAL	J-K M-S FLIP-FLOP	14	LST4	9476
	74110	GATED M-S FLIP/FLOP	14	T6	9405
	74LS113ADUAL	J-K FLIP-FLOP	14	LST5	9477
	74LS114ADUAL	J-K FLIP-FLOP	14	LST5	9477
	74125	QUAD BUS BUFFER (TRI-S)	14	T7	9406
	74126	QUAD BUS BUFFER (TRI-S)	14	T7	9406
	74132	QUAD NAND (SCHMITT)	14	T7	9406
	74136	QUAD 2-INPUT EXCLUSIVE OR	14	T7	9406
	74LS136	QUAD EXCLUSIVE OR GATE	14	LST6	9478
	74S140	4-INPUT NAND LINE DRIVER	14	ST3	9486
	74152	1 OF 8 MUX	14	T8	9407
	74164	8-BIT SHIFT REG PARALLEL OUT	14	T9	9408
	74LS164	8-BIT SHIFT REG PARALLEL OUT	14	LST7	9479
	74176	DECADE COUNTER	14	T10	9409
	74177	BINARY COUNTER	14	T10	9409
	74180	PARITY GENERATOR	14	T10	9409
	74H183	DUAL FULL ADDER	14	T11	9410
	74LS183	DUAL FULL ADDER	14	LST8	9480
	74196	DECADE COUNTER	14	T12	9411
	74LS196	DECADE COUNTER/LATCH	14	LST9	9481
	74197	BINARY COUNTER	14	T12	9411
	74LS197	DECADE COUNTER/LATCH	14	LST9	9481
	74S260	DUAL 5-INPUT POSITIVE NOR	14	ST5	9488
	74LS266	QUAD EXCLUSIVE OR	14	LST10	9482
	74278	4-BIT CASCADE PRIORITY REGISTER	14	T13	9412
	74LS280	9-BIT PARITY GENERATOR/CHECKER	14	LST10	9482
	74S280	9-BIT PARITY GENERATOR	14	ST5	9488
	74293	4-BIT BINARY COUNTER	14	T13	9412
	74LS293	4-BIT BINARY COUNTER	14	LST10	9482
	74393	DUAL 4-BIT BINARY COUNTER	14	T14	9413
	74LS393	DUAL 4-BIT BINARY COUNTER	14	LST11	9483
1732-5901	(non-Kelvin) see also 1732-5962 (Kelvin)				
	54LS85	4-BIT MAGNITUDE COMPARATOR	16	LST14	9302
	54LS109	DUAL J-K FLIP-FLOP (EDGE-TRIG)	16	LST14	9302
	54S109	DUAL J-K FLIP-FLOP (EDGE-TRIG)	16	ST8	9308
	54LS112	DUAL J-K FLIP-FLOP	16	LST14	9302
	54LS138	3-TO-8-LINE DECODER	16	LST15	9303
	54S138	3-TO-8 LINE DECODER	16	ST8	9308
	54LS139	DUAL 2-TO-4-LINE DECODER	16	LST15	9303
	54LS151	1-OF-8 MULTIPLEXER	16	LST15	9303
	54S151	1-OF-8 MULTIPLEXER	16	ST8	9308
	54LS157	QUAD 2-TO-1 MULTIPLEXER	16	LST15	9303
	54LS158	QUAD 2 TO 1 MULTIPLEXER	16	LST15	9303
	54165	8-BIT SHIFT REG PARALLEL IN	16	T16	9310

Adaptor	Device	Description	Pins	Number	(1732-)
	54LS165	8-BIT SHIFT REG PARALLEL IN	16	LST15	9303
	54166	8-BIT SHIFT REG. (PARALLEL IN)	16	T16	9310
	54LS173	4-BIT D-TYPE REGISTER (TRI-S)	16	LST16	9304
	54174	HEX D-TYPE FLIP-FLOP	16	T16	9310
	54LS174	HEX D-TYPE FLIP-FLOP	16	LST16	9304
	54LS175	QUAD DOTYPE FLIP-FLOP	16	LST16	9304
	54S182	LOOK-AHEAD CARRY GENERATOR	16	ST8	9308
	54LS189	64-BIT RAM (TRI-STATE)	16	LST16	9304
	54S189	64-BIT RAM (TRI-STATE)	16	ST8	9308
	54LS191	BINARY UP/DOWN COUNTER	16	LST16	9304
	54LS193	BINARY UP/DOWN COUNTER	16	LST16	9304
	54LS194	4-BIT BI-DIRECTIONAL SHIFT REG.	16	LST16	9304
	54LS195	4-BIT PARALLEL ACCESS SHIFT REG.	16	LST16	9304
	54LS251	1-OF-8 MULTIPLEXER (TRI-STATE)	16	LST17	9305
	54LS253	DUAL 1-OF-4 MULTIPLEXER (TRI-S)	16	LST17	9305
	54S253	DUAL 1-OF-4 MULTIPLEXER (TRI-S)	16	ST8	9308
	54LS257	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	LST17	9305
	54S257	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	ST8	9308
	54LS258	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	LST17	9305
	54LS259	8-BIT ADDRESSABLE LATCH	16	LST17	9305
	54LS279	QUAD S-R LATCH	16	LST18	9306
	54LS289	64-BIT RAM	16	LST18	9306
	54LS365	HEX BUS DRIVER	16	LST18	9306
	54LS366	HEX BUS DRIVER (TRI-STATE)	16	LST18	9306
	54LS367	HEX BUS DRIVER (TRI-STATE)	16	LST18	9306
	54LS395	4-BIT SHIFT REGISTER (TRI-S)	16	LST18	9306
	7423	EXP DUAL 4-INPUT POSITIVE NOR	16	T2	9401
	7442A	BCD TO DEC CONVERTER	16	T3	9402
	74LS42	BCD TO DECIMAL CONVERTER	16	LST3	9475
	7445	BCD TO DEC DECODER/DRIVER (O-C)	16	T3	9402
	7446A	BCD TO 7-SEG DECODER/DRVR (O-C)	16	T3	9402
	7447A	BCD TO 7-SEG DECODER/DRVR (O-C)	16	T3	9402
	74LS47	BCD TO 7-SEGMENT DRIVER (O-C)	16	LST3	9475
	7448	BCD TO 7-SEGMENT DECODER/DRIVER	16	T3	9402
	74LS48	BCD TO 7-SEGMENT DRIVER	16	LST3	9475
	7485	4-BIT MAGNITUDE COMP	16	T5	9404
	74LS85	4-BIT MAGNITUDE COMPARATOR	16	LST4	9476
	74S85	4-BIT MAGNITUDE COMPARATOR	16	ST2	9485
	7497	6-BIT RATE MULT	16	T6	9405
	74L98	4-BIT SELECTOR/STORAGE REGISTER	16	T6	9405
	74109	DUAL J-K FLIP/FLOP	16	T6	9405
	74LS109	DUAL J-K FLIP-FLOP	16	LST4	9476
	74111	DUAL J-K M-S FLIP/FLOP	16	T6	9405
	74LS112	DUAL J-K FLIP/FLOP	16	LST5	9477
	74120	DUAL PULSE SYNCHRONIZER/DRIVER	16	T7	9406
	74S133	13-INPUT POSITIVE NAND	16	ST3	9486
	74S134	12-INPUT POSITIVE NAND (TRI-S)	16	ST3	9486
	74S135	QUAD EXCLUSIVE-OR/NOR	16	ST3	9486
	74LS138	3-TO-8-LINE DECODER	16	LST6	9478
	74S138	3-TO-8 LINE DECODER	16	ST3	9486
	74LS139	DUAL 2-TO-4-LINE DECODER	16	LST6	9478
	74S139	DUAL 2-TO-4 LINE DECODER	16	ST3	9486
	74145	BCD TO DEC DECODER/DRIVER	16	T8	9407
	74LS145	BCD-TO-DEC DECODER/DRIVER	16	LST6	9478

Adaptor	Device	Description	Pins	Number	(1732-)
	74148	8-TO-3-LINE PRIORITY ENCODER	16	T8	9407
	74LS148	8-TO-3 LINE PRIORITY ENCODER	16	LST6	9478
	74151	1 OF 8 MUX	16	T8	9407
	74LS151	1-OF-8 MULTIPLEXER	16	LST6	9478
	74S151	1-OF-8 MULTIPLEXER	16	ST3	9486
	74153	DUAL 1 OF 4 MUX	16	T8	9407
	74LS153	DUAL 1-OF-4 MULTIPLEXER	16	LST6	9478
	74S153	DUAL 1-OF-4 MULTIPLEXER	16	ST4	9487
	74155	DUAL 2-TO-4-LINE DECODER	16	T8	9407
	74LS155	DUAL 2-TO-4 LINE DECODER	16	LST6	9478
	74156	DUAL 2-TO-4-LINE DECODER (O-C)	16	T8	9407
	74LS156	DUAL 2-TO-4 LINE DECODER (O-C)	16	LST6	9478
	74157	QUAD 2 TO 1 MUX	16	T9	9408
	74LS157	QUAD 2-TO-1 MULTIPLEXER	16	LST6	9478
	74S157	QUAD 2-TO-1 MULTIPLEXER	16	ST4	9487
	74LS158	QUAD 2 TO 1 MULTIPLEXER	16	LST7	9479
	74S158	QUAD 2-TO-1 MULTIPLEXER	16	ST4	9487
	74160	DECADE COUNTER	16	T9	9408
	74161A	BINARY COUNTER	16	T9	9408
	74162	DECADE COUNTER	16	T9	9408
	74163	BINARY COUNTER	16	T9	9408
	74165	8-BIT SHIFT REG PARALLEL IN	16	T9	9408
	74LS165	8-BIT SHIFT REG PARALLEL IN	16	LST7	9479
	74166	8-BIT SHIFT REG PARALLEL IN	16	T9	9408
	74LS166	8-BIT SHIFT REG PARALLEL I/O	16	LST7	9479
	74170	4X4 REGISTER FILE	16	T10	9409
	74LS170	4X4 REGISTER FILE (O-C)	16	LST7	9479
	74173	4-BIT D-TYPE FLIP/FLOP (TRI-S)	16	T10	9409
	74LS173	4-BIT D-TYPE REGISTER (TRI-S)	16	LST7	9479
	74174	HEX D-TYPE FLIP/FLOP	16	T10	9409
	74LS174	HEX D-TYPE FLIP-FLOP	16	LST8	9480
	74175	QUAD D-TYPE FLIP/FLOP	16	T10	9409
	74LS175	QUAD D-TYPE FLIP-FLOP	16	LST8	9480
	74182	LOOK-AHEAD CARRY GENERATOR	16	T10	9409
	74S182	LOOK-AHEAD CARRY GENERATOR	16	ST4	9487
	74184	BCD TO BINARY CODE CONVERTER	16	T11	9410
	74185	BINARY TO BCD CODE CONVERTER	16	T11	9410
	74190	BCD UP/DOWN COUNTER	16	T11	9410
	74LS190	BCD UP/DOWN COUNTER	16	LST8	9480
	74191	BINARY UP/DOWN COUNTER	16	T11	9410
	74LS191	BINARY UP/DOWN COUNTER	16	LST8	9480
	74192	BCD UP/DOWN COUNTER	16	T11	9410
	74LS192	BCD UP/DOWN COUNTER	16	LST8	9480
	74193	BINARY UP/DOWN COUNTER	16	T11	9410
	74LS193	BINARY UP/DOWN COUNTER	16	LST8	9480
	74194	4-BIT BI-DIREC SHIFT REGISTER	16	T11	9410
	74LS194	4-BIT BI-DIREC SHIFT REGISTER	16	LST8	9480
	74195	4-BIT PARALLEL ACCESS SHIFT REG	16	T11	9410
	74LS195	4-BIT PARALLEL ACCESS SHIFT REG	16	LST8	9480
	74251	1 OF 8 MUX (TRI-STATE)	16	T12	9411
	74LS251	1-OF-8 MULTIPLEXER (TRI-STATE)	16	LST9	9481
	74S251	1-OF-8 MULTIPLEXER (TRI-STATE)	16	ST5	9488
	74LS253	DUAL 1 OF 4 MUX (TRI-STATE)	16	LST9	9481
	74LS257A	QUAD 1 OF 2 MUX (TRI-STATE)	16	LST9	9481

Adaptor	Device	Description	Pins	Number	(1732-)
	74LS258	QUAD 1 OF 2 MUX (TRI-STATE)	16	LST10	9482
	74S258	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	ST5	9488
	74LS259	8-BIT ADDRESSABLE LATCH	16	LST10	9482
	74265	QUAD COMPLEMENTARY-OUT ELEMENT	16	T13	9412
	74279	QUAD R-S LATCH	16	T13	9412
	74LS279	QUAD S-R LATCH	16	LST10	9482
	74283	4-BIT FULL ADDER	16	T13	9412
	74LS283	4-BIT FULL ADDER	16	LST10	9482
	74S283	4-BIT BINARY FULL ADDERS	16	ST6	9489
	74298	QUAD 1 OF 2 MUX/LATCH	16	T14	9413
	74LS365	HEX BUS DRIVER	16	LST11	9483
	74366	HEX BUS DRIVER (TRI-S)	16	T14	9413
	74LS366	HEX BUS DRIVER (TRI-S)	16	LST11	9483
	74367	HEX BUS DRIVER (TRI-S)	16	T14	9413
	74LS367	HEX BUS DRIVER (TRI-S)	16	LST11	9483
	74368	HEX BUS DRIVER (TRI-S)	16	T14	9413
	74LS368	HEX BUS DRIVER (TRI-S)	16	LST11	9483
	74LS375	4-BIT BISTABLE LATCH	16	LST11	9483
	74390	DUAL DECADE COUNTER	16	T14	9413
	74LS390	DUAL DECADE COUNTER	16	LST11	9483
	8205	1-OF-8 BINARY DECODER	16	M15	9442
	8216	BI-DIRECTIONAL BUS DRIVER	16	M15	9442
	8226	BI-DIRECTIONAL BUS DRIVER	16	M15	9442
1732-5902	(non-Kelvin) see also 1732-5953 (Kelvin)				
	54154	4-TO-16-LINE DECODER	24	T16	9310
	54LS181	ARITHMETIC LOGIC UNIT	24	LST16	9304
	74116	DUAL 4-BIT LATCH	24	T7	9406
	74150	1 OF 16 MUX	24	T8	9407
	74154	4-TO-16-LINE DECODER	24	T8	9407
	74159	4 TO 16 DECODER	24	T9	9408
	74172	16-BIT REGISTER FILE	24	T10	9409
	74181	ARITHMETIC LOGIC UNIT	24	T10	9409
	74LS181	ARITHMETIC LOGIC UNIT	24	LST8	9480
	74S181	ARITHMETIC LOGIC UNIT	24	ST4	9487
	74198	8-BIT BI-DIREC SHIFT REGISTER	24	T12	9411
	74199	8-BIT BI-DIRECTIONAL SHIFT REG	24	T12	9411
	8212	INPUT/OUTPUT PORT	24	M15	9442
	8253	PROGRAMMABLE INTERVAL TIMER	24	M26	9457
1732-5903	(non-Kelvin) see also 1732-5937 (Kelvin)				
	4000	DUAL 3-INPUT NOR PLUS INVERTER	14	C1	9414
	4001	QUAD 2-INPUT NOR	14	C1	9414
	4002	DUAL 4-INPUT NOR	14	C1	9414
	4006	18-STAGE STATIC SHIFT REGISTER	14	C1	9414
	4007UB	DUAL COMPLEMENTARY PAIR	14	C1	9414
	4011	QUAD 2-INPUT NAND GATE	14	C1	9414
	4012	DUAL 4-INPUT NAND	14	C1	9414
	4013	DUAL D-TYPE FLIP/FLOP	14	C1	9414
	4016	QUAD ANALOG SWITCH	14	C2	9415
	4023	TRIPLE 3-INPUT NAND GATE	14	C2	9415
	4024	7-STAGE BINARY COUNTER	14	C2	9415
	4025	TRIPLE 3-INPUT NOR	14	C2	9415
	4030	QUAD EXCLUSIVE OR	14	C3	9416
	4041UB	QUAD BUFFER	14	C3	9416
	4066	QUAD ANALOG SWITCH	14	C4	9417

Adaptor	Device	Description	Pins	Number	(1732-)
	4068	8-INPUT NAND	14	C5	9418
	4069	HEX INVERTER	14	C5	9418
	4070	QUAD EXCLUSIVE OR	14	C5	9418
	4071	2-INPUT OR	14	C5	9418
	4072	DUAL 4-INPUT OR	14	C5	9418
	4073	TRIPLE 3-INPUT AND	14	C5	9418
	4075	TRIPLE 3-INPUT OR	14	C5	9418
	4077	QUAD EXCLUSIVE NOR	14	C5	9418
	4078	8-INPUT NOR	14	C5	9418
	4081	QUAD 2-INPUT AND	14	C5	9418
	4082	DUAL 4-INPUT AND	14	C5	9418
	4085	DUAL 2-2 AND/OR GATE	14	C5	9418
	4086	8-INPUT NAND	14	C5	9418
	4093	QUAD 2-INPUT NAND (SCHMITT)	14	C5	9418
1732-5904	(non-Kelvin) see also 1732-5940 (Kelvin)				
	4008	4-BIT FULL ADDER	16	C1	9414
	4009UB	HEX INVERTING BUFFER	16	C1	9414
	4010	NON-INVERTING HEX BUF/CONVERTER	16	C1	9414
	4014	8-BIT SHIFT REGISTER	16	C1	9414
	4015	DUAL 4-BIT STATIC SHIFT REG	16	C1	9414
	4017	DECADE COUNTER/DIVIDER	16	C2	9415
	4018	DIVIDE-BY-N COUNTER	16	C2	9415
	4019	QUAD AND/OR SELECT (RCA)	16	C2	9415
	4021	8-STAGE STATIC SHIFT REGISTER	16	C2	9415
	4022	DIVIDE-BY-8 COUNTER	16	C2	9415
	4026	DECADE COUNTER WITH 7-SEGMENTS	16	C2	9415
	4027	DUAL J-K FLIP FLOP	16	C3	9416
	4028	BCD TO DECIMAL DECODER	16	C3	9416
	4029	UP/DOWN COUNTER	16	C3	9416
	4031	64-STAGE SHIFT REGISTER	16	C3	9416
	4032	TRIPLE SERIAL ADDER	16	C3	9416
	4033	DECADE COUNTER	16	C3	9416
	4035	4-BIT PARALLEL/SERIAL SHIFT REG	16	C3	9416
	4040	12-BIT BINARY COUNTER	16	C3	9416
	4042	QUAD LATCH	16	C4	9417
	4043	QUAD NOR -- RS LATCH	16	C4	9417
	4044	QUAD NAND -- RS LATCH	16	C4	9417
	4048	8-INPUT GATE	16	C4	9417
	4063	4-BIT MAGNITUDE COMPARATOR	16	C4	9417
	4076	QUAD D-TYPE REGISTER	16	C5	9418
	40103	8-STAGE COUNTER	16	C5	9418
1732-5906	(non-Kelvin) see also 1732-5952 (Kelvin)				
	5473	DUAL J-K FLIP-FLOP	14	T16	9310
	54H73	DUAL J-K FLIP-FLOP	14	T16	9310
	54LS73	DUAL J-K FLIP/FLOP	14	LST13	9301
	54LS78	DUAL J-K FLIP-FLOP	14	LST13	9301
	74LS73A	DUAL J-K FLIP/FLOP	14	LST3	9475
	74LS78A	DUAL J-K FLIP/FLOP	14	LST3	9475
	74H103	DUAL J-K FLIP/FLOP	14	T6	9405
1732-5907	(non-Kelvin) see also 1732-5936 (Kelvin)				
	54LS83	4-BIT FULL ADDER	16	LST13	9301
	7475	4-BIT LATCH	16	T4	9403
	74LS75	4-BIT BISTABLE LATCH	16	LST3	9475
	7483A	4-BIT FULL ADDER	16	T4	9403

Adaptor	Device	Description	Pins	Number	(1732-)
	74LS83A	4-BIT FULL ADDER	16	LST3	9475
	7494	4-BIT SHIFT REGISTER	16	T5	9404
	7496	5-BIT SHIFT REGISTER	16	T5	9404
	74LS96	5-BIT SHIFT REGISTER	16	LST4	9476
1732-5908	(non-Kelvin) see also 1732-5939 (Kelvin)				
	5476	DUAL J-K FLIP/FLOP	16	T16	9310
	54LS76	DUAL J-K FLIP-FLOP	16	LST13	9301
	7476	DUAL J-K FLIP/FLOP	16	T4	9403
	74LS76A	DUAL J-K FLIP-FLOP	16	LST3	9475
	74H106	DUAL J-K FLIP/FLOP	16	T6	9405
1732-5909	(non-Kelvin) see also 1732-5945 (Kelvin)				
	74H62	AND-OR EXPANDER	14	T3	9402
1732-5910	(non-Kelvin) see also 1732-5951 (Kelvin)				
	7460	DUAL EXPANDER	14	T3	9402
1732-5911	(non-Kelvin) see also 1732-5950 (Kelvin)				
	54LS244	OCTAL BUFFER DRVR/RCVR (TRI-S)	20	LST17	9305
	54LS245	OCTAL BUS TRANSCEIVER	20	LST17	9305
	54LS273	OCTAL D-TYPE FLIP-FLOP	20	LST17	9305
	54LS299	8-BIT BI-DIRECTIONAL SHIFT REG.	20	LST18	9306
	74LS240	OCTAL BUFFER (TRI-S)	20	LST9	9481
	74S240	OCTAL BUFFER LINE DRV/RCV (TRI)	20	ST5	9488
	74LS241	OCTAL BUFFER (TRI-S)	20	LST9	9481
	74S241	OCTAL BUFFER LINE DRV/RCV (TRI)	20	ST5	9488
	74LS244	OCTAL BUFFER LINE DRV/RCV (TRI)	20	LST9	9481
	74S244	OCTAL BUFFER (TRI-S)	20	ST5	9488
	74LS245	OCTAL BUS TRANSCEIVER	20	LST9	9481
	74273	OCTAL D-TYPE FLIP/FLOP	20	T13	9412
	74LS273	OCTAL D-TYPE FLIP-FLOP	20	LST10	9482
	74276	QUAD J-K FLIP/FLOP	20	T13	9412
	74LS299	8-BIT BI-DIREC SHIFT REGISTER	20	LST10	9482
	8282	OCTAL LATCH	20	M43	9491
	8283	OCTAL LATCH - INVERTED	20	M43	9491
	8286	OCTAL BUS TRANSCEIVER	20	M45	9493
	8287	OCTAL BUS TRANSCEIVER	20	M45	9493
	8288	BUS CONTROLLER	20	M46	9494
1732-5912	(non-Kelvin) see also 1732-5946 (Kelvin)				
	54LS90	DECADE COUNTER	14	LST14	9302
	54LS92	DIVIDE BY 12	14	LST14	9302
	54LS93	4-BIT BINARY COUNTER	14	LST14	9302
	7490A	DECADE COUNTER	14	T5	9404
	74LS90	DECADE COUNTER	14	LST4	9476
	7491A	8-BIT SHIFT REGISTER	14	T5	9404
	74LS91	8-BIT SHIFT REGISTER	14	LST4	9476
	7492A	DIVIDE BY 12	14	T5	9404
	74LS92	DIVIDE BY 12	14	LST4	9476
	7493A	4-BIT BINARY COUNTER	14	T5	9404
	74LS93	4-BIT BINARY COUNTER	14	LST4	9476
1732-5913	(non-Kelvin) see also 1732-5948 (Kelvin)				
	4049UB	HEX BUFFER (SEE 4009)	16	C4	9417
	4050	HEX BUFFER (SEE 4010)	16	C4	9417
1732-5914	(non-Kelvin) see also 1732-5943 (Kelvin)				
	74122	MONOSTABLE MULTIVIBRATOR	14	T7	9406
1732-5915	(non-Kelvin) see also 1732-5935 (Kelvin)				
	74121	MONOSTABLE MULTIVIBRATOR	14	T7	9406

Adaptor	Device	Description	Pins	Number	(1732-)
1732-5916	(non-Kelvin)	see also 1732-5934 (Kelvin)			
	74123	DUAL MONOSTABLE MULTIVIBRATOR	16	T7	9406
	74221	DUAL MONOSTABLE MULTIVIBRATOR	16	T12	9411
1732-5917	(non-Kelvin)	see also 1732-5949 (Kelvin)			
	4047UB	MONO/ASTABLE MULTIVIBRATOR	14	C4	9417
1732-5918	(non-Kelvin)	see also 1732-5995 (Kelvin)			
	Z-80	8-BIT MICROPROCESSOR (see M13)	40	M1	9428
1732-5920	(non-Kelvin)	see also 1732-5942 (Kelvin)			
	74100	DUAL 4-BIT LATCH	24	T6	9405
1732-5921	(non-Kelvin)	see also 1732-5944 (Kelvin)			
	4020	14-BIT BINARY COUNTER	16	C2	9415
1732-5922	(non-Kelvin)	see also 1732-5947 (Kelvin)			
	54LS374	OCTAL D-TYPE FLIP/FLOP (TRI-S)	20	LST18	9306
	74LS373	OCTAL D-TYPE LATCH (TRI-S)	20	LST11	9483
	74S373	OCTAL D-TYPE LATCH (TRI-S)	20	ST6	9489
	74LS374	OCTAL D-TYPE FLIP-FLOP (TRI-S)	20	LST11	9483
	74S374	OCTAL D-TYPE FLIP-FLOP (TRI-S)	20	ST6	9489
1732-5923	(non-Kelvin)	see also 1732-5941 (Kelvin)			
	10124	QUAD TTL-TO-MECL TRANSLATOR	16	E2	9420
1732-5928	(non-Kelvin)	see also 1732-5957 (Kelvin)			
	10125	QUAD MECL-TO-TTL TRANSLATOR	16	E2	9420
1732-5929	(non-Kelvin)	see also 1732-5956 (Kelvin)			
	10110	DUAL 3-INPUT 3-OUTPUT OR	16	E1	9419
	10111	DUAL 3-INPUT 3-OUTPUT NOR	16	E1	9419
	10211	DUAL 3-INPUT 3-OUTPUT NOR	16	E4	9422
1732-5930	(non-Kelvin)	see also 1732-5955 (Kelvin)			
	10100	QUAD 2-INPUT NOR	16	E1	9419
	10101	QUAD OR/NOR	16	E1	9419
	10102	QUAD 2-INPUT NOR	16	E1	9419
	10103	QUAD 2-INPUT OR	16	E1	9419
	10104	QUAD 2-INPUT AND	16	E1	9419
	10105	TRIPLE 2-3-2 INPUT OR/NOR	16	E1	9419
	10106	TRIPLE 4-3-3 INPUT NOR	16	E1	9419
	10107	TRIPLE 2-INPUT EX/OR, EX/NOR	16	E1	9419
	10109	DUAL 4-5-INPUT OR/NOR	16	E1	9419
	10113	QUAD EXCLUSIVE OR	16	E1	9419
	10114	TRIPLE LINE RECEIVER	16	E1	9419
	10115	QUAD LINE RECEIVER	16	E1	9419
	10116	TRIPLE LINE RECEIVER	16	E1	9419
	10117	DUAL 2-WIDE 2-3-INPUT OR-AND	16	E2	9420
	10118	DUAL 2-WIDE 3-INPUT OR-AND	16	E2	9420
	10119	4-WIDE 4-3-3-3 INPUT OR-AND	16	E2	9420
	10121	4-WIDE OR (AND/OR) AND INVERTER	16	E2	9420
	10123	TRIPLE 4-3-3-INPUT BUS DRIVER	16	E2	9420
	10130	DUAL LATCH	16	E2	9420
	10131	DUAL D-TYPE FLIP/FLOP	16	E2	9420
	10132	DUAL MUX WITH LATCH	16	E2	9420
	10133	QUAD LATCH	16	E2	9420
	10134	DUAL MUX WITH LATCH	16	E2	9420
	10135	DUAL J-K MASTER-SLAVE FLIP/FLOP	16	E2	9420
	10136	UNIVERSAL HEX COUNTER	16	E2	9420
	10138	BI-QUINARY COUNTER	16	E2	9420
	10141	4-BIT UNIVERSAL SHIFT REGISTER	16	E3	9421
	10153	QUAD LATCH	16	E3	9421

Adaptor	Device	Description	Pins	Number	(1732-)
	10160	12-BIT PARITY CHECKER	16	E3	9421
	10161	BINARY 1-8 DECODER (LOW)	16	E3	9421
	10162	BINARY 1-8 DECODER (HIGH)	16	E3	9421
	10164	8-LINE MUX	16	E3	9421
	10174	DUAL 4 TO 1 MULTIPLEXER	16	E3	9421
	10175	QUINT LATCH	16	E3	9421
	10176	HEX D-TYPE FLIP/FLOP	16	E3	9421
	10178	BINARY COUNTER	16	E4	9422
	10184	2-BIT ALU	16	E4	9422
	10195	HEX INVERTER/BUFFER	16	E4	9422
	10197	HEX AND	16	E4	9422
	10216	TRIPLE LINE RECEIVER	16	E4	9422
	10231	DUAL D-TYPE FLIP/FLOP	16	E4	9422
1732-5931	(non-Kelvin)	see also 1732-5954 (Kelvin)			
	10181	4-BIT ARITHMETIC LOGIC UNIT	24	E4	9422
1732-5932	(non-Kelvin)	see also 1732-5933 (Kelvin)			
	10173	QUAD 2-INPUT MUX/LATCH	16	E3	9421
1732-5933	(Kelvin)	see also 1732-5932 (non-Kelvin)			
	10173	QUAD 2-INPUT MUX/LATCH	16	E3	9421
1732-5934	(Kelvin)	see also 1732-5916 (non-Kelvin)			
	74123	DUAL MONOSTABLE MULTIVIBRATOR	16	T7	9406
	74221	DUAL MONOSTABLE MULTIVIBRATOR	16	T12	9411
1732-5935	(Kelvin)	see also 1732-5915 (non-Kelvin)			
	74121	MONOSTABLE MULTIVIBRATOR	14	T7	9406
1732-5936	(Kelvin)	see also 1732-5907 (non-Kelvin)			
	54LS83	4-BIT FULL ADDER	16	LST13	9301
	7475	4-BIT LATCH	16	T4	9403
	74LS75	4-BIT BISTABLE LATCH	16	LST3	9475
	7483A	4-BIT FULL ADDER	16	T4	9403
	74LS83A	4-BIT FULL ADDER	16	LST3	9475
	7494	4-BIT SHIFT REGISTER	16	T5	9404
	7496	5-BIT SHIFT REGISTER	16	T5	9404
	74LS96	5-BIT SHIFT REGISTER	16	LST4	9476
1732-5937	(Kelvin)	see also 1732-5903 (non-Kelvin)			
	4000	DUAL 3-INPUT NOR PLUS INVERTER	14	C1	9414
	4001	QUAD 2-INPUT NOR	14	C1	9414
	4002	DUAL 4-INPUT NOR	14	C1	9414
	4006	18-STAGE STATIC SHIFT REGISTER	14	C1	9414
	4007UB	DUAL COMPLEMENTARY PAIR	14	C1	9414
	4011	QUAD 2-INPUT NAND GATE	14	C1	9414
	4012	DUAL 4-INPUT NAND	14	C1	9414
	4013	DUAL D-TYPE FLIP/FLOP	14	C1	9414
	4016	QUAD ANALOG SWITCH	14	C2	9415
	4023	TRIPLE 3-INPUT NAND GATE	14	C2	9415
	4024	7-STAGE BINARY COUNTER	14	C2	9415
	4025	TRIPLE 3-INPUT NOR	14	C2	9415
	4030	QUAD EXCLUSIVE OR	14	C3	9416
	4041UB	QUAD BUFFER	14	C3	9416
	4066	QUAD ANALOG SWITCH	14	C4	9417
	4068	8-INPUT NAND	14	C5	9418
	4069	HEX INVERTER	14	C5	9418
	4070	QUAD EXCLUSIVE OR	14	C5	9418
	4071	2-INPUT OR	14	C5	9418
	4072	DUAL 4-INPUT OR	14	C5	9418

Adaptor	Device	Description	Pins	Number	(1732-)
	4073	TRIPLE 3-INPUT AND	14	C5	9418
	4075	TRIPLE 3-INPUT OR	14	C5	9418
	4077	QUAD EXCLUSIVE NOR	14	C5	9418
	4078	8-INPUT NOR	14	C5	9418
	4081	QUAD 2-INPUT AND	14	C5	9418
	4082	DUAL 4-INPUT AND	14	C5	9418
	4085	DUAL 2-2 AND/OR GATE	14	C5	9418
	4086	8-INPUT NAND	14	C5	9418
	4093	QUAD 2-INPUT NAND (SCHMITT)	14	C5	9418
1732-5938	(Kelvin)	see also 1732-5900 (non-Kelvin)			
	5400	QUAD 2-INPUT POSITIVE NAND	14	T15	9309
	54LS00	QUAD 2-INPUT NAND GATE	14	LST 12	9300
	54S00	QUAD 2-INPUT NAND GATE	14	ST7	9307
	5401	QUAD 2-INPUT POS NAND (O-C)	14	T15	9309
	5402	QUAD 2-INPUT POSITIVE NOR	14	T15	9309
	54LS02	QUAD 2-INPUT NOR GATE	14	LST 12	9300
	54S02	QUAD 2-INPUT POSITIVE NOR	14	ST7	9307
	5404	HEX INVERTER	14	T15	9309
	54L04	HEX INVERTER	14	T15	9309
	54LS04	HEX INVERTER	14	LST 12	9300
	54S04	HEX INVERTER	14	ST7	9307
	54LS05	HEX INVERTER (O-C)	14	LST 12	9300
	5407	HEX BUFFER/DRIVER	14	T15	9309
	54LS08	QUAD 2-INPUT AND GATE	14	LST 12	9300
	54S08	QUAD 2-INPUT POSITIVE AND	14	ST7	9307
	54LS09	QUAD 2-INPUT AND GATE (O-C)	14	LST 12	9300
	5410	TRIPLE 3-INPUT POSITIVE NAND	14	T15	9309
	54LS10	TRIPLE 3-INPUT NAND GATE	14	LST 12	9300
	54S10	TRIPLE 3-INPUT POSITIVE NAND	14	ST7	9307
	54LS11	TRIPLE 3-INPUT AND GATE	14	LST 12	9300
	54S11	TRIPLE 3-INPUT POSITIVE AND	14	ST7	9307
	5420	DUAL 4-INPUT POSITIVE NAND	14	T15	9309
	54H20	DUAL 4-INPUT POSITIVE NAND	14	T15	9309
	54LS20	DUAL 4-INPUT NAND GATE	14	LST 12	9300
	54S20	DUAL 4-INPUT POSITIVE NAND	14	ST7	9307
	54LS21	DUAL 4-INPUT AND GATE	14	LST 12	9300
	54L26	QUAD 2-INPUT POS NAND (O-C)	14	T15	9309
	54LS26	QUAD 2-INPUT NAND GATE	14	LST 13	9301
	54LS27	TRIPLE 3-INPUT NOR GATE	14	LST 13	9301
	5430	8-INPUT POSITIVE NAND	14	T16	9310
	54LS30	8-INPUT NAND GATE	14	LST 13	9301
	54S30	8-INPUT POSITIVE NAND	14	ST7	9307
	54LS32	QUAD 2-INPUT OR GATE	14	LST 13	9301
	54S32	QUAD 2-INPUT POSITIVE OR	14	ST7	9307
	5438	QUAD 2-INPUT POS NAND (O-C)	14	T16	9310
	54S40	DUAL 4-INPUT NAND GATE	14	ST7	9307
	54LS51	DUAL 2X2 AND-OR-INVERT	14	LST 13	9301
	54S51	DUAL 2X2 AND-OR-INVERT	14	ST7	9307
	54LS74	DUAL D-TYPE FLIP-FLOP	14	LST 13	9301
	54LS86	QUAD 2-INPUT EXCLUSIVE OR	14	LST 14	9302
	54S86	QUAD 2-INPUT EXCLUSIVE OR	14	ST8	9308
	54LS113	DUAL J-K FLIP-FLOP	14	LST 14	9302
	54S113	DUAL J-K FLIP-FLOP	14	ST8	9308
	54LS125	QUAD BUS BUFFER (TRI-STATE)	14	LST 14	9302

Adaptor	Device	Description	Pins	Number	(1732-)
	54LS164	8-BIT SHIFT REG PARALLEL OUT	14	LST15	9303
	54LS196	DECADE COUNTER	14	LST17	9305
	54LS393	DUAL 4-BIT BINARY COUNTER	14	LST18	9306
	7400	QUAD 2-INPUT POSITIVE NAND	14	T1	9400
	74LS00	QUAD 2-INPUT NAND GATE	14	LST1	9473
	74S00	QUAD 2-INPUT POSITIVE NAND	14	ST1	9484
	7401	QUAD 2-INPUT POSITIVE NAND(O-C)	14	T1	9400
	74LS01	QUAD 2-INPUT NAND GATE (O-C)	14	LST1	9473
	7402	QUAD 2-INPUT POSITIVE NOR	14	T1	9400
	74LS02	QUAD 2-INPUT NOR GATE	14	LST1	9473
	74S02	QUAD 2-INPUT POSITIVE NOR	14	ST1	9484
	7403	QUAD 2-INPUT POSITIVE NAND(O-C)	14	T1	9400
	74LS03	QUAD 2-INPUT NAND GATE (O-C)	14	LST1	9473
	74S03	QUAD 2-INPUT POSITIVE NAND(O-C)	14	ST1	9484
	7404	HEX INVERTER	14	T1	9400
	74LS04	HEX INVERTER	14	LST1	9473
	74S04	HEX INVERTER	14	ST1	9484
	7405	HEX INVERTER (O-C)	14	T1	9400
	74LS05	HEX INVERTER (O-C)	14	LST1	9473
	74S05	HEX INVERTER (O-C)	14	ST1	9484
	7408	QUAD 2-INPUT POSITIVE AND	14	T1	9400
	74LS08	QUAD 2-INPUT AND GATE	14	LST1	9473
	74S08	QUAD 2-INPUT POSITIVE AND	14	ST1	9484
	7409	QUAD 2-INPUT POSITIVE AND (O-C)	14	T1	9400
	74LS09	QUAD 2-INPUT AND GATE (O-C)	14	LST1	9473
	74S09	QUAD 2-INPUT POSITIVE NAND(O-C)	14	ST1	9484
	7410	TRIPLE 3-INPUT POSITIVE NAND	14	T1	9400
	74LS10	TRIPLE 3-INPUT NAND GATE	14	LST1	9473
	74S10	TRIPLE 3-INPUT POSITIVE NAND	14	ST1	9484
	74H11	TRIPLE 3-INPUT POSITIVE AND	14	T1	9400
	74LS11	TRIPLE 3-INPUT AND GATE	14	LST1	9473
	74S11	TRIPLE 3-INPUT POSITIVE AND	14	ST1	9484
	7412	TRIPLE 3-INPUT POS NAND (O-C)	14	T1	9400
	74LS12	TRIPLE 3-INPUT NAND GATE (O-C)	14	LST1	9473
	7413	DUAL 4-INPUT POS NAND (SCHMITT)	14	T1	9400
	74LS13	DUAL 4-INPUT NAND (SCHMITT)	14	LST1	9473
	74H15	TRIPLE 3-INPUT POS AND (O-C)	14	T1	9400
	74LS15	TRIPLE 3-INPUT AND GATE (O-C)	14	LST1	9473
	74S15	TRIPLE 3-INPUT POS AND (O-C)	14	ST1	9484
	7416	HEX INVERTER	14	T1	9400
	7417	HEX BUFFER (O-C)	14	T2	9401
	7420	DUAL 4-INPUT POSITIVE NAND	14	T2	9401
	74LS20	DUAL 4-INPUT NAND GATE	14	LST2	9474
	74S20	DUAL 4-INPUT POSITIVE AND	14	ST1	9484
	74H21	DUAL 4-INPUT POSITIVE AND	14	T2	9401
	74LS21	DUAL 4-INPUT AND GATE	14	LST2	9474
	7422	DUAL 4-INPUT POSITIVE AND (O-C)	14	T2	9401
	74LS22	DUAL NAND GATE (O-C)	14	LST2	9474
	74S22	DUAL 4-INPUT POSITIVE NAND	14	ST1	9484
	7425	DUAL 4-INPUT POSITIVE NOR W/STR	14	T2	9401
	7426	QUAD HI V 2-INPUT POS NAND(O-C)	14	T2	9401
	74LS26	QUAD 2-INPUT NAND GATE	14	LST2	9474
	7427	TRIPLE 3-INPUT POSITIVE NOR	14	T2	9401
	74LS27	TRIPLE 3-INPUT NOR GATE	14	LST2	9474

Adaptor	Device	Description	Pins	Number	(1732-)
	7428	QUAD 2-INPUT POSITIVE NOR	14	T2	9401
	74LS28	QUAD 2-INPUT NOR GATE	14	LST2	9474
	7430	8-INPUT POSITIVE NAND	14	T2	9401
	74LS30	8-INPUT NAND GATE	14	LST2	9474
	74S30	8-INPUT POSITIVE NAND	14	ST2	9485
	7432	QUAD 2-INPUT POSITIVE OR	14	T2	9401
	74LS32	QUAD 2-INPUT OR GATE	14	LST2	9474
	74S32	QUAD 2-INPUT POSITIVE OR	14	ST2	9485
	7433	QUAD 2-INPUT POSITIVE OR (O-C)	14	T2	9401
	74LS33	QUAD 2-INPUT NOR GATE (O-C)	14	LST2	9474
	7437	QUAD 2-INPUT NAND	14	T2	9401
	74LS37	QUAD 2-INPUT NAND GATE	14	LST2	9474
	74S37	QUAD 2-INPUT POSITIVE NAND	14	ST2	9485
	7438A	QUAD 2-INPUT POS NAND (O-C)	14	T2	9401
	74LS38	QUAD NAND GATE (O-C)	14	LST2	9474
	74S38	QUAD NAND BUFFER (O-C)	14	ST2	9485
	74LS40	DUAL 4-INPUT NAND GATE	14	LST2	9474
	7450	DUAL 2X2 AND-OR-INVERTER	14	T3	9402
	7451	3X3, 2X2 AND-OR-INVERTER	14	T3	9402
	74LS51	DUAL 2X2 AND-OR-INVERTER	14	LST3	9475
	74S51	DUAL 2X2 AND-OR-INVERTER	14	ST2	9485
	74H52	AND-OR-INVERTER	14	T3	9402
	7453	AND-OR-INVERTER EXPANDABLE	14	T3	9402
	74H53	AND-OR-INVERTER EXPANDABLE	14	T3	9402
	7454	AND-OR-INVERTER	14	T3	9402
	74LS54	AND-OR-INVERTER	14	LST3	9475
	74H55	AND-OR-INVERTER	14	T3	9402
	74LS55	AND-OR-INVERTER EXPANDABLE	14	LST3	9475
	74H61	TRIPLE EXPANDER	14	T3	9402
	74S64	4-2-3-2 AND-OR-INVERTER	14	ST2	9485
	7470	GATED J-K FLIP/FLOP	14	T4	9403
	74H71	GATED J-K FLIP/FLOP	14	T4	9403
	7472	GATED J-K FLIP/FLOP	14	T4	9403
	7474	DUAL D-TYPE FLIP/FLOP	14	T4	9403
	74LS74A	DUAL D-TYPE FLIP-FLOP	14	LST3	9475
	7480	GATED FULL ADDER	14	T4	9403
	7486	QUAD 2-INPUT EXCLUSIVE OR	14	T5	9404
	74LS86	QUAD 2-INPUT EXCLUSIVE OR	14	LST4	9476
	74S86	QUAD 2-INPUT EXCLUSIVE OR	14	ST2	9485
	74H87	4-BIT TRUE/COMP 0/1 ELEMENT	14	T5	9404
	7495A	4-BIT SHIFT REGISTER	14	T5	9404
	74LS95B	4-BIT SHIFT REGISTER	14	LST4	9476
	74107	DUAL J-K M-S FLIP/FLOP	14	T6	9405
	74LS107ADUAL	J-K M-S FLIP-FLOP	14	LST4	9476
	74LS113ADUAL	J-K FLIP-FLOP	14	LST5	9477
	74LS114ADUAL	J-K FLIP-FLOP	14	LST5	9477
	74110	GATED M-S FLIP/FLOP	14	T6	9405
	74125	QUAD BUS BUFFER (TRI-STATE)	14	T7	9406
	74126	QUAD BUS BUFFER (TRI-STATE)	14	T7	9406
	74132	QUAD NAND (SCHMITT)	14	T7	9406
	74136	QUAD 2-INPUT EXCLUSIVE OR	14	T7	9406
	74LS136	QUAD EXCLUSIVE OR GATE	14	LST6	9478
	74S140	4-INPUT NAND LINE DRIVER	14	ST3	9486
	74152	1 OF 8 MUX	14	T8	9407

Adaptor	Device	Description	Pins	Number	(1732-)
	74S160	4-INPUT NAND LINE DRIVER	14	ST3	9486
	74164	8-BIT SHIFT REG PARALLEL OUT	14	T9	9408
	74LS164	8-BIT SHIFT REG PARALLEL OUT	14	LST7	9479
	74176	DECADE COUNTER	14	T10	9409
	74177	BINARY COUNTER	14	T10	9409
	74180	PARITY GENERATOR	14	T10	9409
	74H183	DUAL FULL ADDER	14	T11	9410
	74LS183	DUAL FULL ADDER	14	LST8	9480
	74196	DECADE COUNTER	14	T12	9411
	74LS196	DECADE COUNTER/LATCH	14	LST9	9481
	74197	BINARY COUNTER	14	T12	9411
	74LS197	BINARY COUNTER/LATCH	14	LST9	9481
	74S260	DUAL 5-INPUT POSITIVE NOR	14	ST5	9488
	74LS266	QUAD EXCLUSIVE OR	14	LST10	9482
	74278	4-BIT CASCADE PRIORITY REGISTER	14	T13	9412
	74LS280	9-BIT PARITY GENERATOR/CHECKER	14	LST10	9482
	74S280	9-BIT PARITY GENERATOR	14	T6	9489
	74293	4-BIT BINARY COUNTER	14	T13	9412
	74LS293	4-BIT BINARY COUNTER	14	LST10	9482
	74393	DUAL 4-BIT BINARY COUNTER	14	T14	9413
	74LS393	DUAL 4-BIT BINARY COUNTER	14	LST11	9483
1732-5939	(Kelvin)	see also 1732-5908 (non-Kelvin)			
	5476	DUAL J-K FLIP/FLOP	16	T16	9310
	54LS76	DUAL J-K FLIP-FLOP	16	LST13	9301
	7476	DUAL J-K FLIP/FLOP	16	T4	9403
	74LS76A	DUAL J-K FLIP-FLOP	16	LST3	9475
	74H106	DUAL J-K FLIP/FLOP	16	T6	9405
1732-5940	(Kelvin)	see also 1732-5904 (non-Kelvin)			
	4008	4-BIT FULL ADDER	16	C1	9414
	4009UB	HEX INVERTING BUFFER	16	C1	9414
	4010	NON-INVERTING HEX BUF/CONVERTER	16	C1	9414
	4014	8-BIT SHIFT REGISTER	16	C1	9414
	4015	DUAL 4-BIT STATIC SHIFT REG	16	C1	9414
	4017	DECADE COUNTER/DIVIDER	16	C2	9415
	4018	DIVIDE-BY-N COUNTER	16	C2	9415
	4019	QUAD AND/OR SELECT (RCA)	16	C2	9415
	4021	8-STAGE STATIC SHIFT REGISTER	16	C2	9415
	4022	DIVIDE-BY-8 COUNTER	16	C2	9415
	4026	DECADE COUNTER WITH 7-SEGMENTS	16	C2	9415
	4027	DUAL J-K FLIP FLOP	16	C3	9416
	4028	BCD TO DECIMAL DECODER	16	C3	9416
	4029	UP/DOWN COUNTER	16	C3	9416
	4031	64-STAGE SHIFT REGISTER	16	C3	9416
	4032	TRIPLE SERIAL ADDER	16	C3	9416
	4033	DECADE COUNTER	16	C3	9416
	4035	4-BIT PARALLEL/SERIAL SHIFT REG	16	C3	9416
	4040	12-BIT BINARY COUNTER	16	C3	9416
	4042	QUAD LATCH	16	C4	9417
	4043	QUAD NOR -- RS LATCH	16	C4	9417
	4044	QUAD NAND -- RS LATCH	16	C4	9417
	4048	8-INPUT GATE	16	C4	9417
	4063	4-BIT MAGNITUDE COMPARATOR	16	C4	9417
	4076	QUAD D-TYPE REGISTER	16	C5	9418
	40103	8-STAGE COUNTER	16	C5	9418

Adaptor	Device	Description	Pins	Number	(1732-)
1732-5941	(Kelvin)	see also 1732-5923 (non-Kelvin)			
	10124	QUAD TTL-TO-MECL TRANSLATOR	16	E2	9420
1732-5942	(Kelvin)	see also 1732-5920 (non-Kelvin)			
	74100	DUAL 4-BIT LATCH	24	T6	9405
1732-5943	(Kelvin)	see also 1732-5914 (non-Kelvin)			
	74122	MONOSTABLE MULTIVIBRATOR	14	T7	9406
1732-5944	(Kelvin)	see also 1732-5921 (non-Kelvin)			
	4020	14-BIT BINARY COUNTER	16	C2	9415
1732-5945	(Kelvin)	see also 1732-5909 (non-Kelvin)			
	74H62	AND-OR EXPANDER	14	T3	9402
1732-5946	(Kelvin)	see also 1732-5912 (non-Kelvin)			
	54LS90	DECADE COUNTER	14	LST14	9302
	54LS92	DIVIDE BY 12	14	LST14	9302
	54LS93	4-BIT BINARY COUNTER	14	LST14	9302
	7490A	DECADE COUNTER	14	T5	9404
	74LS90	DECADE COUNTER	14	LST4	9476
	7491A	8-BIT SHIFT REGISTER	14	T5	9404
	74LS91	8-BIT SHIFT REGISTER	14	LST4	9476
	7492A	DIVIDE BY 12	14	T5	9404
	74LS92	DIVIDE BY 12	14	LST4	9476
	7493A	4-BIT BINARY COUNTER	14	T5	9404
	74LS93	4-BIT BINARY COUNTER	14	LST4	9476
1732-5947	(Kelvin)	see also 1732-5922 (non-Kelvin)			
	54LS374	OCTAL D-TYPE FLIP/FLOP (TRI-S)	20	LST18	9306
	74LS373	OCTAL D-TYPE LATCH (TRI-S)	20	LST11	9483
	74S373	OCTAL D-TYPE LATCH (TRI-S)	20	ST6	9489
	74LS374	OCTAL D-TYPE FLIP-FLOP (TRI-S)	20	LST11	9483
	74S374	OCTAL D-TYPE FLIP-FLOP (TRI-S)	20	ST6	9489
1732-5948	(Kelvin)	see also 1732-5913 (non-Kelvin)			
	4049UB	HEX BUFFER (SEE 4009)	16	C4	9417
	4050	HEX BUFFER (SEE 4010)	16	C4	9417
1732-5949	(Kelvin)	see also 1732-5917 (non-Kelvin)			
	4047UB	MONO/ASTABLE MULTIVIBRATOR	14	C4	9417
1732-5950	(Kelvin)	see also 1732-5911 (non-Kelvin)			
	54LS244	OCTAL BUFFER DRV/RCVR (TRI-S)	20	LST17	9305
	54LS245	OCTAL BUS TRANSCEIVER	20	LST17	9305
	54LS273	OCTAL D-TYPE FLIP-FLOP	20	LST17	9305
	54LS299	8-BIT BI-DIRECTIONAL SHIFT REG.	20	LST18	9306
	74LS240	OCTAL BUFFER (TRI-S)	20	LST9	9481
	74S240	OCTAL BUFFER LINE DRV/RCV (TRI)	20	ST5	9488
	74LS241	OCTAL BUFFER (TRI-S)	20	LST9	9481
	74S241	OCTAL BUFFER LINE DRV/RCV (TRI)	20	ST5	9488
	74LS244	OCTAL BUFFER LINE DRV/RCV (TRI)	20	LST9	9481
	74S244	OCTAL BUFFER (TRI-S)	20	ST5	9488
	74LS245	OCTAL BUS TRANSCEIVER	20	LST9	9481
	74273	OCTAL D-TYPE FLIP/FLOP	20	T13	9412
	74LS273	OCTAL D-TYPE FLIP-FLOP	20	LST10	9482
	74276	QUAD J-K FLIP/FLOP	20	T13	9412
	74LS299	8-BIT BI-DIREC SHIFT REGISTER	20	LST10	9482
	8282	OCTAL LATCH	20	M43	9491
	8283	OCTAL LATCH - INVERTED	20	M43	9491
	8286	OCTAL BUS TRANSCEIVER	20	M45	9493
	8287	OCTAL BUS TRANSCEIVER	20	M45	9493
	8288	BUS CONTROLLER	20	M46	9494

Adaptor	Device	Description	Pins	Number	(1732-)
1732-5951	(Kelvin)	see also 1732-5910 (non-Kelvin)			
	7460	DUAL EXPANDER	14	T3	9402
1732-5952	(Kelvin)	see also 1732-5906 (non-Kelvin)			
	5473	DUAL J-K FLIP-FLOP	14	T16	9310
	54H73	DUAL J-K FLIP-FLOP	14	T16	9310
	54LS73	DUAL J-K FLIP/FLOP	14	LST13	9301
	54LS78	DUAL J-K FLIP-FLOP	14	LST13	9301
	74LS73A	DUAL J-K FLIP/FLOP	14	LST3	9475
	74LS78A	DUAL J-K FLIP/FLOP	14	LST3	9475
	74H103	DUAL J-K FLIP/FLOP	14	T6	9405
1732-5953	(Kelvin)	see also 1732-5902 (non-Kelvin)			
	54154	4-TO-16-LINE DECODER	24	T16	9310
	54LS181	ARITHMETIC LOGIC UNIT	24	LST16	9304
	74116	DUAL 4-BIT LATCH	24	T7	9406
	74150	1-OF-16 MULTIPLEXER	24	T8	9407
	74154	4-TO-16-LINE DECODER	24	T8	9407
	74159	4-TO-16 DECODER	24	T9	9408
	74172	16-BIT REGISTER FILE	24	T10	9409
	74181	ARITHMETIC LOGIC UNIT	24	T10	9409
	74LS181	ARITHMETIC LOGIC UNIT	24	LST8	9480
	74S181	ARITHMETIC LOGIC UNIT	24	ST4	9487
	74198	8-BIT BI-DIREC SHIFT REGISTER	24	T12	9411
	74199	8-BIT BI-DIRECTIONAL SHIFT REG	24	T12	9411
	8212	INPUT/OUTPUT PORT	24	M15	9442
	8253	PROGRAMMABLE INTERVAL TIMER	24	M26	9457
1732-5954	(Kelvin)	see also 1732-5931 (non-Kelvin)			
	10181	4-BIT ARITHMETIC LOGIC UNIT	24	E4	9422
1732-5955	(Kelvin)	see also 1732-5930 (non-Kelvin)			
	10100	QUAD 2-INPUT NOR	16	E1	9419
	10101	QUAD OR/NOR	16	E1	9419
	10102	QUAD 2-INPUT NOR	16	E1	9419
	10103	QUAD 2-INPUT OR	16	E1	9419
	10104	QUAD 2-INPUT AND	16	E1	9419
	10105	TRIPLE 2-3-2 INPUT OR/NOR	16	E1	9419
	10106	TRIPLE 4-3-3 INPUT NOR	16	E1	9419
	10107	TRIPLE 2-INPUT EX/OR, EX/NOR	16	E1	9419
	10109	DUAL 4-5-INPUT OR/NOR	16	E1	9419
	10113	QUAD EXCLUSIVE OR	16	E1	9419
	10114	TRIPLE LINE RECEIVER	16	E1	9419
	10115	QUAD LINE RECEIVER	16	E1	9419
	10116	TRIPLE LINE RECEIVER	16	E1	9419
	10117	DUAL 2-WIDE 2-3-INPUT OR-AND	16	E2	9420
	10118	DUAL 2-WIDE 3-INPUT OR-AND	16	E2	9420
	10119	4-WIDE 4-3-3-3 INPUT OR-AND	16	E2	9420
	10121	4-WIDE OR (AND/OR) AND INVERTER	16	E2	9420
	10123	TRIPLE 4-3-3-INPUT BUS DRIVER	16	E2	9420
	10130	DUAL LATCH	16	E2	9420
	10131	DUAL D-TYPE FLIP/FLOP	16	E2	9420
	10132	DUAL MUX WITH LATCH	16	E2	9420
	10133	QUAD LATCH	16	E2	9420
	10134	DUAL MUX WITH LATCH	16	E2	9420
	10135	DUAL J-K MASTER-SLAVE FLIP/FLOP	16	E2	9420
	10136	UNIVERSAL HEX COUNTER	16	E2	9420
	10138	BI-QUINARY COUNTER	16	E2	9420

Adaptor	Device	Description	Pins	Number	(1732-)
	10141	4-BIT UNIVERSAL SHIFT REGISTER	16	E3	9421
	10153	QUAD LATCH	16	E3	9421
	10160	12-BIT PARITY CHECKER	16	E3	9421
	10161	BINARY 1-8 DECODER (LOW)	16	E3	9421
	10162	BINARY 1-8 DECODER (HIGH)	16	E3	9421
	10164	8-LINE MULTIPLEXER	16	E3	9421
	10174	DUAL 4-TO-1 MULTIPLEXER	16	E3	9421
	10175	QUINT LATCH	16	E3	9421
	10176	HEX D-TYPE FLIP/FLOP	16	E3	9421
	10178	BINARY COUNTER	16	E4	9422
	10184	2-BIT ALU	16	E4	9422
	10195	HEX INVERTER/BUFFER	16	E4	9422
	10197	HEX AND	16	E4	9422
	10216	TRIPLE LINE RECEIVER	16	E4	9422
	10231	DUAL D-TYPE FLIP/FLOP	16	E4	9422
1732-5956	(Kelvin)	see also 1732-5929 (non-Kelvin)			
	10110	DUAL 3-INPUT 3-OUTPUT OR	16	E1	9419
	10111	DUAL 3-INPUT 3-OUTPUT NOR	16	E1	9419
	10211	DUAL 3-INPUT 3-OUTPUT NOR	16	E4	9422
1732-5957	(Kelvin)	see also 1732-5928 (non-Kelvin)			
	10125	QUAD MECL-TO-TTL TRANSLATOR	16	E2	9420
1732-5958	(non-Kelvin)	see also 1732-5961 (Kelvin)			
	280-PIO	2 X 8-BIT PARALLEL I/O (see M1)	40	M13	9440
1732-5959	(Kelvin)	see also 1732-5960 (non-Kelvin)			
	6852	SYNC SERIAL DATA ADAPTOR	40	M12	9439
1732-5960	(non-Kelvin)	see also 1732-5959 (Kelvin)			
	6852	SYNC SERIAL DATA ADAPTOR	40	M12	9439
1732-5961	(Kelvin)	see also 1732-5958 (non-Kelvin)			
	280-PIO	2 X 8-BIT PARALLEL I/O (see M1)	40	M13	9440
1732-5962	(Kelvin)	see also 1732-5901 (non-Kelvin)			
	54LS85	4-BIT MAGNITUDE COMPARATOR	16	LST14	9302
	54LS109	DUAL J-K FLIP-FLOP (EDGE-TRIG)	16	LST14	9302
	54S109	DUAL J-K FLIP-FLOP (EDGE-TRIG)	16	ST8	9308
	54LS112	DUAL J-K FLIP-FLOP	16	LST14	9302
	54LS138	3-TO-8-LINE DECODER	16	LST15	9303
	54S138	3-TO-8 LINE DECODER	16	ST8	9308
	54LS139	DUAL 2-TO-4-LINE DECODER	16	LST15	9303
	54LS151	1-OF-8 MULTIPLEXER	16	LST15	9303
	54S151	1-OF-8 MULTIPLEXER	16	ST8	9308
	54LS157	QUAD 2-TO-1 MULTIPLEXER	16	LST15	9303
	54LS158	QUAD 2 TO 1 MULTIPLEXER	16	LST15	9303
	54165	8-BIT SHIFT REG PARALLEL IN	16	T16	9310
	54LS165	8-BIT SHIFT REG PARALLEL IN	16	LST15	9303
	54166	8-BIT SHIFT REG. (PARALLEL IN)	16	T16	9310
	54LS173	4-BIT D-TYPE REGISTER (TRI-S)	16	LST16	9304
	54174	HEX D-TYPE FLIP-FLOP	16	T16	9310
	54LS174	HEX D-TYPE FLIP-FLOP	16	LST16	9304
	54LS175	QUAD DOTYPE FLIP-FLOP	16	LST16	9304
	54S182	LOOK-AHEAD CARRY GENERATOR	16	ST8	9308
	54LS189	64-BIT RAM (TRI-STATE)	16	LST16	9304
	54S189	64-BIT RAM (TRI-STATE)	16	ST8	9308
	54LS191	BINARY UP/DOWN COUNTER	16	LST16	9304
	54LS193	BINARY UP/DOWN COUNTER	16	LST16	9304
	54LS194	4-BIT BI-DIRECTIONAL SHIFT REG.	16	LST16	9304

54LS195	4-BIT PARALLEL ACCESS SHIFT REG.	16	LST16	9304
54LS251	1-OF-8 MULTIPLEXER (TRI-STATE)	16	LST17	9305
54LS253	DUAL 1-OF-4 MULTIPLEXER (TRI-S)	16	LST17	9305
54S253	DUAL 1-OF-4 MULTIPLEXER (TRI-S)	16	ST8	9308
54LS257	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	LST17	9305
54S257	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	ST8	9308
54LS258	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	LST17	9305
54LS259	8-BIT ADDRESSABLE LATCH	16	LST17	9305
54LS279	QUAD S-R LATCH	16	LST18	9306
54LS289	64-BIT RAM	16	LST18	9306
54LS365	HEX BUS DRIVER	16	LST18	9306
54LS366	HEX BUS DRIVER (TRI-STATE)	16	LST18	9306
54LS367	HEX BUS DRIVER (TRI-STATE)	16	LST18	9306
54LS395	4-BIT SHIFT REGISTER (TRI-S)	16	LST18	9306
7423	EXP DUAL 4-INPUT POSITIVE NOR	16	T2	9401
7442A	BCD TO DEC CONVERTER	16	T3	9402
74LS42	BCD-TO-DEC CONVERTER	16	LST3	9475
7445	BCD TO DEC DECODER/DRIVER (O-C)	16	T3	9402
7446A	BCD TO 7-SEG DECODER/DRVR (O-C)	16	T3	9402
7447A	BCD TO 7-SEG DECODER/DRVR (O-C)	16	T3	9402
74LS47	BCD TO 7-SEGMENT DRIVER (O-C)	16	LST3	9475
7448	BCD TO 7-SEG DECODER/DRIVER	16	T3	9402
74LS48	BCD TO 7-SEGMENT DRIVER	16	LST3	9475
7485	4-BIT MAGNITUDE COMP	16	T5	9404
74LS85	4-BIT MAGNITUDE COMPARATOR	16	LST4	9476
74S85	4-BIT MAGNITUDE COMPARATOR	16	ST2	9485
7497	6-BIT RATE MULTIPLEXER	16	T6	9405
74L98	4-BIT SELECTOR/STORAGE REGISTER	16	T6	9405
74109	DUAL J-K FLIP/FLOP	16	T6	9405
74LS109A	DUAL J-K FLIP-FLOP	16	LST4	9476
74111	DUAL J-K M-S FLIP/FLOP	16	T6	9405
74LS112A	DUAL J-K FLIP/FLOP	16	LST5	9477
74120	DUAL PULSE SYNCHRONIZER/DRIVER	16	T7	9406
74S133	13-INPUT POSITIVE NAND	16	ST3	9486
74S134	12-INPUT POSITIVE NAND (TRI-S)	16	ST3	9486
74S135	QUAD EXCLUSIVE-OR/NOR	16	ST3	9486
74LS138	3-TO-8-LINE DECODER	16	LST6	9478
74S138	3-TO-8 LINE DECODER	16	ST3	9486
74LS139	DUAL 2-TO-4-LINE DECODER	16	LST6	9478
74S139	DUAL 2-TO-4 LINE DECODER	16	ST3	9486
74145	BCD TO DEC DECODER/DRIVER	16	T8	9407
74LS145	BCD TO DEC DECODER/DRIVER	16	LST6	9478
74148	8-TO-3-LINE PRIORITY ENCODER	16	T8	9407
74LS148	8-TO-3 LINE PRIORITY ENCODER	16	LST6	9478
74151	1 OF 8 MUX	16	T8	9407
74LS151	1-OF-8 MULTIPLEXER	16	LST6	9478
74S151	1-OF-8 MULTIPLEXER	16	ST3	9486
74153	DUAL 1 OF 4 MULTIPLEXER	16	T8	9407
74LS153	DUAL 1-OF-4 MULTIPLEXER	16	LST6	9478
74S153	DUAL 1-OF-4 MULTIPLEXER	16	ST4	9487
74155	DUAL 2-TO-4-LINE DECODER	16	T8	9407
74LS155	DUAL 2-TO-4 LINE DECODER	16	LST6	9478
74156	DUAL 2-TO-4-LINE DECODER (O-C)	16	T8	9407
74LS156	DUAL 2-TO-4 LINE DECODER (O-C)	16	LST6	9478

Adaptor	Device	Description	Pins	Number	(1732-)
	74157	QUAD 2 TO 1 MULTIPLEXER	16	T9	9408
	74LS157	QUAD 2-TO-1 MULTIPLEXER	16	LST6	9478
	74S157	QUAD 2-TO-1 MULTIPLEXER	16	ST4	9487
	74LS158	QUAD 2 TO 1 MULTIPLEXER	16	LST7	9479
	74S158	QUAD 2-TO-1 MULTIPLEXER	16	ST4	9487
	74160	DECADE COUNTER	16	T9	9408
	74161A	BINARY COUNTER	16	T9	9408
	74162	DECADE COUNTER	16	T9	9408
	74163	BINARY COUNTER	16	T9	9408
	74165	8-BIT SHIFT REG PARALLEL IN	16	T9	9408
	74LS165	8-BIT SHIFT REG PARALLEL IN	16	LST7	9479
	74166	8-BIT SHIFT REG PARALLEL IN	16	T9	9408
	74LS166	8-BIT SHIFT REG PARALLEL I/O	16	LST7	9479
	74170	4X4 REGISTER FILE	16	T10	9409
	74LS170	4X4 REGISTER FILE (O-C)	16	LST7	9479
	74173	4-BIT D-TYPE FLIP/FLOP (TRI-S)	16	T10	9409
	74LS173	4-BIT D-TYPE REGISTER (TRI-S)	16	LST7	9479
	74174	HEX D-TYPE FLIP/FLOP	16	T10	9409
	74LS174	HEX D-TYPE FLIP-FLOP	16	LST8	9480
	74175	QUAD D-TYPE FLIP/FLOP	16	T10	9409
	74LS175	QUAD D-TYPE FLIP-FLOP	16	LST8	9480
	74182	LOOK-AHEAD CARRY GENERATOR	16	T10	9409
	74S182	LOOK-AHEAD CARRY GENERATOR	16	ST4	9487
	74184	BCD TO BINARY CODE CONVERTER	16	T11	9410
	74185	BINARY TO BCD CODE CONVERTER	16	T11	9410
	74190	BCD UP/DOWN COUNTER	16	T11	9410
	74LS190	BCD UP/DOWN COUNTER	16	LST8	9480
	74191	BINARY UP/DOWN COUNTER	16	T11	9410
	74LS191	BINARY UP/DOWN COUNTER	16	LST8	9480
	74192	BCD UP/DOWN COUNTER	16	T11	9410
	74LS192	BCD UP/DOWN COUNTER	16	LST8	9480
	74193	BINARY UP/DOWN COUNTER	16	T11	9410
	74LS193	BINARY UP/DOWN COUNTER	16	LST8	9480
	74194	4-BIT BI-DIREC SHIFT REGISTER	16	T11	9410
	74LS194	4-BIT BI-DIREC SHIFT REGISTER	16	LST8	9480
	74195	4-BIT PARALLEL ACCESS SHIFT REG	16	T11	9410
	74LS195	4-BIT PARALLEL ACCESS SHIFT REG	16	LST8	9480
	74251	1 OF 8 MUX (TRI-STATE)	16	T12	9411
	74LS251	1-OF-8 MULTIPLEXER (TRI-STATE)	16	LST9	9481
	74S251	1-OF-8 MULTIPLEXER (TRI-STATE)	16	ST5	9488
	74LS253	DUAL 1 OF 4 MUX (TRI-STATE)	16	LST9	9481
	74LS257A	QUAD 1 OF 2 MUX (TRI-STATE)	16	LST9	9481
	74LS258	QUAD 1 OF 2 MUX (TRI-STATE)	16	LST10	9482
	74S258	QUAD 1-OF-2 MULTIPLEXER (TRI-S)	16	ST5	9488
	74LS259	8-BIT ADDRESSABLE LATCH	16	LST10	9482
	74265	QUAD COMPLEMENTARY-OUT ELEMENT	16	T13	9412
	74279	QUAD R-S LATCH	16	T13	9412
	74LS279	QUAD S-R LATCH	16	LST10	9482
	74283	4-BIT FULL ADDER	16	T13	9412
	74LS283	4-BIT FULL ADDER	16	LST10	9482
	74S283	4-BIT BINARY FULL ADDER	16	ST6	9489
	74298	QUAD 1 OF 2 MUX/LATCH	16	T14	9413
	74LS365	HEX BUS DRIVER	16	LST11	9483
	74366	HEX BUS DRIVER (TRI-STATE)	16	T14	9413

Adaptor	Device	Description	Pins	Number	(1732-)
	74LS366	HEX BUS DRIVER (TRI-STATE)	16	LST11	9483
	74367	HEX BUS DRIVER (TRI-STATE)	16	T14	9413
	74LS367	HEX BUS DRIVER (TRI-STATE)	16	LST11	9483
	74368	HEX BUS DRIVER (TRI-STATE)	16	T14	9413
	74LS368	HEX BUS DRIVER (TRI-STATE)	16	LST11	9483
	74LS375	4-BIT BISTABLE LATCH	16	LST11	9483
	74390	DUAL DECADE COUNTER	16	T14	9413
	74LS390	DUAL DECADE COUNTER	16	LST11	9483
	8205	1-OF-8 BINARY DECODER	16	M15	9442
	8216	BI-DIRECTIONAL BUS DRIVER	16	M15	9442
	8226	BI-DIRECTIONAL BUS DRIVER	16	M15	9442
1732-5963	(non-Kelvin)	see also 1732-5964 (Kelvin)			
	6828	PRIORITY INTERRUPT CONTROLLER	24	M10	9437
1732-5964	(Kelvin)	see also 1732-5963 (non-Kelvin)			
	6828	PRIORITY INTERRUPT CONTROLLER	24	M10	9437
1732-5965	(non-Kelvin)	see also 1732-5966 (Kelvin)			
	6800	8-BIT MICROPROCESSOR	40	M7	9434
1732-5966	(Kelvin)	see also 1732-5965 (non-Kelvin)			
	6800	8-BIT MICROPROCESSOR	40	M7	9434
1732-5967	(Kelvin)	see also 1732-5968 (non-Kelvin)			
	8080	8-BIT MICROPROCESSOR	40	M2	9429
1732-5968	(non-Kelvin)	see also 1732-5967 (Kelvin)			
	8080	8-BIT MICROPROCESSOR	40	M2	9429
1732-5971	(Kelvin)	see also 1732-5972 (non-Kelvin)			
	2708	1KX8 STATIC EPROM	24	R6	9443
1732-5972	(non-Kelvin)	see also 1732-5971 (Kelvin)			
	2708	1KX8 STATIC EPROM	24	R6	9443
1732-5973	(Kelvin)	see also 1732-5974 (non-Kelvin)			
	2716	2KX8 STATIC EPROM	24	R7	9444
1732-5974	(non-Kelvin)	see also 1732-5973 (Kelvin)			
	2716	2KX8 STATIC EPROM	24	R7	9444
1732-5975	(Kelvin)	see also 1732-5976 (non-Kelvin)			
	8259	INTERRUPT CONTROLLER	28	M5	9432
1732-5976	(non-Kelvin)	see also 1732-5975 (Kelvin)			
	8259	INTERRUPT CONTROLLER	28	M5	9432
1732-5977	(Kelvin)	see also 1732-5978 (non-Kelvin)			
	8085	8-BIT MICROPROCESSOR	40	M6	9433
1732-5978	(non-Kelvin)	see also 1732-5977 (Kelvin)			
	8085	8-BIT MICROPROCESSOR	40	M6	9433
1732-5979	(non-Kelvin)	see also 1732-5983 (Kelvin)			
	8224	CLOCK DRIVER	16	M3	9430
1732-5981	(non-Kelvin)	see also 1732-5982 (Kelvin)			
	8214	PRIORITY INTERRUPT CONTROLLER	24	M3	9430
1732-5982	(Kelvin)	see also 1732-5981 (non-Kelvin)			
	8214	PRIORITY INTERRUPT CONTROLLER	24	M3	9430
1732-5983	(Kelvin)	see also 1732-5979 (non-Kelvin)			
	8224	CLOCK DRIVER	16	M3	9430
1732-5984	(non-Kelvin)	see also 1732-5985 (Kelvin)			
	8035	8-BIT MICROPROCESSOR	40	M17	9446
	8039	8-BIT MICROPROCESSOR	40	M19	9448
	8048	8-BIT MICROPROCESSOR	40	M14	9441
	8048H	8-BIT MICROPROCESSOR	40	M23	9454
	8049	8-BIT MICROPROCESSOR	40	M18	9447
1732-5985	(Kelvin)	see also 1732-5984 (non-Kelvin)			

Adaptor	Device	Description	Pins	Number	(1732-)
	8035	8-BIT MICROPROCESSOR	40	M17	9446
	8039	8-BIT MICROPROCESSOR	40	M19	9448
	8048	8-BIT MICROPROCESSOR	40	M14	9441
	8048H	8-BIT MICROPROCESSOR	40	M23	9454
	8049	8-BIT MICROPROCESSOR	40	M18	9447
1732-5986	(Kelvin)	see also 1732-5987 (non-Kelvin)			
	6802	8-BIT MICROPROCESSOR	40	M8	9435
1732-5987	(non-Kelvin)	see also 1732-5986 (Kelvin)			
	6802	8-BIT MICROPROCESSOR	40	M8	9435
1732-5988	(non-Kelvin)	see also 1732-5989 (Kelvin)			
	6821	PERIPHERAL INTERFACE ADAPTOR	40	M9	9436
1732-5989	(Kelvin)	see also 1732-5988 (non-Kelvin)			
	6821	PERIPHERAL INTERFACE ADAPTOR	40	M9	9436
1732-5990	(Kelvin)	see also 1732-5991 (non-Kelvin)			
	6850	ASYNCHRONOUS INTERFACE ADAPTOR	24	M11	9438
1732-5991	(non-Kelvin)	see also 1732-5990 (Kelvin)			
	6850	ASYNCHRONOUS INTERFACE ADAPTOR	24	M11	9438
1732-5992	(non-Kelvin)	see also 1732-5993 (Kelvin)			
	8255A	PARALLEL I/O	40	M4	9431
1732-5993	(Kelvin)	see also 1732-5992 (non-Kelvin)			
	8255A	PARALLEL I/O	40	M4	9431
1732-5995	(Kelvin)	see also 1732-5918 (non-Kelvin)			
	Z-80	8-BIT MICROPROCESSOR (see M13)	40	M1	9428
1732-5996	(Kelvin)	see also 1732-5997 (non-Kelvin)			
	8228	BUS CONTROLLER	28	M3	9430
	8238	BUS CONTROLLER	28	M3	9430
1732-5997	(non-Kelvin)	see also 1732-5996 (Kelvin)			
	8228	BUS CONTROLLER	28	M3	9430
	8238	BUS CONTROLLER	28	M3	9430
1732-5998	(Kelvin)	see also 1732-5800 (non-Kelvin)			
	AM2901	4-BIT MICROPROCESSOR	40	M20	9449
	AM2910	4-BIT MICROPROCESSOR	40	M21	9450
1732-9616	(Kelvin)				
	2102	1KX1 RAM - STATIC MOS	16	R1	9423
	2112	256X4 RAM - STATIC MOS	16	R1	9423
	2114	1KX4 RAM - STATIC MOS	18	R1	9423
	93415	1KX1 RAM - STATIC BIPOLAR	16	R5	9427
	93470	4KX1 RAM - STATIC BIPOLAR	18	R5	9427
1732-9617	(Kelvin)				
	4096	4KX1 RAM - DYNAMIC MOS	16	R3	9425
	4116	16KX1 RAM - DYNAMIC MOS	16	R4	9426
	4164	64KX1 RAM - DYNAMIC SMOS	16	R10	9495

LIST H. CROSS REFERENCE TO DEVICES TESTABLE ON 2-CABLE HANDLER ADAPTORS

(* means device requires special non-Kelvin handler adaptor, see Lists A and B.)

Adaptors Devices

1732-5821 (non-Kelvin)	1732-5822 (Kelvin)	54LS85	54LS109	54S109	54LS112
54S112*	54LS138	54LS138	54LS139	54LS151	54LS157
54165	54LS165	54166	54LS173	54174	54LS174
54S175*	54S182	54LS189	54S189	54LS191	54LS193
54LS251	54LS253	54S253	54LS257	54S257	54LS258
54LS289	54LS365	54LS366	54LS367	54LS395	7423
7445	7446A	7447A	74LS47	7448	74LS48
74S85	7497	74L98	74109	74LS109A	74111
74120	74S133	74S134	74S135	74LS138	74S138
74145	74LS145	74148	74LS148	74151	74LS151
74LS153	74S153	74155	74LS155	74156	74LS156
74S157	74LS158	74S158	74160	74161A	74162
74LS165	74166	74LS166	74170	74LS170	74173
74LS174	74S174*	74175	74LS175	74S175*	74182
74185	74190	74LS190	74191	74LS191	74192
74LS193	74194	74LS194	74S194*	74195	74LS195
74LS251	74S251	74LS253	74LS257A	74LS258	74S258
74LS365	74279	74LS279	74283	74LS283	74S283
74LS366	74367	74LS367	74368	74LS368	74LS375
8205	8216	8226			
1732-5823 (Kelvin)	1732-5824 (non-Kelvin)	54LS83	7475	74LS75	7483A
74LS83A	7494	7496	74LS96		
1732-5825 (Kelvin)	1732-5826 (non-Kelvin)	5473	54H73	54LS73	54LS78
74LS73A	74LS78A	74H103			
1732-5829 (Kelvin)	1732-5830 (non-Kelvin)	5476	54LS76	7476	74LS76A
74H106					
1732-5831 (Kelvin)	1732-5832 (non-Kelvin)	8224			
1732-5835 (Kelvin)	1732-5839 (non-Kelvin)	AM2901	AM2910		
1732-5836 (non-Kelvin)		54S174	54S175	74S174	74S175
1732-5837 (Kelvin)	1732-5838 (non-Kelvin)	5400	54LS00	54S00	5401
5402	54LS02	54S02	5404	54L04	54LS04
5407	54LS08	54S08	54LS09	5410	54LS10
54S11	5420	54H20	54LS20	54S20	54LS21
54LS27	5430	54LS30	54S30	54LS32	54S32
54LS51	54S51	54LS74	54S74*	54LS86	54S86
54LS125	54LS164	54LS196	54LS393	7400	74LS00
74LS01	7402	74LS02	74S02	7403	74LS03
74LS04	74S04	7405	74LS05	74S05	7408
7409	74LS09	74S09	7410	74LS10	74S10
74S11	7412	74LS12	7413	74LS13	74H15
7416	7417	7420	74LS20	74S20	74H21
74LS22	74S22	7425	7426	74LS26	7427
74LS28	7430	74LS30	74S30	7432	74LS32
74LS33	7437	74LS37	74S37	7438A	74LS38
7450	7451	74LS51	74S51	74H52	7453
74LS54	74H55	74LS55	74H61	74S64	7470
7474	74LS74A	74S74*	7480	7486	74LS86
7495A	74LS95B	74107	74LS107A	74110	74LS113A
					74LS114A
					74S114*

Adaptors Devices

	74125	74126	74132	74136	7LS136	74S140	74152	74164
	74LS164	74176	74177	74180	74H183	74LS183	74196	74LS196
	74S196*	74197	74LS197	74S197*	74S260	74LS266	74278	74LS280
	74S280	74293	74LS293	74393	74LS393			
1732-5840 (non-Kelvin)					74S195			
1732-5841 (Kelvin)	1732-5842 (non-Kelvin)				54LS90	54LS92	54LS93	7490A
	7490A	74LS90	7491A	74LS91	7492A	74LS92	7493A	74LS93
1732-5846 (non-Kelvin)					54S112	74S112A		
1732-5850 (non-Kelvin)					74S194			
1732-5854 (non-Kelvin)					74S114A			
1732-5857 (Kelvin)	1732-5858 (non-Kelvin)				74LS221			
1732-5861 (Kelvin)	1732-5862 (non-Kelvin)				54LS123	74LS123		
1732-5865 (Kelvin)	1732-5866 (non-Kelvin)				74LS122			
1732-5867 (Kelvin)	1732-5868 (non-Kelvin)				54LS244	54LS245	54LS273	54LS299
	74LS240	74S240	74LS241	74S241	74LS244	74S244	74LS245	74273
	74LS273	74276	74LS299	74S299*	8282	8283	8286	8287
	8288							
1732-5871 (Kelvin)	1732-5872 (non-Kelvin)				54LS160	54LS161	54LS163	54LS169
	74LS160A	74LS161A	74S161	74LS162A	74S162	74LS163A	74S163	74S169
1732-5876 (non-Kelvin)					74S196	74S197		
1732-5877 (Kelvin)	1732-5878 (non-Kelvin)				54LS374	74LS373	74S373	74LS374
	74S374							
1732-5879 (Kelvin)	1732-5880 (non-Kelvin)				54154	54LS181	74116	74150
	74154	74159	74172	74181	74LS181	74S181	74198	74199
	8212	8253						
1732-5884 (non-Kelvin)					54S74	74S74A		
1732-5888 (non-Kelvin)					74S299			
1732-5889 (Kelvin)	1732-5890 (non-Kelvin)				6502			
1732-5891 (Kelvin)	1732-5892 (non-Kelvin)				6809			
1732-5893 (Kelvin)	1732-5894 (non-Kelvin)				74123	74221		
1732-5895 (Kelvin)	1732-5896 (non-Kelvin)				6800			
1732-5897 (Kelvin)	1732-5898 (non-Kelvin)				8080			



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